LINEAR/SWITCHMODE VOLTAGE REGULATOR HANDBOOK

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PREFACE

In most electronic systems, voltage regulation is required for various functions. Today's complex electronic systems are requiring greater regulating performance, higher efficiency and lower parts count. Present integrated circuit and power package technology have produced IC voltage regulators which can ease the task of regulated power supply design, provide the performance required and remain cost effective. Available in a growing variety, Motorola offers a wide range of regulator products from fixed and adjustable voltage types to special-function and switching regulator control ICs.

This handbook describes Motorola's voltage regulator products and provides information on applying these products. Basic Linear regulator theory and switching regulator topologies has been included along with practical design examples. Other relevant topics include: trade-offs of Linear versus switching regulators, series pass elements for Linear regulators, switching regulator component design considerations, heatsinking, construction and layout, power supply supervision and protection, and reliability. A Motorola regulator selector guide along with data sheets and an industry cross-reference are also contained in this handbook.

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SECTION 1
BASIC LINEAR REGULATOR THEORY

A. THE IC VOLTAGE REGULATOR

The basic functional block diagram of an integrated circuit voltage regulator is shown in Figure 1-1. It consists of a stable reference, whose output voltage is V_{REF}, and a high gain error amplifier. The output voltage, V_o, is equal to, or a multiple of, V_{REF}. The regulator will tend to keep V_o constant by sensing any changes in V_o and trying to return it to its original value. Therefore, the ideal voltage regulator could be considered a voltage source with a constant output voltage. However, in practice the IC regulator is better represented by the model shown in Figure 1-2.

In this figure, the regulator is modeled as a voltage source with a positive output impedance, Z_o. The value of the voltage source, V, is not constant; instead, it varies with changes in supply voltage, V_{CC}, and with changes in IC junction temperature, T_j, induced by changes in ambient temperature and power dissipation. Also, the regulator output voltage, V_o, is affected by the voltage drop across Z_o, caused by the output current, I_o. In the following text, the reference and amplifier sections will be described, and their contributions to the changes in the output voltage analyzed.

B. THE VOLTAGE REFERENCE

Naturally, the major requirement for the reference is that it be stable; variations in supply voltage or junction temperature should have little or no effect on the value of the reference voltage, V_{REF}.

The Zener Diode Reference

The simplest form of a voltage reference is shown in Figure 1-3a. It consists of a resistor and a zener diode. The zener voltage, V_Z, is used as the reference voltage. In order to determine V_Z, consider Figure 1-3b. The zener diode, VR1, of Figure 1-3a has been replaced with its equivalent circuit model and the value of V_Z is therefore given by (at a constant junction temperature):

$$V_Z = V_{BZ} + I_Z Z_Z = V_{BZ} + \left(\frac{V_{CC} - V_{BZ}}{R + Z_Z}\right) Z_Z \qquad (1)$$

where V_{BZ} = zener breakdown voltage

I_Z = zener current

Z_Z = zener impedance at I_Z

Note that changes in the supply voltage give rise to changes in the zener current, thereby changing the value of V_Z, the reference voltage.

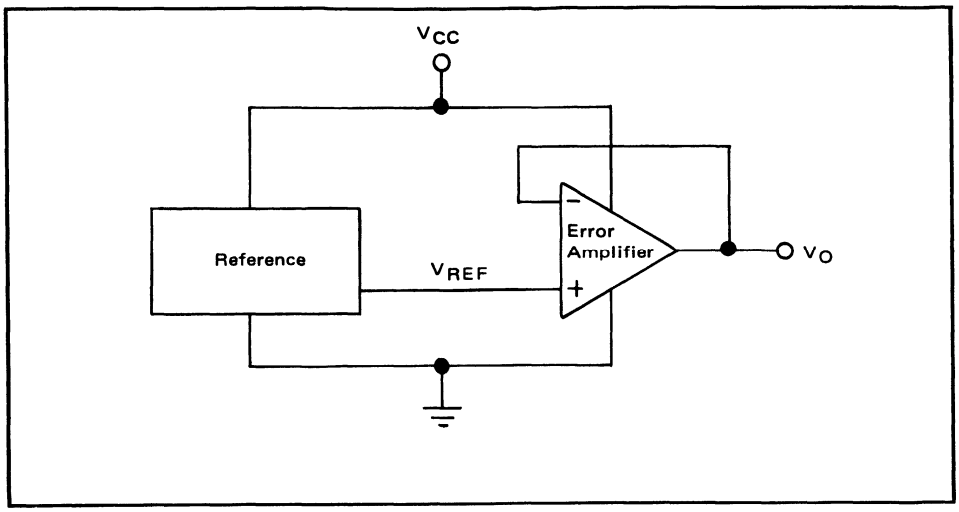


Figure 1-1. Voltage Regulator Functional Block Diagram

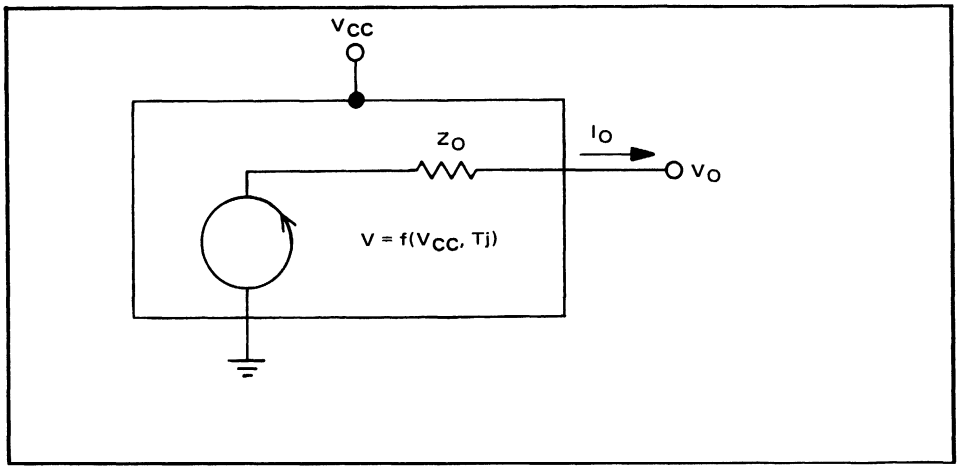


Figure 1-2. Voltage Regulator Equivalent Circuit Model

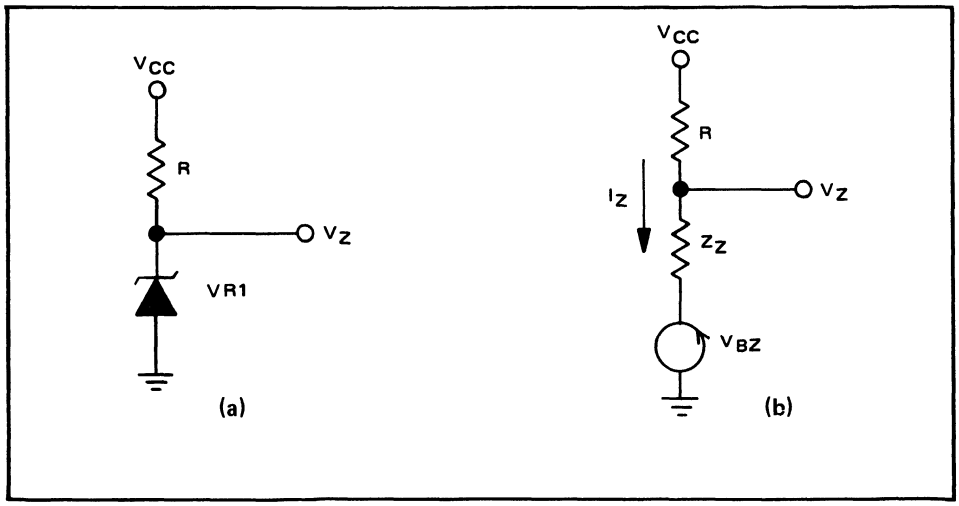


Figure 1-3. Zener Diode Reference

The Constant Current — Zener Reference

The effect of zener impedance can be minimized by driving the zener diode with a constant current as shown in Figure 1-4. The value of the zener current is largely independent of V_{CC} and is given by:

$$I_Z = \frac{V_{BEQ1}}{R_{SC}} \tag{2}$$

where V_{BEQ1} = base-emitter voltage of Q1

This gives a reference voltage of:

$$V_{REF} = V_Z + V_{BEQ1} = V_{BZ} + I_Z Z_Z + V_{BEQ1} \tag{3}$$

where Iz is constant and given by equation 2.

The reference voltage (about 7 V) of this configuration is therefore largely independent of supply voltage variations. This configuration has the additional benefit of better temperature stability than that of a simple resistor-zener reference.

Referring back to Figure 1-3a, it can be seen that the reference voltage temperature stability is equal to that of the zener diode, VR1. The stability of zener diodes used in most integrated circuitry is about +2.2 mV/°C or ≃ .04%/°C(for a 6.2 V zener). If the junction temperature varies 100°C, the zener, or reference, voltage would vary 4%. A variation this large is usually unacceptable.

However, the circuit of Figure 1-4 does not have this drawback. Here the positive 2.2 mV/°C temperature coefficient (TC) of the zener diode is offset by the negative 2.2 mV/°C TC of the V_{BE} of Q1. This results in a reference voltage with very stable temperature characteristics.

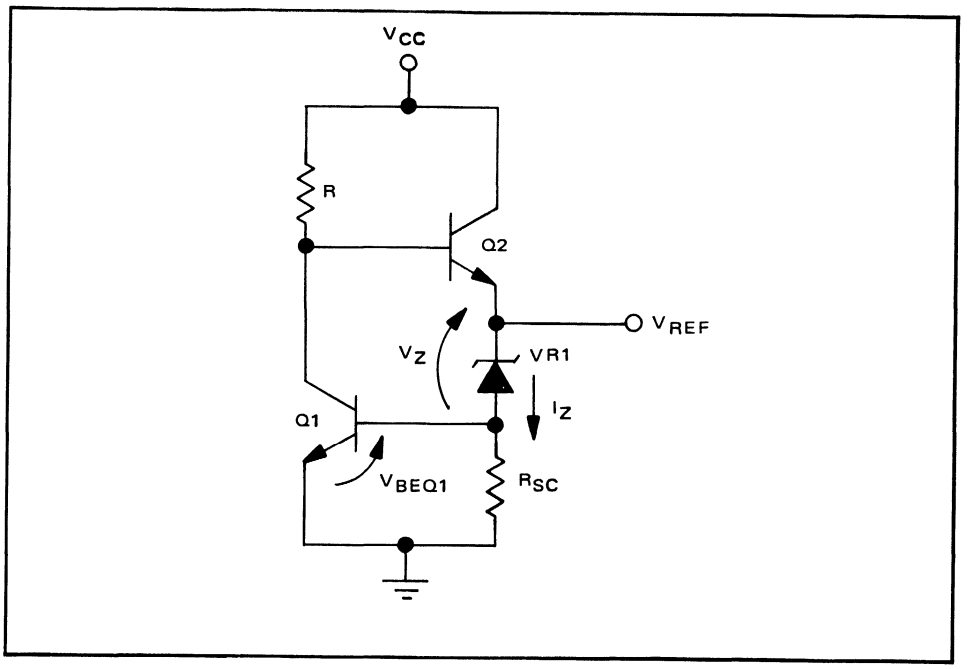


Figure 1-4. Constant Current – Zener Reference

The Bandgap Reference

Although very stable, the circuit of Figure 1-4 does have a disadvantage in that it requires a supply voltage of 9 volts or more. Another type of stable reference which requires only a few volts to operate was described by Widlar[1] and is shown in Figure 1-5. In this circuit V_{REF} is given by:

$$V_{REF} = V_{BEQ3} + I_2R_2 \tag{4}$$

where $$I_2 = \frac{V_{BEQ1} - V_{BEQ2}}{R_1}$$ (neglecting base currents)

The change in V_{REF} with junction temperature is given by:

$$\Delta V_{REF} = \Delta V_{BE3} + \left\{\frac{\Delta V_{BEQ1} - \Delta V_{BEQ2}}{R_1}\right\} R_2 \tag{5}$$

It can be shown that,

$$\Delta V_{BEQ1} = \Delta T_j \, K \, \ln I_1 \tag{6}$$

and $$\Delta V_{BEQ2} = \Delta T_j \, K \, \ln I_2 \tag{7}$$

where K = a constant

ΔT_j = change in junction temperature

and $I_1 > I_2$

Combining (5), (6), and (7)

$$\Delta V_{REF} = \Delta V_{BEQ3} + \Delta T_j K \left(\frac{R_2}{R_1}\right) \ln\frac{I_1}{I_2} \tag{8}$$

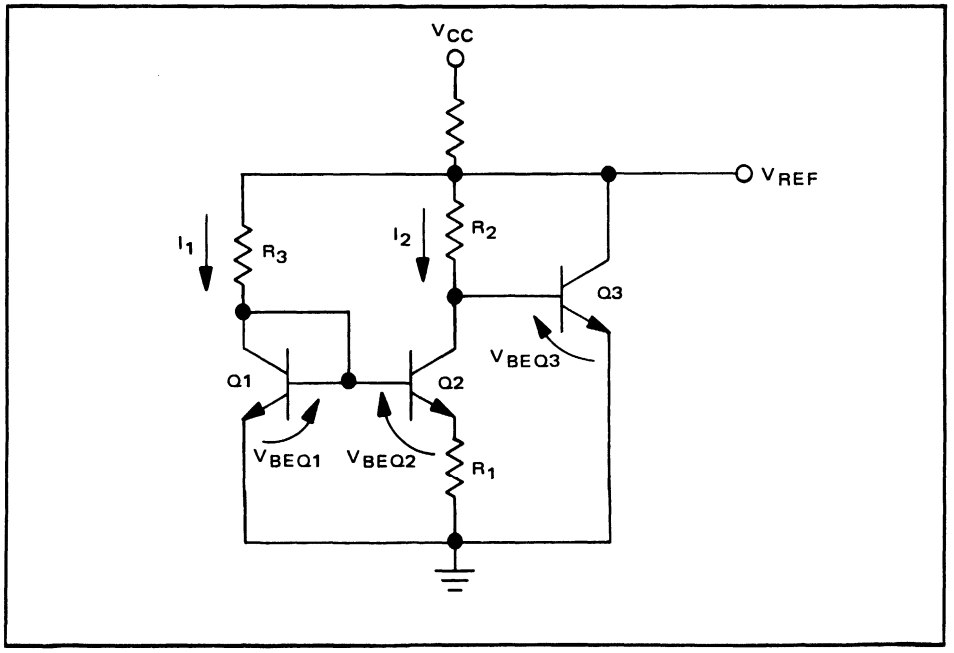


Figure 1-5. Bandgap Reference

Since ΔV_{BEQ3} is negative, and with $I_1 > I_2$, $\ln I_1/I_2$ is positive, the net change in V_{REF} with temperature variations can be made to equal zero by appropriately selecting the values of I_1, R_1, and R_2.

C. THE ERROR AMPLIFIER

Given a stable reference, the error amplifier becomes the determining factor in integrated circuit voltage regulator performance. Figure 1-6 shows a typical differential error amplifier in a voltage regulator configuration. With a constant supply voltage, V_{CC}, and junction temperature, the output voltage is given by:

$$V_O = A_{VOL}\, v_i - Z_{OL}\, I_O = A_{VOL}\{(V_{REF} \pm V_{IO}) - V_O\, \beta\} - Z_{OL}\, I_O \qquad (9)$$

where A_{VOL} = amplifier open loop gain

V_{IO} = input offset voltage

Z_{OL} = open loop output impedance

$\beta = \dfrac{R_1}{R_1 + R_2}$ = feedback ratio (β is always ≤ 1)

I_O = output current

v_i = true differential input voltage

Manipulating (9)

$$V_O = \frac{(V_{REF} \pm V_{IO}) - \dfrac{Z_{OL}}{A_{VOL}} I_O}{\beta + \dfrac{1}{A_{VOL}}} \qquad (10)$$

Note that if the amplifier open loop gain is infinite, this expression reduces to:

$$V_O = \frac{1}{\beta}(V_{REF} \pm V_{IO}) = (V_{REF} \pm V_{IO})\left(1 + \frac{R_2}{R_1}\right) \qquad (11)$$

The output voltage can thus be set any value equal to or greater than ($V_{REF} \pm V_{IO}$). Note also that if A_{VOL} is not infinite, with constant output current (a non-varying output load), the output voltage can still be "tweaked in" by varying R_1 and R_2, even though V_O will not exactly equal that given by equation 11.

Assuming a stable reference and a finite value of A_{VOL}, inaccuracy of the output voltage can be traced to the following amplifier characteristics:

1. **Amplifier input offset voltage drift —**
The input transistors of integrated circuit amplifiers are usually not perfectly matched. As in operational amplifiers, this is expressed in terms of an input offset voltage, V_{IO}. At a given temperature, this effect can be nulled out of the desired output voltage by adjusting V_{REF} or $1/\beta$. However, V_{IO} drifts with temperature, typically ± 5 to 15 μV/°C, causing a proportional change in the output voltage. Closer matching of the internal amplifier input transistors, minimizes this effect, as does selecting a feedback ratio, β, to be close to unity.

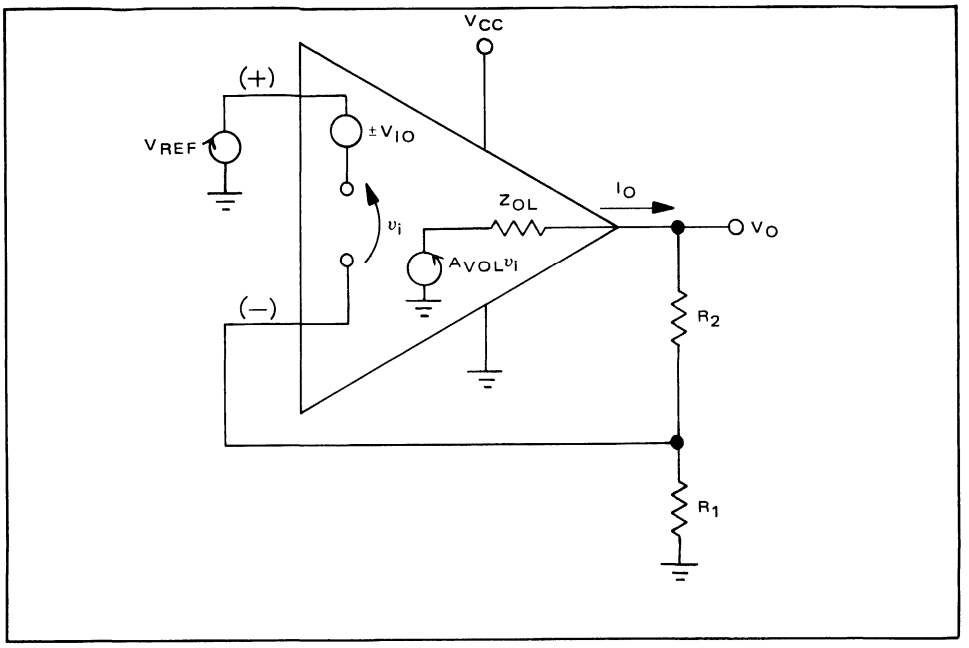


Figure 1-6. Typical Voltage Regulator Configuration

2. **Amplifier power supply sensitivity —**
Changes in regulator output voltage due to power supply voltage variations can be attributed to two amplifier performance parameters: power supply rejection ratio (PSRR) and common-mode rejection ratio (CMRR). In modern integrated circuit regulator amplifiers, the utilization of constant current sources gives such large values of PSRR that this effect on Vo can usually be neglected. However, supply voltage changes can affect the output voltage since these changes appear as common mode voltage changes, and they are best measured by the CMRR.

The definition of common mode voltage, V_{CM}, illustrated by Figure 1-7a, is:

$$V_{CM} = \left(\frac{V_1 + V_2}{2}\right) - \left(\frac{V_+ + V_-}{2}\right) \qquad (12)$$

where V_1 = voltage on amplifier non-inverting input

V_2 = voltage on amplifier inverting input

V_+ = positive supply voltage

V_- = negative supply voltage

In an ideal amplifier, only the differential input voltage ($V_1 - V_2$) has any effect on the output voltage; the value of V_{CM} would not effect the output. In fact, V_{CM} does influence the amplifier output voltage. This effect can be modeled as an additional voltage offset at the amplifier input equal to $V_{CM}/CMRR$ as shown in Figures 1-7b and 1-8. The latter figure is the same configuration as Figure 1-6, with amplifier input offset voltage and output impedance deleted for clarity and common-mode voltage effects added. The output voltage of this configuration is given by:

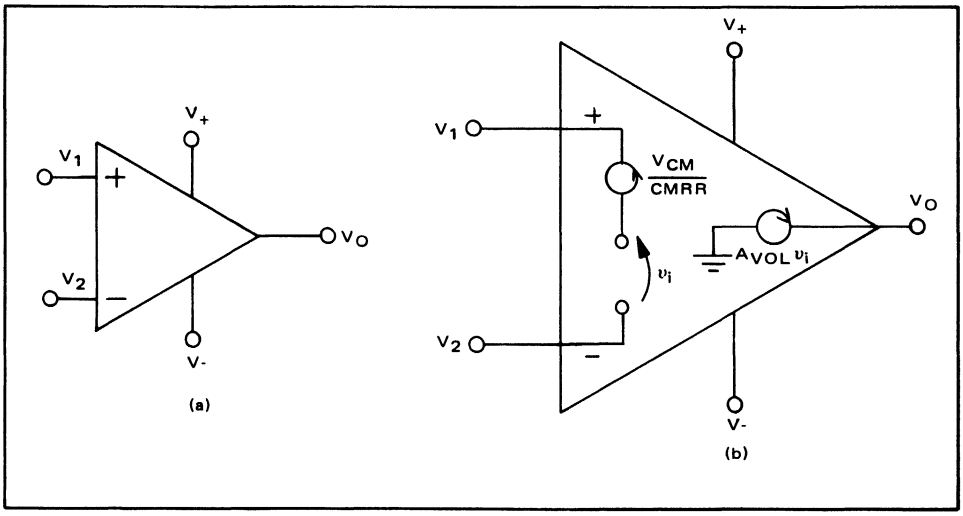


Figure 1-7. Definition of Common-mode Voltage Error

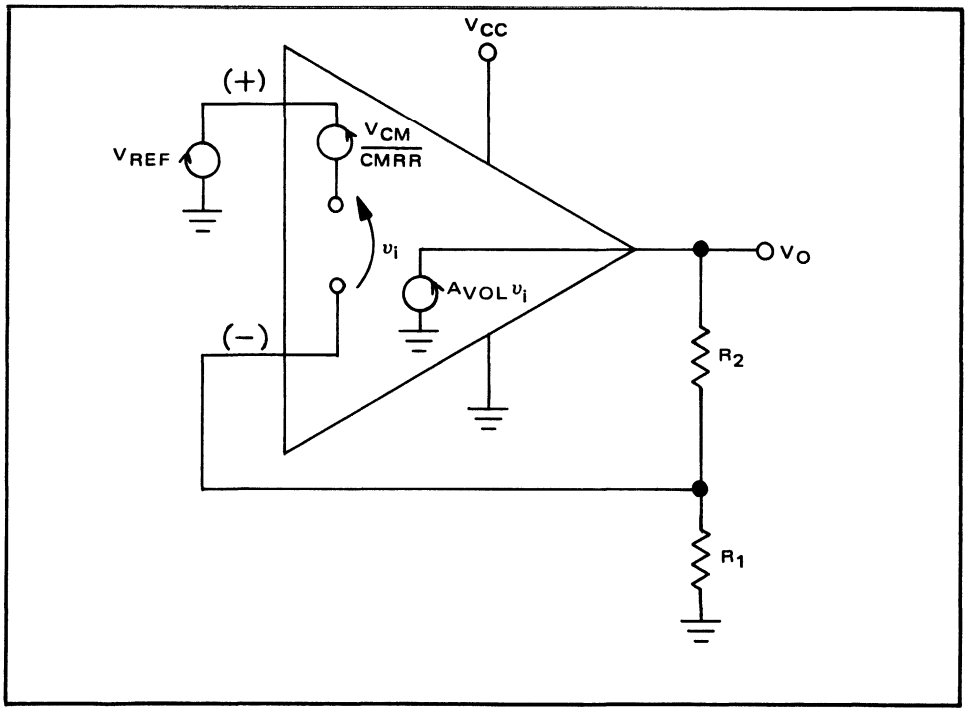


Figure 1-8. Common-mode Regulator Effects

$$V_O = A_{VOL} v_i = A_{VOL}(V_{REF} - \frac{V_{CM}}{CMRR} - \beta V_O) \tag{13}$$

Manipulating,

$$V_O = \frac{(V_{REF} - \frac{V_{CM}}{CMRR})}{\beta + \frac{1}{A_{VOL}}} \tag{14}$$

where $V_{CM} = V_{REF} - \frac{V_{CC}}{2}$ (15)

and CMRR = common-mode rejection ratio

It can be seen from equations (14) and (15) that the output can vary when V_{CC} varies. This can be reduced by designing the amplifier to have a high A_{VOL}, a high CMRR, and by choosing the feedback ratio, β, to be unity.

3. **Amplifier Output Impedance —**

Referring back to equation (9), it can be seen that the equivalent regulator output impedance, Z_O, is given by:

$$Z_O = \frac{\Delta V_O}{\Delta I_O} \simeq \frac{Z_{OL}}{\beta A_{VOL}} \tag{16}$$

This impedance must be as low as possible, in order to minimize load current effects on the output voltage. This can be accomplished by lowering Z_{OL}, choosing an amplifier with high A_{VOL}, and by selecting the feedback ratio, β, to be unity.

A simple way of lowering the effective value of Z_{OL} is to make an impedance transformation with an emitter follower, as shown in Figure 1-9. Given a change in output current, ΔI_O, the amplifier will see a change of only $\Delta I_O/h_{FEQ1}$ in its output current, I_O'. Therefore Z_{OL} in equation (16) has been effectively reduced to Z_{OL}/h_{FEQ1}, reducing the overall regulator output impedance, Z_O.

D. THE REGULATOR WITHIN A REGULATOR APPROACH

In the preceding text, we have analyzed the sections of an integrated circuit voltage regulator and determined how they contribute to its non-ideal performance characteristics. These are shown in Table 1-1 along with procedures which minimize their effects.

It can be seen that in all cases regulator performance can be improved by selecting A_{VOL} as high as possible and $\beta = 1$. Since a limit is soon approached in how much A_{VOL} can be practically obtained in an integrated circuit amplifier, selecting a feedback ratio, β, equal to unity is the only viable way of improving total regulator performance, especially in reducing regulator output impedance. However, this method presents a basic problem to the regulator designer. If the configuration of Figure 1-6 is used, the output voltage cannot be adjusted to a value other than V_{REF}. The solution is to utilize a different regulator configuration known as the "regulator within a regulator approach."[2] Its greatest benefit is in reducing total regulator output impedance.

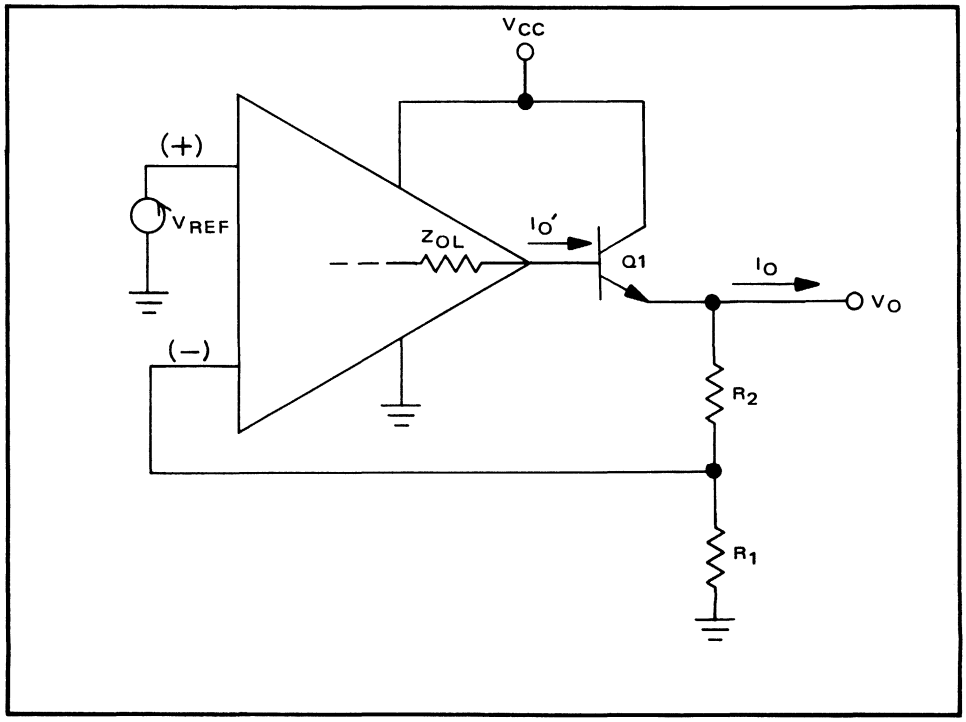


Figure 1-9. Emitter Follower Output

TABLE 1-1

VO CHANGES SECTION	EFFECT CAN BE INDUCED BY	MINIMIZED BY SELECTING
Reference	Vcc	1. Constant current-zener method 2. Bandgap reference
	Tj	1. Bandgap reference 2. TC compensated zener method
Amplifier	Vcc	1. High CMRR amplifier 2. High AVOL amplifier 3. $\beta = 1$
	Tj	1. Low VIO drift amplifier 2. High AVOL amplifier 3. $\beta = 1$
	Io	1. Low ZOL amplifier 2. High AVOL amplifier 3. Additional emitter follower output 4. $\beta = 1$

As shown in Figure 1-10, amplifier A1 sets up a voltage, V_1, given by:

$$V_1 \simeq V_{REF}\left(1 + \frac{R_2}{R_1}\right) \tag{17}$$

V_1 now serves as the reference voltage for amplifier A2, whose output voltage, V_O, is given by:

$$V_O \simeq V_1 \simeq V_{REF}\left(1 + \frac{R_2}{R_1}\right) \tag{18}$$

Note that the output impedance of A2, and therefore the regulator output impedance, has been minimized by selecting A2's feedback factor to be unity; and that output voltage can still be set at voltages greater than V_{REF} by adjusting R_1 and R_2.

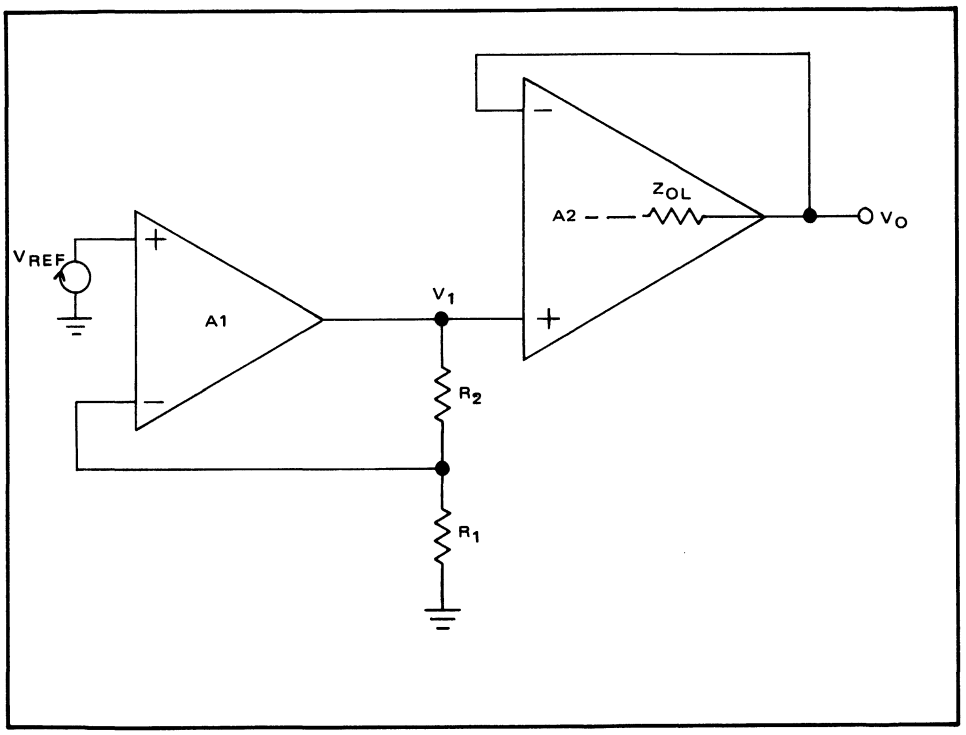


Figure 1-10. The "Regulator within a Regulator" Configuration

[1]Widlar, R. J., "New Developments in IC Voltage Regulators," IEEE Journal of Solid State Circuits, Feb. 1971, Vol. SC-6, pgs. 2-7.

[2]Tom Fredericksen, IEEE Journal of Solid State Circuits, Vol. SC-3, Number 4, Dec. 1968, "A Monolithic High Power Series Voltage Regulator."

SECTION 2

SELECTING A LINEAR IC VOLTAGE REGULATOR

A. SELECTING THE TYPE OF REGULATOR

There are five basic linear regulator types; these are the positive, negative, fixed output, tracking and floating regulators. Each has its own particular characteristics and best uses, and selection depends on the designer's needs and trade-offs in performance and cost.

1. Positive Versus Negative Regulators

In most cases, a positive regulator is used to regulate positive voltages and a negative regulator negative voltages. However, depending on the system's grounding requirements, each regulator type may be used to regulate the "opposite" voltage.

Figures 2-1a and 2-1b show the regulators used in the conventional and obvious mode. Note that the ground reference for each (indicated by the heavy line) is continuous. Several positive regulators could be used with the same input supply to deliver several voltages with common grounds; negative regulators may be utilized in a similar manner.

If no other common supplies or system components operate off the input supply to the regulator, the circuits of Figures 2-1c and 2-1d may be used to regulate positive voltages with a negative regulator and vice versa. In these configurations, the input supply is essentially floated, i.e., neither side of the input is tied to the system ground.

There are methods of utilizing positive regulators to obtain negative output voltages without sacrificing ground bus continuity; however, these methods are only possible at the expense of increased circuit complexity and cost. An example of this technique is shown in Section 3.

2. Three Terminal, Fixed Output Regulators

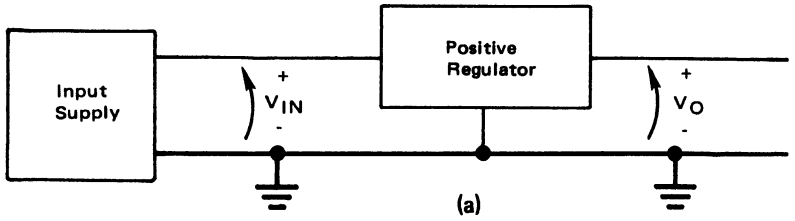
These regulators offer the designer a simple, inexpensive way to obtain a source of regulated voltage. They are available in a variety of positive or negative output voltages and current ranges.

The advantages of these regulators are:

a) Easy to use.
b) Internal overcurrent and thermal protection.
c) No circuit adjustments necessary.
d) Low cost.

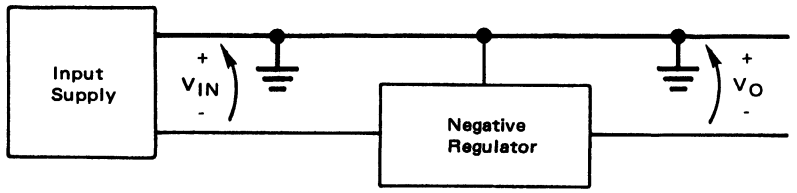
Their disadvantages are:

a) Output voltage cannot be precisely adjusted. (Methods for obtaining adjustable outputs are shown in Section 3).
b) Available only in certain output voltages and currents.
c) Obtaining greater current capability is more difficult than with other regulators. (Methods for obtaining greater output currents are shown in Section 3.)



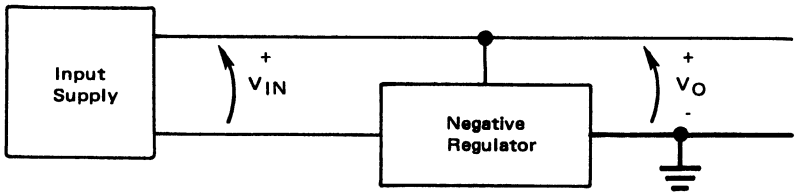
(a)

Positive Output Using Positive Regulator



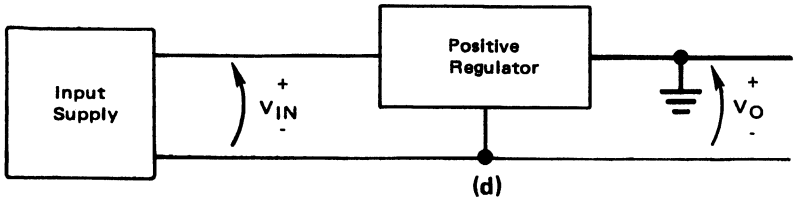
(b)

Negative Output Using Negative Regulator



(c)

Positive Output Using Negative Regulator



(d)

Negative Output Using Positive Regulator

Figure 2-1. Regulator Configurations

3. **Three Terminal, Adjustable Output Regulators**

Like the three terminal fixed regulators, the three terminal adjustable regulators are easy and inexpensive to use. These devices provide added flexibility with output voltage adjustable over a wide range, from 1.2 V to nearly 40 V, by means of an external, two-resistor voltage divider. A variety of current ranges from 100 mA to 3.0 Amperes are available.

4. **Tracking Regulators**

Often a regulated source of symmetrical positive and negative voltage is required for supplying op amps, etc. In these cases, a tracking regulator is required. In addition to supplying regulated positive and negative output voltages, the tracking regulator assures that these voltages are balanced; in other words, the midpoint of the positive and negative output voltages is at ground potential.

This function can be implemented using a positive output regulator together with an op amp or negative output regulator. However, this method results in the use of two IC packages and a multitude of external components. To minimize component count, an IC is offered which performs this function in a single package: the MC1568/MC1468 ±15V tracking regulator.

5. **Floating Regulator**

If the desired output voltage is in excess of 40 volts, a floating regulator such as the MC1466L should be considered. The output voltage of this regulator can be any magnitude and is limited only by the capabilities of an external transistor. However, an additional floating low voltage input supply is required.

B. SELECTING AN IC REGULATOR

Once the type of regulator is decided upon, the next step is to choose a specific device. As an aid in choosing an appropriate IC regulator, a Selection Guide is contained in Section 17.

To provide higher currents than are available from monolithic technologies, an IC regulator will often be used as a driver to a boost transistor. This complicates the selection and design task, as there are now several overlapping solutions to many of the design problems.

Unfortunately, there is no exact step-by-step procedure that can be followed which will lead to the ideal regulator and circuit configuration for a specific application. The regulating circuit that is finally accepted will be a compromise between such factors as performance, cost, size and complexity.

Because of this, the following general design procedure is suggested:

1. Select the regulators which meet or exceed the requirements for line regulation, load regulation, TC of the output voltage and operating ambient temperature range. At this point, do not be overly concerned with the regulator capabilities in terms of output voltage, output current, SOA and special features.
2. Next, select application circuits from Section 3 which meet the requirements for output current, output voltage, special features, etc. Preliminary designs using the chosen regulators and circuit configurations are then possible. From these designs a judgement can be made by the designer as to which regulator — circuit configuration combination best meets his requirements in terms of cost, size and complexity.

SECTION 3
LINEAR REGULATOR CIRCUIT CONFIGURATION AND DESIGN CONSIDERATIONS

Once the IC regulators, which meet the designer's performance requirements, have been selected, the next step is to determine suitable circuit configurations. Initial designs are devised and compared to determine the IC regulator/circuit configuration that best meets the designer's requirements. In this section, several circuit configurations and design equations are given for the various regulator ICs. Additional circuit configurations can be found on the device data sheets (see Section 18). Organization is first by regulator type and then by variants, such as current boost. Each circuit diagram has component values for a particular voltage and current regulator design.

A. Positive, Adjustable
B. Negative, Adjustable
C. Positive, Fixed
D. Negative, Fixed
E. Tracking
F. Floating
G. Special
    1. Obtaining Extended Output Voltage Range
    2. Electronic Shutdown
H. General Design Considerations

It should be noted that all circuit configurations shown have constant current limiting; if foldback limiting is desired, see Section 4C for techniques and design equations.

A. POSITIVE, ADJUSTABLE OUTPUT IC REGULATOR CONFIGURATIONS

1. Basic Regulator Configurations

Positive Three-Terminal Adjustables

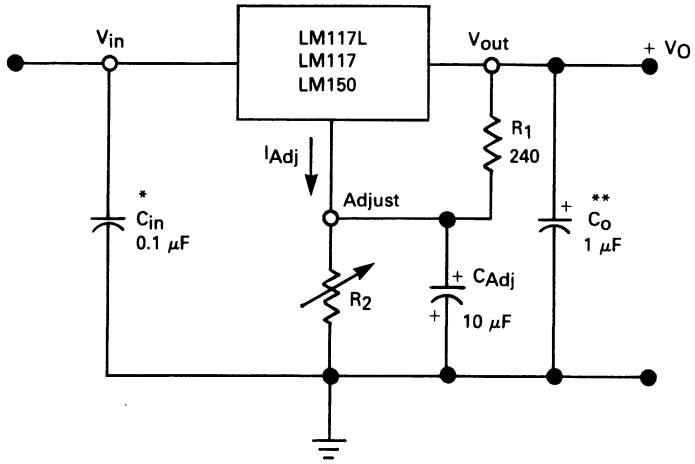
These adjustables, comprised of the LM117L, LM117, and LM150 series devices range in output currents of 100 mA, 500 mA, 1.5 A, and 3.0 A respectively. All of these devices utilize the same basic circuit configuration as shown in Figure 3-1A.

MC1723(C)

The basic circuit configurations for the MC1723(C) regulator are shown in Figures 3-3A and 3-2A. For output voltages from $\simeq$ 7 V to 37 V the configuration of Figure 3-2A can be used, while Figure 3-3A can be used to obtain output voltages from 2 V to $\simeq$ 7 V.

2. Output Current Boosting

If output currents greater than those available from the basic circuit configurations are desired, the current boost circuits shown in this section can be used. The output currents which can be obtained with these configurations are limited only by the capabilities of the external pass element(s).



* C_{in} is required if regulator is located an appreciable distance from power supply filter.

** C_O is not needed for stability, however it does improve transient response.

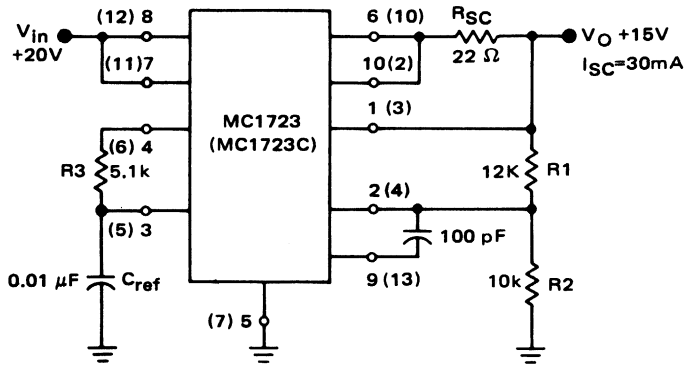
† C_{Adj} is not required; however, it does improve Ripple Rejection

$$V_{out} = 1.25\ V\left(1 + \frac{R_2}{R_1}\right) + I_{Adj}\,R_2$$

Since I_{Adj} is controlled to less than 100 μA, the error associated with this term is negligible in most applications.

Figure 3-1A — Basic Configuration for Positive, Adjustable Ouput Three-Terminal Regulators

Pin Numbers Adjacent to Terminals are for the Metal Package.
Pin Numbers in Parenthesis are for the Dual In-Line Package.



$$R_{SC} \cong \frac{0.66V}{I_{SC}} \; ; \; 10\,k\Omega < R1+R2 < 100\,k\Omega$$

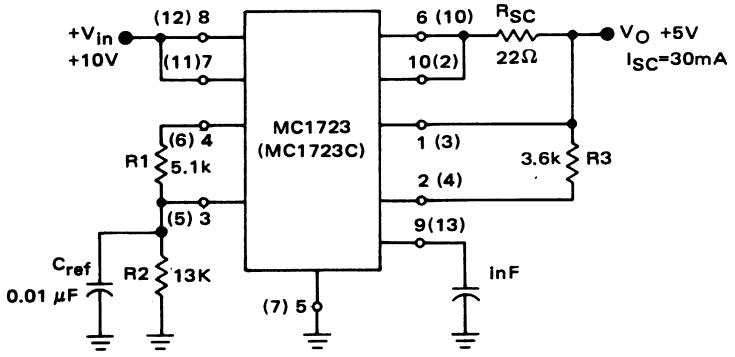
$$R3 \cong R1 \parallel R2 \; ; \; 0 \leq C_{REF} \leq 0.1\mu F$$

$$R2 = \frac{V_{REF}}{V_O}(R1+R2) \approx \frac{7V}{V_O}(R1+R2)$$

Values shown are for a [15V, 30mA] regulator using an MC1723CL for a $T_{A_{MAX}} = 25^{\circ}C$

Figure 3-2A. MC1723 Basic Circuit Configuration for $V_{REF} \leq V_O \leq 37V$

Pin Numbers Adjacent to Terminals are for the Metal Package.
Pin Numbers in Parenthesis are for the Dual In-Line Package.



$$R_{SC} \simeq \frac{0.66V}{I_{SC}} \; ; \; 10k\Omega < R1+R2 < 100k\Omega$$

$$R2 = \frac{V_O}{V_{REF}}(R1+R2) \simeq \frac{V_O}{7V}(R1+R2); \; R3 = R1 \parallel R2$$

$$0 < C_{REF} < 0.1\mu F$$

Values shown are for a [5V, 30mA] regulator using an MC1723CL for a $T_{A_{MAX}} = 70^{\circ}C$

Figure 3-3A. MC1723 Basic Circuit Configuration for $2v \leq V_O \leq V_{REF}$

To obtain greater output currents with the MC1723 the configurations shown in Figures 3-4A and 3-5A can be used. Figure 3-4A uses an NPN external pass element, while a PNP is used in Figure 3-5A.

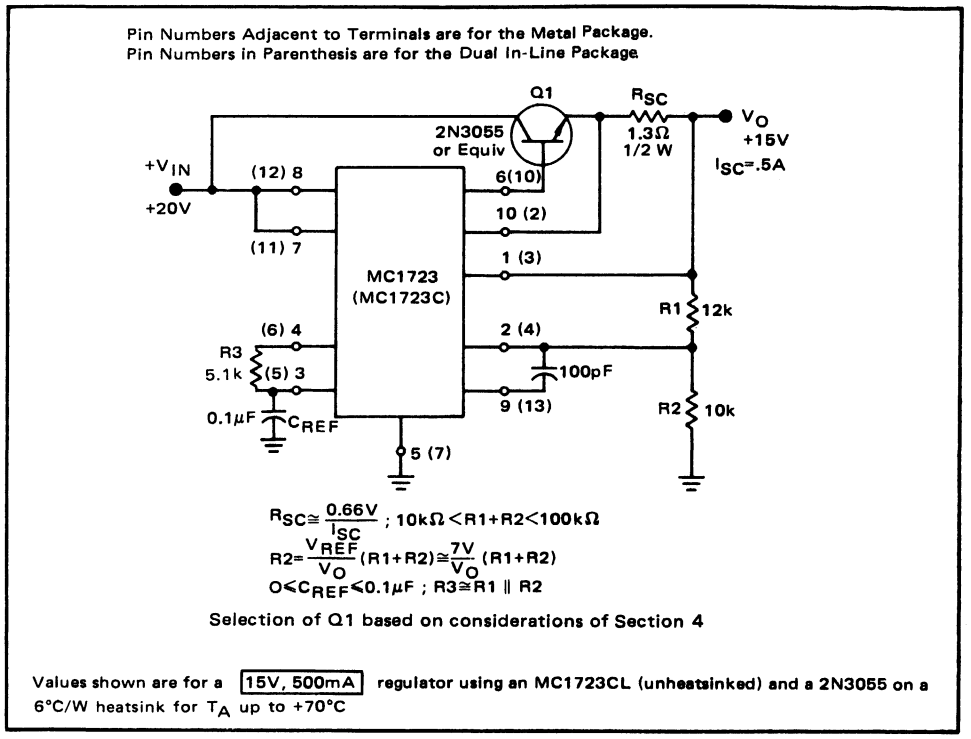


Figure 3-4A. MC1723(C) NPN Boost Configuration

3. High Efficiency Regulator Configurations

When large output currents at voltages under approximately 9 volts are desired, the configuration of Figure 3-6A can be utilized to obtain increased operating efficiency. This is accomplished by providing a separate low voltage input supply for the pass element. This method, however, usually necessitates that separate short circuit protection be provided for the IC regulator and external pass element. Figure 3-6A shows a high efficiency regulator configuration for the MC1723(C).

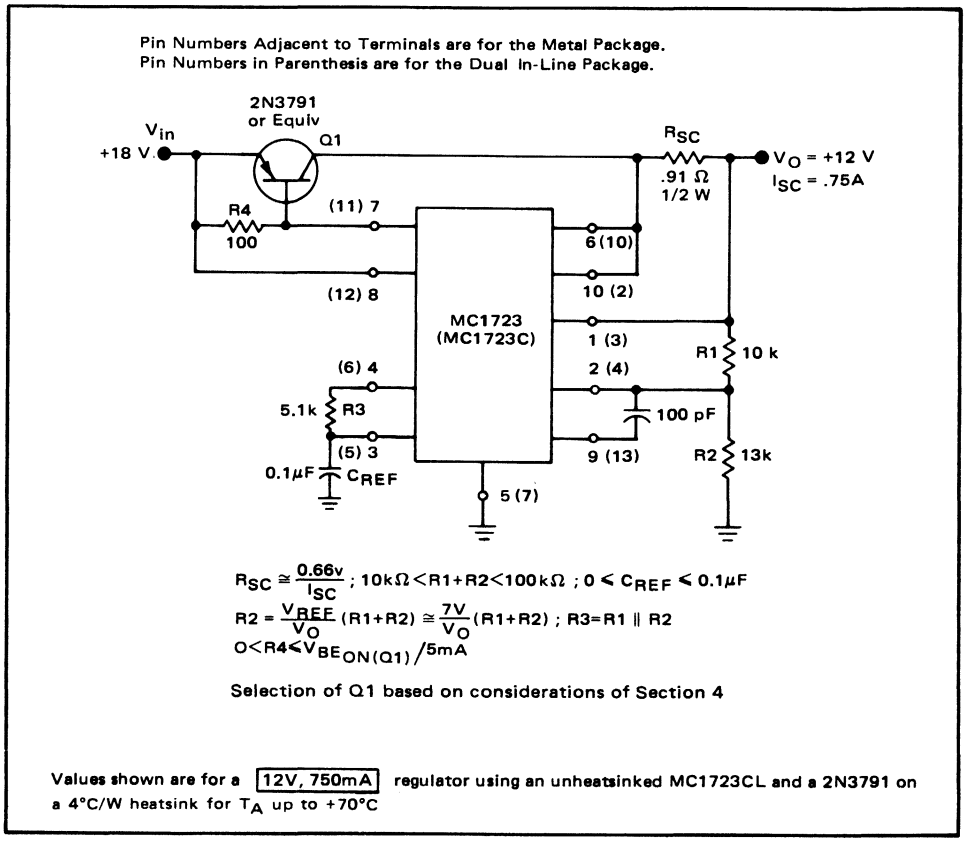


Figure 3-5A. MC1723(C) PNP Boost Configuration

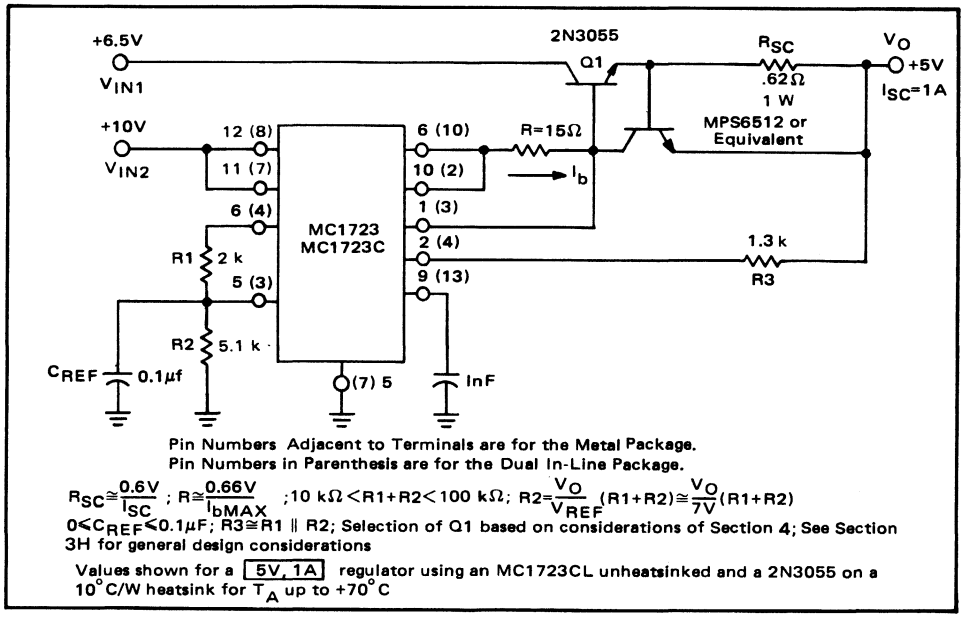


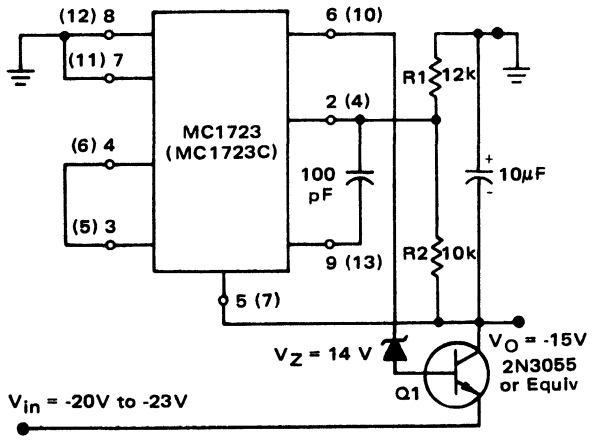
Figure 3-6A. MC1723(C) High Efficiency Regulator Configuration

B. NEGATIVE, ADJUSTABLE OUTPUT IC REGULATOR CONFIGURATIONS

1. Basic Regulator Configurations

MC1723(C)

Although a positive regulator, the MC1723(C) can be used in a negative regulator circuit configuration. This is done by using an external pass element and a zener level shifter as shown in Figure 3-1B. It should be noted that for proper operation, the input supply must not vary over a wide range, since the correct value for Vz depends directly on this voltage. In addition, it should be noted that this circuit will not operate with a shorted output.



$$|V_O| \geq 10\ V;\ 10\ k\Omega \leq R1 + R2 \leq 100\ k\Omega;\ R2 = \frac{V_{REF}}{|V_O|}(R1 + R2) \cong \frac{7\ V}{|V_O|}(R1 + R2)$$

$$V_Z \leq |V_{IN}| - V_{BE(Q1)} - 3\ V;\ V_Z \geq |V_{IN}| - |V_O| - V_{BE(Q1)} + 6\ V$$

Selection of Q1 based on considerations of Section 4

Warning: Do not short circuit output

Values shown are for a -15V, 750mA regulator using the MC1723CL with Q1 mounted on a 20°C/W heatsink at T_A up to +70°C. (DO NOT SHORT CIRCUIT OUTPUT)

Figure 3-1B. MC1723(C) Negative Regulator Configuration

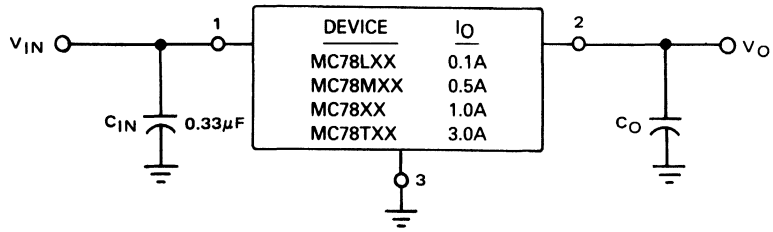
C. POSITIVE, FIXED OUTPUT IC REGULATOR CONFIGURATIONS

1. Basic Regulator Configurations

The basic current configuration for the positive three terminal regulators is shown in Figure 3-1C. Depending on which regulator type is used, this configuration can provide output currents in excess of 3A.

2. Output Current Boosting

Figure 3-2C illustrates a method for obtaining greater output currents with the three terminal positive regulators. Although any of these regulators may be used, usually it is most economical to use the 1 ampere MC7800C in this configuration.



C_{IN}: required if regulator is located more than a few (≈2" to 4") inches away from input supply capacitor; for long input leads to regulator, up to 1μF may be needed for C_{IN}. C_{IN} should be a high frequency type capacitor

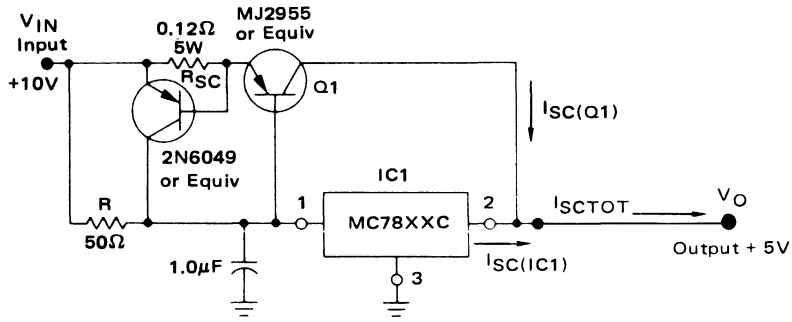
C_O: improves transient response

XX: these two digits of the type number indicate nominal output voltage.

See Section 17 for available device output voltages

See Section 15 for heatsinking

Figure 3-1C. Basic Circuit Configuration for the Positive, Fixed Output Three Terminal Regulators



XX = 2 digits of type number indicating voltage. See Section 17 for available device output voltages

R: used to divert IC regulator bias current and determines at what output current level Q1 begins conducting. $0 < R \leq \frac{V_{BEON(Q1)}}{I_{BIAS(IC1)}}$; $R_{SC} \approx \frac{0.6V}{I_{SC(Q1)}}$; $I_{SCTOT} = I_{SC(Q1)} + I_{SC(IC1)}$

Selection of Q1 based on considerations of Section 4

Values shown are for a [5V, 5A] regulator using an MC7805CK on a 2.5°C/W heatsink and Q1 on a 1°C/W heatsink for T_A up to 70°C.

Figure 3-2C. Current Boost Configuration for Positive Three Terminal Regulators

3. Obtaining an Adjustable Output Voltage

With the addition of an op amp, an adjustable output voltage supply can be obtained with the MC7805C. Regulation characteristics of the three terminal regulators are retained in this configuration, shown in Figure 3-3C. If lower output currents are required, an MC78M05C (0.5A) could be used in place of the MC7805C.

4. Current Regulator

In addition to providing voltage regulation, the three terminal positive regulators can also be used as current regulators to provide a constant current source. Figure 3-4C shows this configuration. The output current can be adjusted to any value from ≈ 8 mA (I_Q, the regulator bias current) up to the available output current of the regulator. Five volt regulators should be used to obtain the greatest output voltage compliance range for a given input voltage.

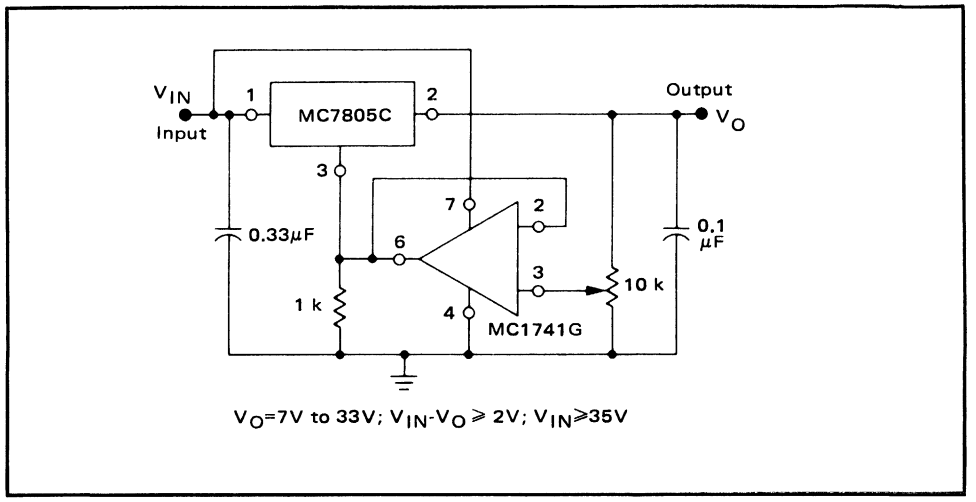


Figure 3-3C. Adjustable Ouput Voltage Configuration Using a Three Terminal Positive Regulator

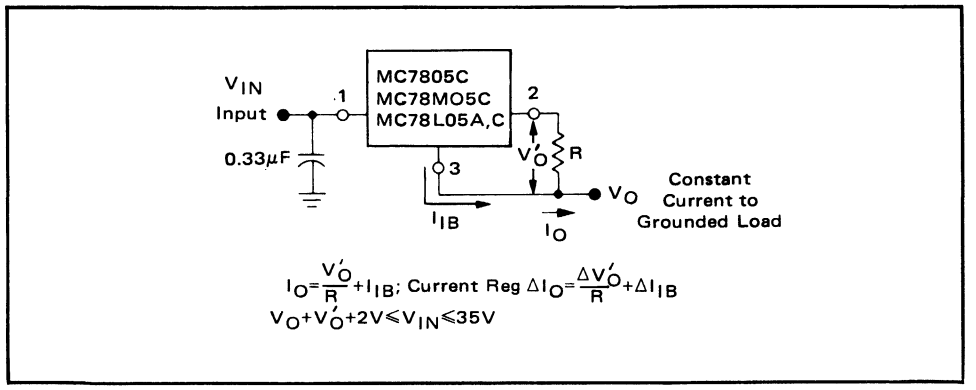


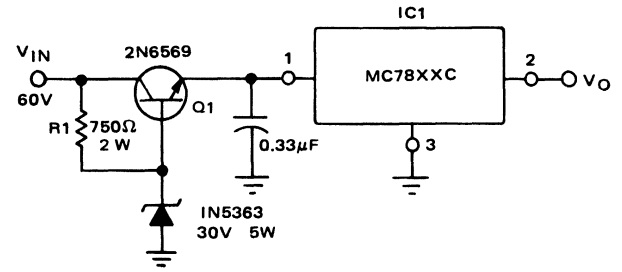
Figure 3-4C. Current Regulator Configuration

5. High Input Voltage

Occasionally, it may be necessary to power a three terminal regulator from a supply voltage greater than $V_{IN(MAX)}$ (35V or 40V). In these cases a preregulator circuit, as shown in Figure 3-5C may be used.

6. High Output Voltage

If output voltages above 24 V are desired, the circuit configuration of Figure 3-6C may be used. Zener diode Z1 sets the output voltage, while Q1, Z2, & D1 assure that the MC7824C does not have more than 30 V across it during short circuit conditions.

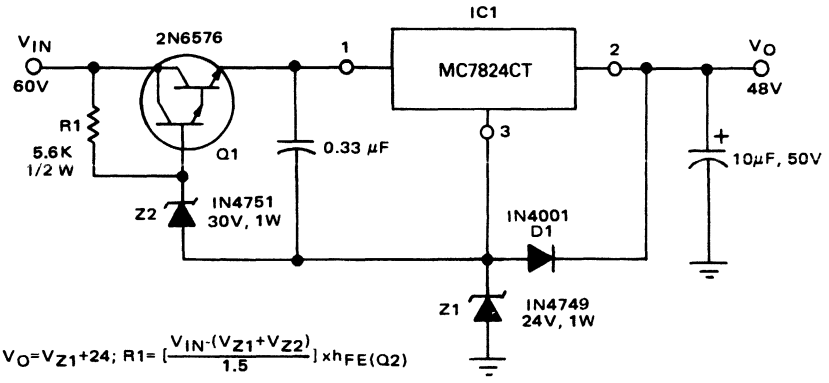


XX=2 digits of type number indicating voltage

$$R1=(\frac{V_{IN}-30}{1.5})xh_{FEQ1};\ V_{CEO_{Q1}}>V_{IN}$$

Values shown for V_{IN}=60V; Q1 should be mounted on a 2°C/W heatsink for operation at T_A up to +70°C. IC1 should be appropriately heatsinked for the package type used.

Figure 3-5C. Preregulator for Input Voltages Above V_{INMAX}



$$V_O=V_{Z1}+24;\ R1=[\frac{V_{IN}-(V_{Z1}+V_{Z2})}{1.5}]xh_{FE(Q2)}$$

Values shown are for a 48V, 1A regulator; Q1 mounted on a 10°C/W heatsink and IC1 mounted on a 2°C/W heatsink for T_A up to +70°C.

Figure 3-6C. High Output Voltage Configuration for Three Terminal Positive Regulators

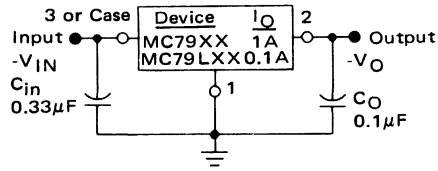
D. NEGATIVE, FIXED OUTPUT IC REGULATOR CONFIGURATIONS

1. Basic Regulator Configurations

Figure 3-1D gives the basic circuit configuration for the MC79XX and MC79LXX three terminal negative regulators.

Output Current Boosting

In order to obtain increased output current capability from the negative three terminal regulators, the current boost configuration of Figure 3-2D may be used. Currents which can be obtained with this configuration are limited only by the capabilities of the external pass transistor(s).



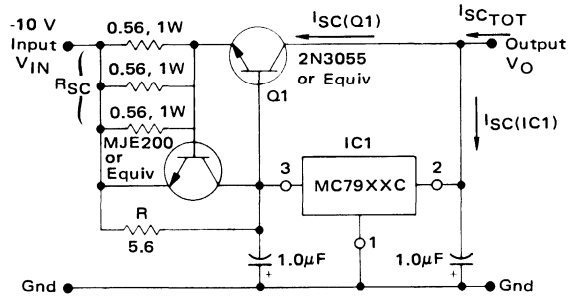
C_{IN}: required if regulator is located more than a few inches (≈2" to 4") away from input supply capacitor; for long input leads to regulator, up to 1μF may be required. C_{IN} should be a high frequency type capacitor.

C_O: improves stability and transient response

XX: these two digits of the type number indicate nominal output voltage. See Section 17 for available device output voltages

See Section 15 for heatsinking

Figure 3-1D. Basic Circuit Configuration for the Negative Three Terminal Regulators



XX= 2 digits of type number indicating output voltage. See Section 2 for voltages available

R: used to divert regulator bias current and determines at what output current level Q1 begins conducting. $0 < R \leq \frac{V_{BE\,ON(Q1)}}{I_{BIAS(IC1)}}$

$I_{SC\,TOT} = I_{SC(Q1)} + I_{SC(IC1)}$

$R_{SC} \approx \frac{0.6V}{I_{SC(Q1)}}$

Selection of Q1 based on considerations of Section 4

Values shown are for a [-5V, 4A] regulator using an MC7805CK on a 1.5°C/W heatsink with Q1 mounted on a 1°C/W heatsink for T_A up to 70°C.

Figure 3-2D. Output Current Boost Configuration for Three Terminal Negative Regulators

2. Current Regulator

The three terminal negative regulators may also be used to provide a constant current sink, as shown in Figure 3-3D. In order to obtain the greatest output voltage compliance range at a given input voltage, the MC7905 or MC79L05 should be used in this configuration.

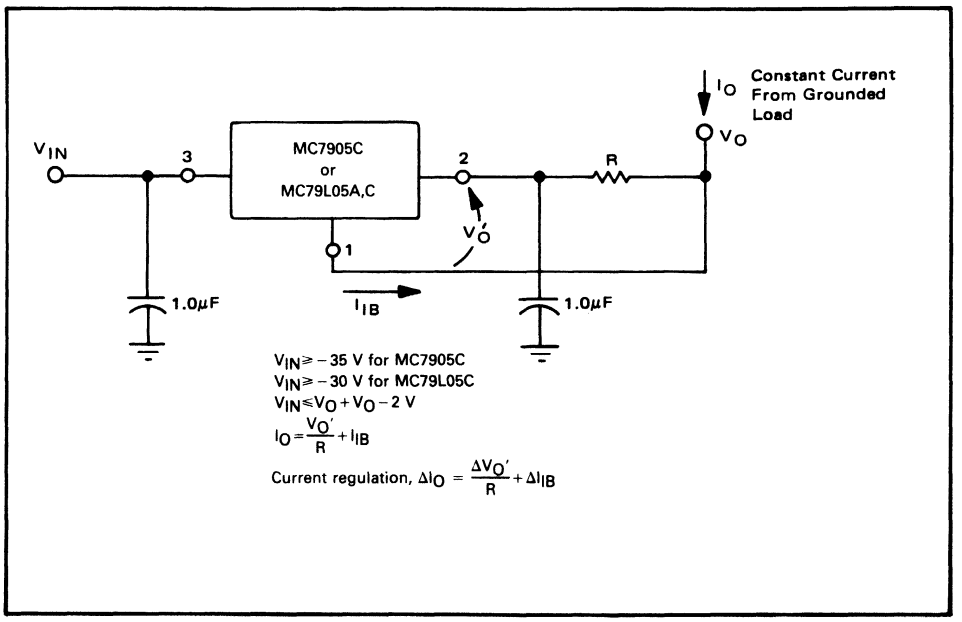


Figure 3-3D. Current Regulator Configuration for the Three Terminal Negative Regulators

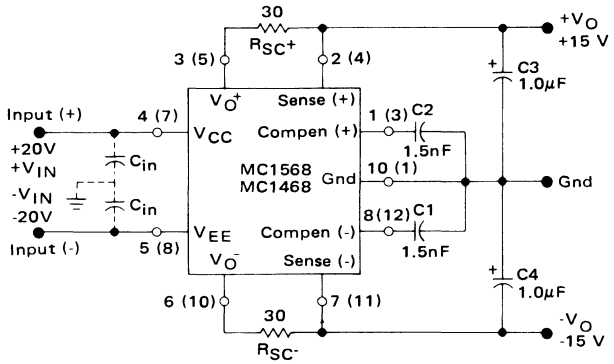
E. TRACKING IC REGULATOR CONFIGURATIONS

MC1568, MC1468

Figure 3-1E shows the basic circuit configuration for the MC1568, MC1468 Dual Tracking Regulator. The outputs of this device are internally set at ± 15V. (The output voltage can be externally adjusted with some accompanying loss of temperature performance; see device data sheet, Section 18.) This configuration is capable of providing up to ± 100mA of load current, depending on operating conditions and package style chosen. If greater output currents are desired, the current boost configuration shown in Figure 3-2E can be used.

It should be noted that in this configuration, when the positive output of the MC1568, MC1468 drops below approximately 14.5V, e.g. during a short circuit, the negative output will not drop proportionally. Instead, it collapses to ≈ 0V. This can create a latch condition, depending on the type of load.

Pin numbers adjacent to terminals are for the G suffix package. Pin numbers in parenthesis are for the L suffix package. Pin 10 is ground for the G suffix package only.



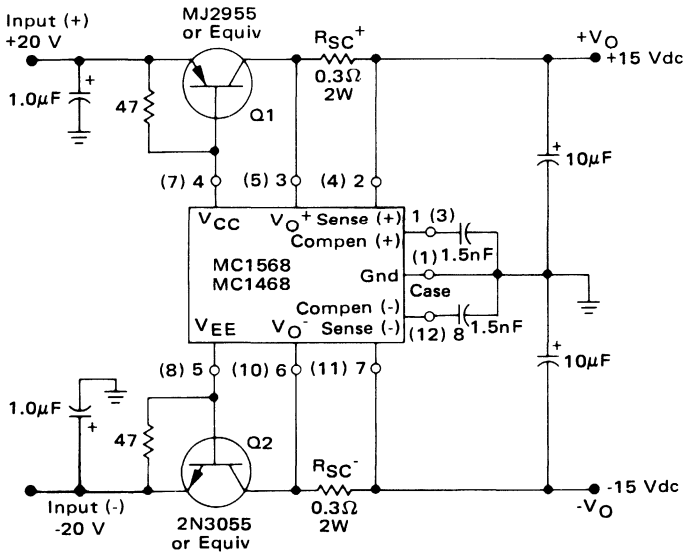
C1 and C2 should be located as close to the device as possible. A 0.1 μF ceramic capacitor (C_{in}) may be required on the input lines if the device is located an appreciable distance from the rectifier filter capacitors. C3 and C4 may be increased to improve load transient response and to reduce the output noise voltage. At low temperature operation, it may be necessary to bypass C4 with a 0.1μF ceramic disc capacitor.

$$R_{SC}^+ \cong \frac{0.6V}{I_{SC}^+} \; ; \; R_{SC}^- \cong \frac{0.6V}{I_{SC}^-}$$

Values shown are for a ±15V, 20mA regulator using an MC1468 regulator for $T_A \leq 75^\circ$ C.

Figure 3-1E. MC1568, MC1468 Basic Regulator Configuration

Pin numbers adjacent to terminals are for the G suffix package. Pin numbers in parenthesis are for the L suffix package. Pin 10 is ground for the G suffix package only.



$$R_{SC}^+ \approx \frac{0.6V}{I_{SC}^+} \; ; \; R_{SC}^- \approx \frac{0.6V}{I_{SC}^-}$$

Selection of Q1 based on considerations of Section 4

Values shown are for a ±15V, ±2A regulator using an MC1468 on a 2° C/W heatsink with Q1 & Q2 mounted on a 1° C/W heatsink for $T_A \leq 70^\circ$ C.

Figure 3-2E. MC1568, MC1468 Current Boost Configuration

F. FLOATING REGULATOR CONFIGURATIONS

If an output voltage exceeding 40 V is required, the MC1466L floating regulator can be used, as shown in Figure 3-1F. Although a standard regulator (MC1723, etc.) can be used to regulate output voltages above 40 V, by the use of level shifting techniques, the output voltage of these configurations is not adjustable over a wide range, as is the output voltage of the MC1466L. In addition, the MC1466L has several features which are not available elsewhere:

1. Output voltage adjustable to zero volts.
2. Output voltage and current capabilities limited only by choice of external series pass element.
3. Internal current limit amplifier for excellent current regulation and sharp cross-over between constant voltage and constant current regulation modes.

Note that an auxiliary supply is used to power the MC1466. This supply must be isolated from the main supply voltage since the MC1466 "floats" on the output voltage. (For a complete description of the MC1466's operation, consult its data sheet, in Section 18.)

G. GENERAL DESIGN CONSIDERATIONS

In addition to the design equations given in the regulator circuit configuration panels of Sections 3A–F, there are a few general design considerations which apply to all regulator circuits. These considerations are given below:

1. Regulator Voltages — for any circuit configuration, the worse-case voltages present on each pin of the IC regulator must be within the maximum and/or minimum limits specified on the device data sheets. These limits are instantaneous values, not averages. They include:

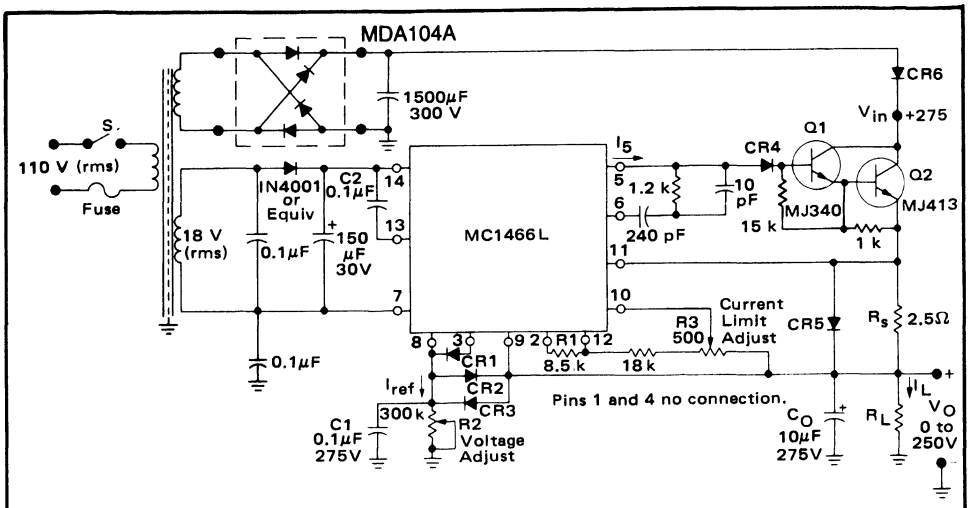
a. $V_{IN\ MIN}$
b. $V_{IN\ MAX}$
c. $(V_{IN} - V_{OUT})_{MIN}$
d. $V_{O\ MIN}$
e. $V_{O\ MAX}$

For example, the voltage between pins 8 and 5 (V_{IN}) of an MC1723CG must never fall below 9.5 V, even instantaneously, or the regulator will not function properly.

2. Regulator Power Dissipation, Junction Temperature and Safe Operating Area

The junction temperature, power dissipation output current or safe operating area limits of the IC regulator must never be exceeded.

3. Operation with a load common to a voltage of opposite polarity — In many cases, a regulator powers a load which is not connected to ground but instead is connected to a voltage source of opposite polarity (e.g. op amps, level shifting circuits, etc.). In these cases, a clamp diode should be connected to the regulator output as shown in Figure 3-1G. This protects the regulator, during startup and short-circuit operation, from output polarity reversals.



DESIGN CONSIDERATIONS

1. Constant Voltage:
   For constant voltage operation, output voltage V_O is given by:
   $V_O = (I_{ref})(R_2)$
   where R2 is the resistance from pin 8 to ground and I_{ref} is the output current of pin 3.
   The recommended value of I_{ref} is 1.0 mAdc. Resistor R1 sets the value of I_{ref}:
   $$I_{ref} = \frac{8.5}{R_1}$$
   where R1 is the resistance between pins 2 and 12.
2. Constant Current:
   For constant current operation:
   (a) Select R_S for a 250 mV drop at the maximum desired regulated output current, I_{max}.
   (b) Adjust potentiometer R3 to set constant current output at desired value between zero and I_{max}.
3. If V_{in} is greater than 20 Vdc, CR2, CR3, and CR4 are necessary to protect the MC1466 during short-circuit or transient conditions.
4. In applications where very low output noise is desired, R2 may be bypassed with C1 (0.1 μF to 2.0 μF). When R2 is bypassed, CR1 is necessary for protection during short-circuit conditions.
5. CR5 is recommended to protect the MC1466 from simultaneous pass transistor failure and output short-circuit.
6. The RC network (10 pF, 240 pF, 1.2 k ohms) is used for compensation. The values shown are valid for all applications. However, the 10 pF capacitor may be omitted if f_τ of Q1 and Q2 is greater than 0.5 MHz.
7. For remote sense applications, the positive voltage sense terminal (pin 9) is connected to the positive load terminal through a separate sense lead; and the negative sense terminal (the ground side of R2 is connected to the negative load terminal through a separate sense lead).
8. C_O may be selected by using the relationship:
   $C_O = (100\ \mu F)\ I_{L(max)}$, where $I_{L(max)}$ is the maximum load current in amperes.
9. C2 is necessary for the internal compensation of the MC1466.
10. For optimum regulation, current out of pin 5, I_5, should not exceed 0.5 mAdc. Therefore select Q1 and Q2 such that:
    $$\frac{I_{max}}{\beta_1\beta_2} \leq 0.5 \text{ mAdc}$$
    where: I_{max} = maximum short-circuit load current (mAdc)
    β_1 = minimum beta of Q1
    β_2 = minimum beta of Q2
    Although Pin 5 will source up to 1.5 mAdc, $I_5 > 0.5$ mAdc will result in a degradation in regulation.
11. CR6 is recommended when $V_O > 150$ Vdc and should be rated such that Peak Inverse Voltage > V_O.

Q1 & Q2 selected on the basis of considerations given in Section 3

Values shown are for a 0 to 250V, 100 mA regulator using an MC1466L with Q1 & Q2 mounted on a 1°C/W heatsink for $T_A \leq 70°C$.

Figure 3-1F. MC1466 Floating Regulator Configuration

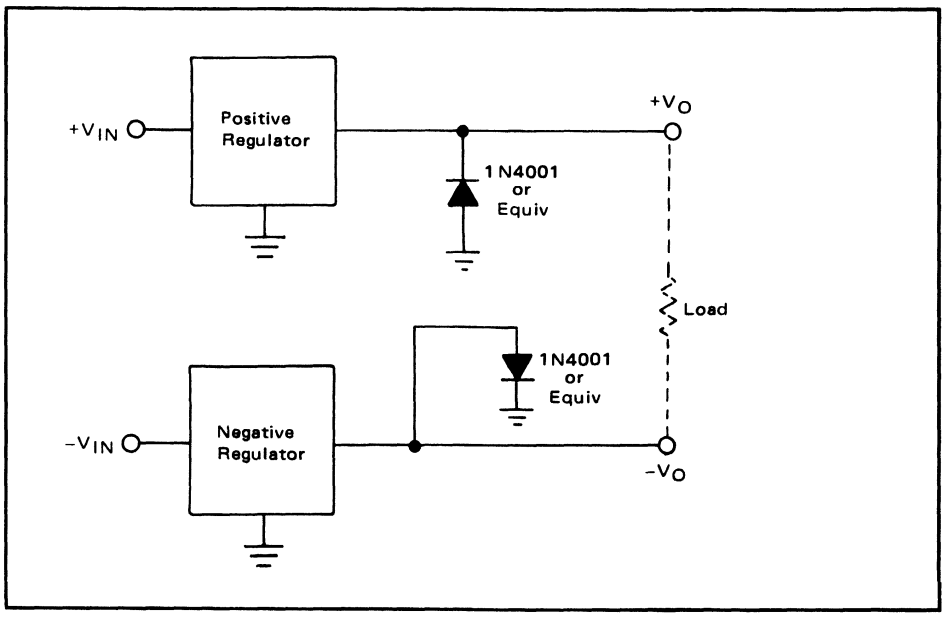


Figure 3-1G. Output Polarity Reversal Protection

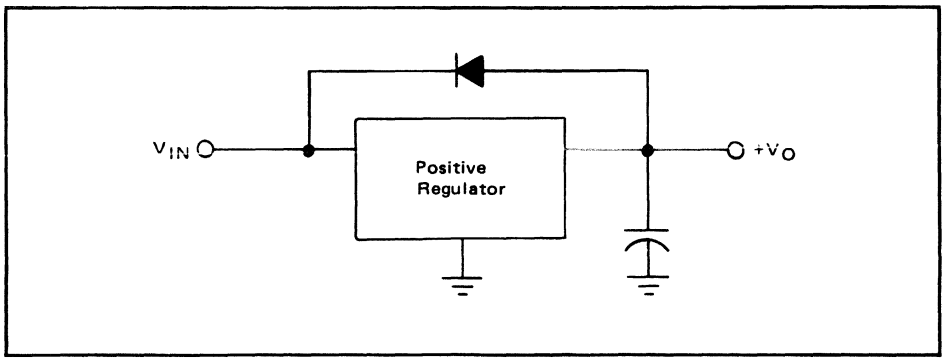


Figure 3-2G. Reverse Bias Protection

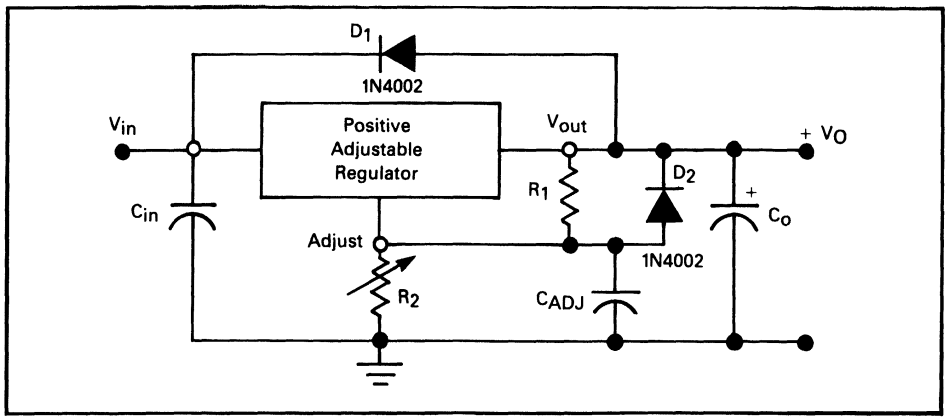


Figure 3-3G. Reverse Bias Protection for Three Terminal Adjustable Regulators

4. Reverse Bias Protection — Occasionally, there exists the possibility that the input voltage to the regulator can collapse faster than the output voltage. This could occur, for example, if the input supply is "crowbarred" during an output overvoltage condition. If the output voltage is greater $\approx$ 7 V, the emitter-base junction of the series pass element (internal or external) could break down and be damaged. To prevent this, a diode shunt can be employed, as shown in Figure 3-2G.

Figure 3-3G shows a three-terminal positive-adjustable regulator with the recommended protection diodes for output voltages in excess of 25 volts, or high-output capacitance values ($C_O > 25\ \mu F$, $C_{Adj} > 10\ \mu F$). Diode D_1 prevents C_O from discharging through the regulator during an input short-circuit. Diode D_2 protects against capacitor C_{Adj} from discharging through the regulator during an output short circuit. The combination of diodes D_1 and D_2 prevents C_{Adj} from discharging through the regulator during an input short circuit.

SECTION 4
SERIES PASS ELEMENT CONSIDERATIONS FOR LINEAR REGULATORS

Presently, most monolithic IC voltage regulators that are available have output current capabilities from 100 mA to 3.0 A. If greater current capability is required, or if the IC regulator does not possess sufficient safe-operating-area (SOA), the addition of an external series pass element is necessary.

In this section, configurations, specifications and current limit techniques for external series pass elements will be considered. For illustrative purposes, pass elements for only positive regulator types will be discussed. However, the same considerations apply for pass elements used with negative regulators.

A. SERIES PASS ELEMENT CONFIGURATIONS

Using an NPN Type Transistor

If the IC regulator has an external sense lead, an NPN type series pass element may be used, as shown in Figure 4-1A. This pass element could be a single transistor or multiple transistors arranged in darlington and/or paralleled configurations.

In this configuration, the IC regulator supplies the base current (I_B) to the pass element, Q2, which acts as a current amplifier and provides the increased output current (I_O) capability.

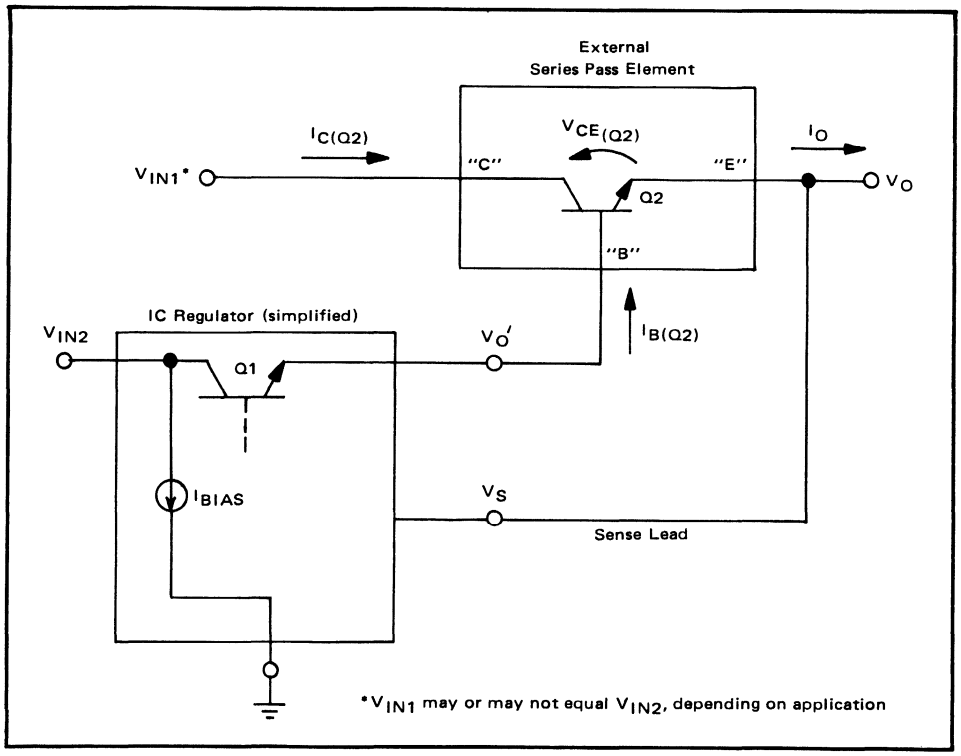


Figure 4-1A. NPN Type Series Pass Element Configuration

Using a PNP Type Transistor

If the IC regulator does not have an external sense lead, as in the case of the three terminal, fixed output regulators, the configuration of Figure 4-1B can be used. (Regulators which possess an external sense lead may also be used with this configuration.) As before, the PNP type pass element can be a single transistor or multiple transistors.

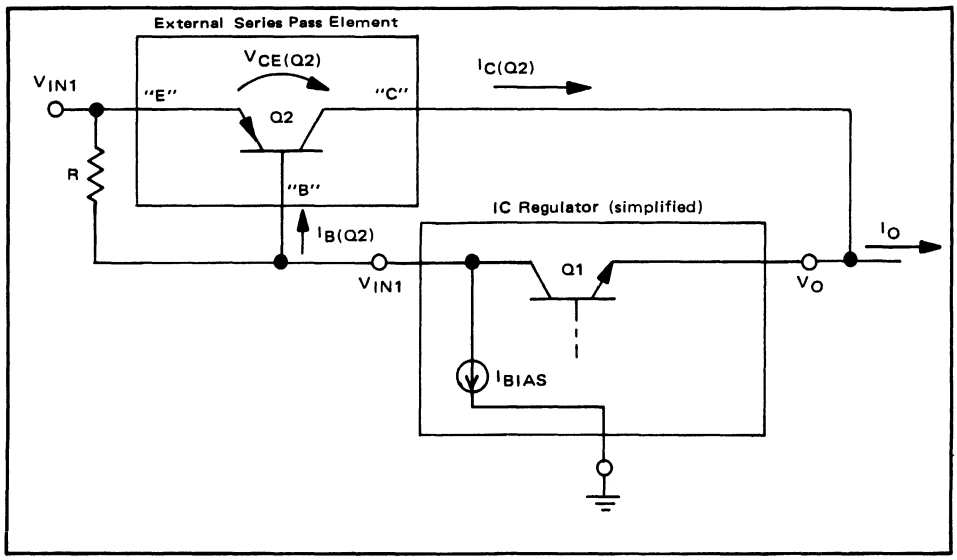


Figure 4-1B. PNP Type Series Pass Element Configuration

This configuration functions in a similar manner to that of Figure 4-1A, in that the regulator supplies base current to pass element. The resistor, R, serves to route the IC regulator bias current, I_{BIAS}, away from the base of Q2. If not included, regulation would be lost at low output currents. The value of R is low enough to prevent Q2 from turning on when I_{BIAS} flows through this resistor, and is given by:

$$0 < R \leq \frac{V_{BE\ ON}(Q2)}{I_{BIAS}} \tag{4.0}$$

B. SERIES PASS ELEMENT SPECIFICATIONS

Independent of which configuration is utilized, the transistor or transistors that compose the pass element must have adequate ratings for I_{CMAX}, V_{CEO}, h_{FE}, power dissipation, and safe-operating-area.

1. I_{CMAX} — for the pass element of Figure 4-1A, I_{CMAX} is given by:

$$I_{CMAX(Q2)} \geqslant I_{OMAX} - I_{BMAX(Q2)} = I_{OMAX} - \frac{I_{CMAX(Q2)}}{h_{FE(Q2)}} \tag{4.1}$$

$$\geqslant I_{OMAX} \tag{4.2}$$

For the configuration of Figure 4-1B:

$$I_{CMAX(Q2)} \geqslant I_{OMAX} + I_{BMAX(Q2)} \tag{4.3}$$

$$\geqslant I_{OMAX} \tag{4.4}$$

2. V_{CEO} — since $V_{CE(Q2)}$ is equal to $V_{IN1(MAX)}$ when the output is shorted or during start up:

$$V_{CEO(Q2)} \geq V_{IN1(MAX)} \tag{4.5}$$

3. hFE — the minimum DC current gain for Q2 in Figures 4-1A and 4-1B is given by:

$$h_{FEMIN(Q2)} \geq \frac{I_{CMAX(Q2)}}{I_{BMAX(Q2)}} @ V_{CE} = (V_{IN1(MIN)} - V_O) \tag{4.6}$$

4. Maximum Power Dissipation, $P_{D(MAX)}$ and Safe-Operating Area (SOA) — for any transistor there are certain combinations of I_C and V_{CE} at which it may safely be operated. When plotted on a graph, whose axes are V_{CE} and I_C, a safe-operating region is formed.

As an example, the safe-operating-area (SOA) curve for the well known 2N3055 NPN silicon power transistor is shown in Figure 4-2. The boundaries of the SOA curve are formed by the I_{CMAX}, power dissipation, second breakdown and V_{CEO} ratings of the transistor. Notice, that the power dissipation and second breakdown ratings are given for a case temperature of +25°C, and must be derated at higher case temperatures. (Derating factors may be found in the transistors' data sheets.) These boundaries must never be exceeded during operation, or destruction of the transistor or transistors which constitute the pass element may result. (In addition, the maximum operating junction temperature must not be exceeded. See Section 15.)

C. CURRENT LIMITING TECHNIQUES

In order to select a transistor or transistors with adequate SOA, the locus of pass element I_C and V_{CE} operating points must be known. This locus of points is determined by the input voltage (V_{IN}), output voltage (V_O), output current (I_O) and the type of output current limiting technique employed.

In most cases, V_{IN}, V_O, and the required output current are already known. All that is left to determine is how the chosen current limit scheme affects required pass element SOA.

NOTE: Since the external pass element is merely an extension of the IC regulator, the following discussions apply equally well to IC regulators not using an external pass element.

1. Constant Current Limiting

This method is the simplest to implement and is extensively used, especially at the lower output current levels. The basic curcuit configuration is shown in Figure 4-3A, and operates in the following manner:

As the output current increases, the voltage drop across R_{SC} increases, proportionately. When the output current has increased to the point that the voltage drop across R_{SC} is equal to the base-emitter "on" voltage of Q3 ($V_{BEON(Q3)}$), Q3 conducts. This diverts base current (I_{DRIVE}) away from Q1, the IC regulator's internal series pass element. Base drive ($I_{B(Q2)}$) of Q2 is therefore reduced and its collector-emitter voltage increases, thereby reducing the output voltage below its regulated value, V_{OUT}. The resulting output voltage-current characteristic is shown in Figure 4-3B. The value of I_{SC} is given by:

$$I_{SC} = \frac{V_{BEON(Q3)}}{R_{SC}} \tag{4.7}$$

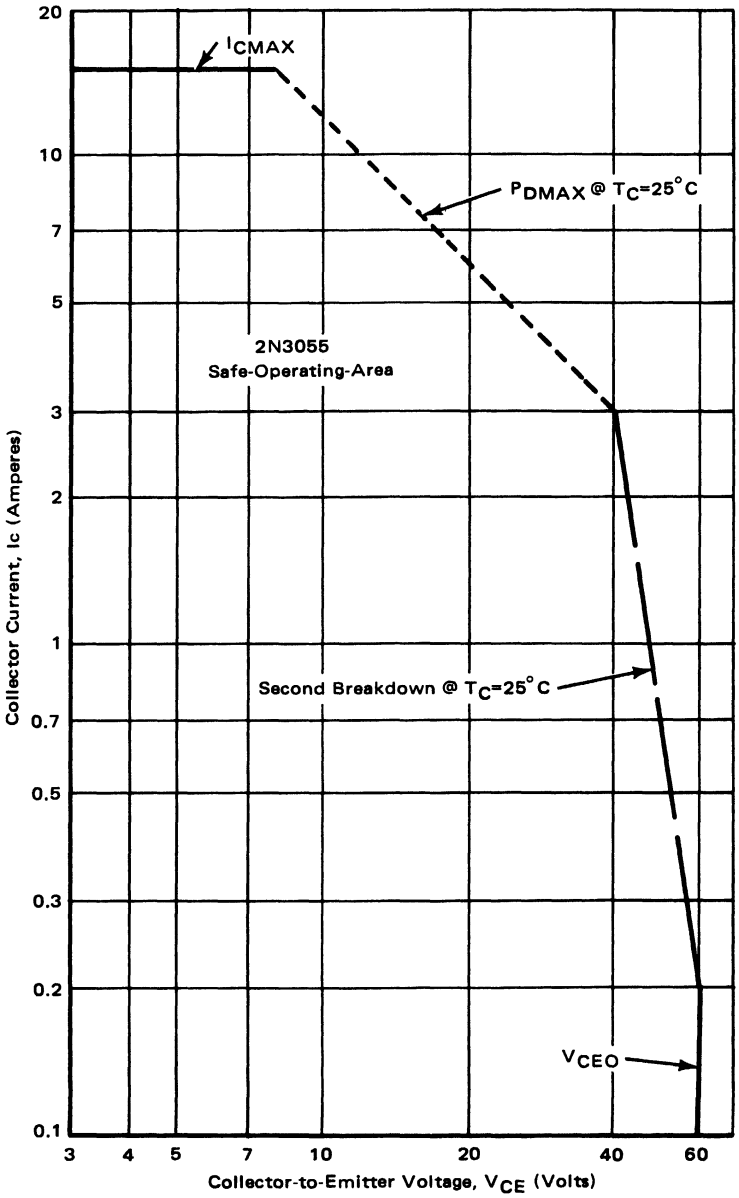


Figure 4-2. 2N3055 Safe-Operating-Area

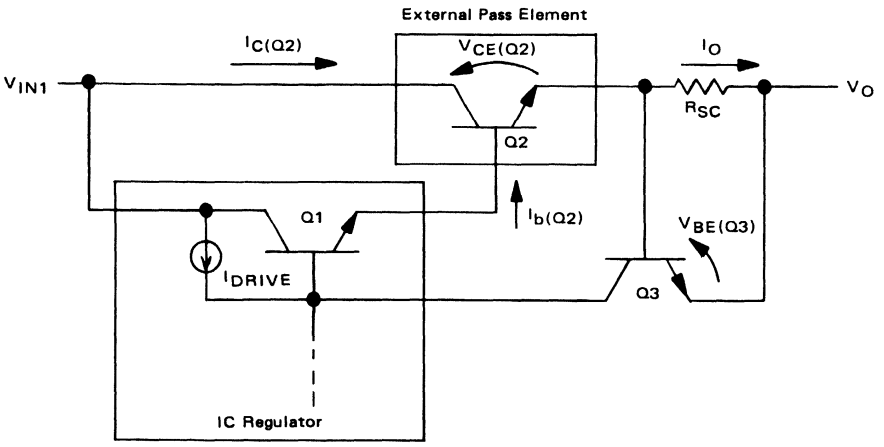


Figure 4-3A. Constant Current Limiting

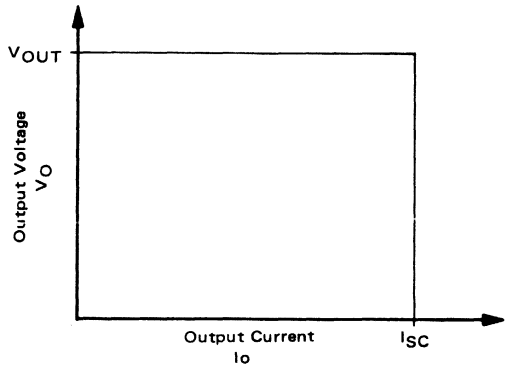


Figure 4-3B. Constant Current Limiting

By using the base of Q1 in the IC regulator as a control point, this configuration has the added benefit of limiting the IC regulator output current ($I_{B(Q2)}$) to $I_{SC}/h_{FE(Q2)}$, as well as limiting the collector current of Q2 to I_{SC}. Of course, access to this point is necessary. Fortunately, it is usually available in the form of a separate pin or as the regulator's compensation terminal.*

The required safe-operating-area for Q2 can be obtained by plotting the V_{CE} and I_C of Q2 given by:

$$V_{CE(Q2)} = V_{IN1} - V_O - I_O R_{SC} \simeq V_{IN1} - V_O \quad (4.8)$$

$$I_{C(Q2)} \simeq I_O \quad (4.9)$$

where $V_O = V_{OUT}$ for $0 \leq I_O \leq I_{SC}$ (4.10)

and $I_O = I_{SC}$ for $0 \leq V_O \leq V_{OUT}$ (4.11)

*The three terminal regulators have internal current limiting and therefore do not provide access to this point. If an external pass element is used with these regulators, constant current limiting can still be accomplished by diverting pass element drive. See Section 3 for circuit techniques.

The resulting plot is shown in Figure 4-4. The transistor chosen for Q2 must have an SOA which encloses this plot, as shown in this Figure.

Note that the greatest demand on the transistors SOA capability occurs when the output of the regulator is short circuited and the pass element must support the full input voltage and short circuit current simultaneously.

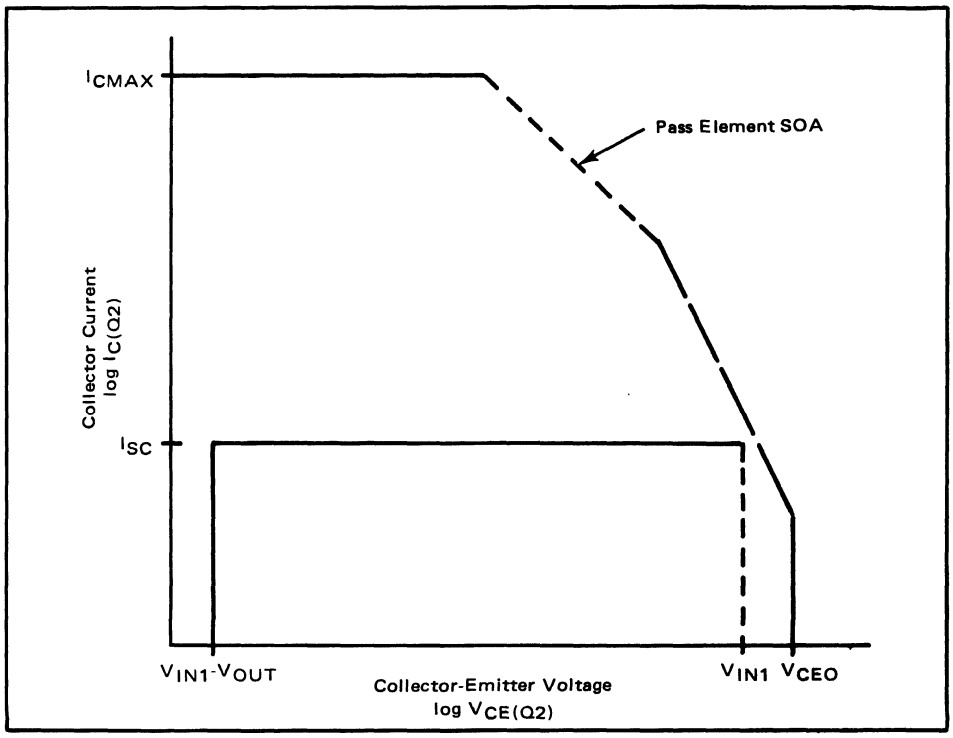


Figure 4-4. Constant Current Limit SOA Requirements

2. Foldback Current Limiting

A disadvantage of the constant current limit technique is that in order to obtain sufficient SOA the pass element must have a much greater collector current capability than is actually needed. If the short circuit current could be reduced, while still allowing full output current to be obtained during normal regulator operation, more efficient utilization of the pass elements SOA capability would result. This can be done by using a "foldback" current limiting technique instead of constant current limiting.

The basic circuit configuration for this method is shown in Figure 4-5A. The circuit operates in a manner similar to that of the constant current limiting circuit, in that output current control is obtained by diverting base drive away from Q1 with Q3.

At low output currents, V_A approximately equals V_O and V_{R2} is less than than V_O. Q3 is therefore non-conducting and the output voltage remains constant. As the output current increases, the voltage drop across R_{SC} increases until V_A and V_{R2} are great enough to bias Q3 on. The output current at which this occurs is I_K, the "knee" current.

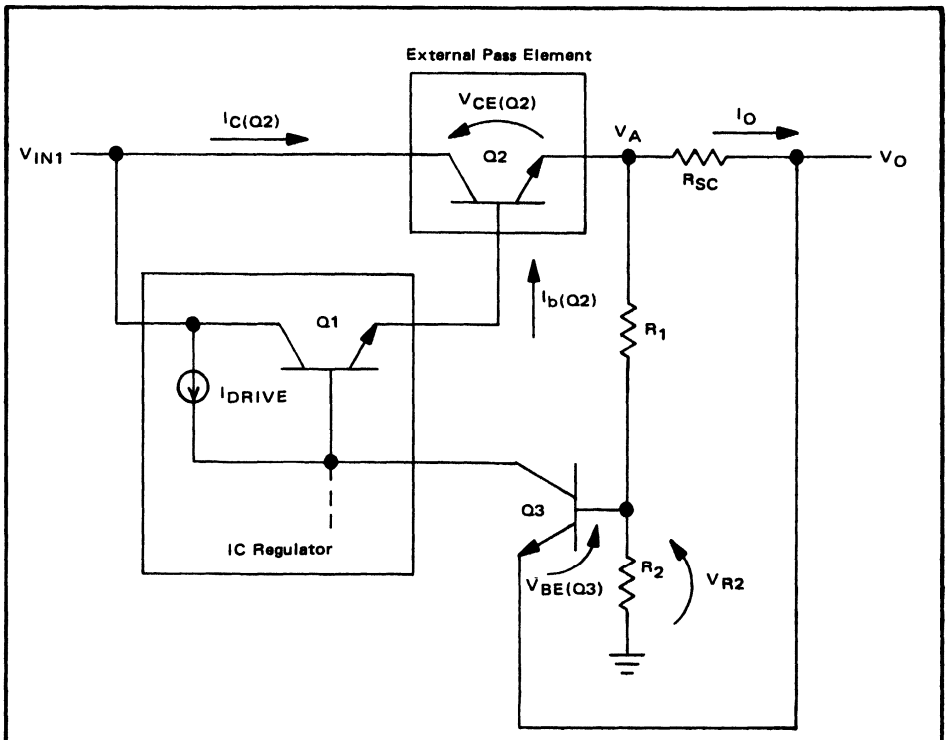


Figure 4-5A. Foldback Current Limiting

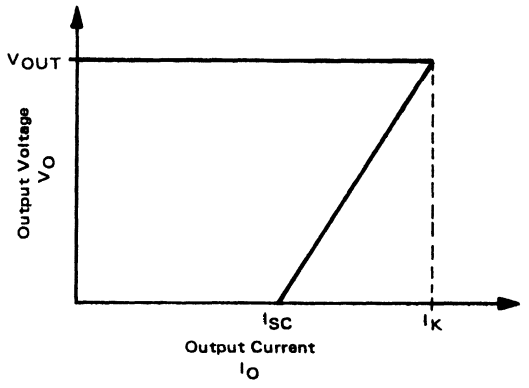


Figure 4-5B. Foldback Current Limiting

The output voltage will now decrease. Less output current is now required to keep V_A and V_{R2} at a level sufficient to bias Q3 on since the voltage at its emitter has the tendency to decrease faster than that at its base. The output current will continue to "foldback" as the output voltage decreases, until an output short circuit current level, I_{SC}, is reached when the output voltage is zero. The resulting output current-voltage characteristic is shown in Figure 4-5B. The values for R1, R2, and R_{SC} (neglecting base current of Q3) are given by:

$$R_{SC} = \frac{V_{OUT}/I_{SC}}{(1 + \frac{V_{OUT}}{V_{BEON(Q3)}}) - \frac{I_K}{I_{SC}}} \quad (4.12)$$

$$\frac{R2}{R1 + R2} = \frac{V_{BEON(Q3)}}{I_{SC} R_{SC}} \quad (4.13)$$

$$\text{and} \quad R1 + R2 \leq \frac{V_{OUT}}{I_{DRIVE}} \quad (4.14)$$

where V_{OUT} = normal regulator output voltage

I_K = knee current

I_{SC} = short circuit current

I_{DRIVE} = base drive to regulator's internal pass element(s)

A plot of Q2 operating points which result when using this technique are shown in Figure 4-6. Note that the pass element is required to operate with a collector current of only I_{SC} during short circuit conditions, not the full output current, I_K. This resuts in a more efficient utilization of the SOA of Q2 allowing the use of a smaller transistor than if constant current limiting were used. Although foldback current limiting allows use of smaller pass element transistors for a given regulator output current than does constant current limiting, it does have a few disadvantages.

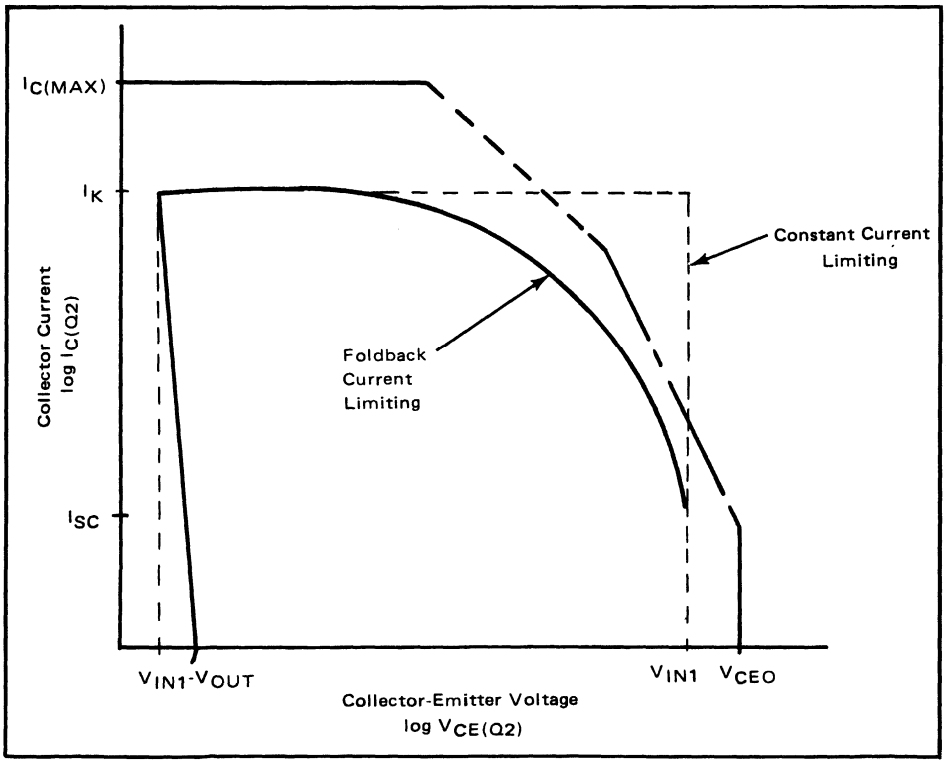


Figure 4-6. Foldback Current Limit SOA Requirements

Referring to Equation (4.12), as the foldback ratio, I_K/I_{SC}, is increased, the required value of R_{SC} increases. This results in a greater input voltage at higher foldback ratios. In addition, it can be seen for Equation (4.12) that there exists an absolute limit to the foldback ratio equal to:

$$\left(\frac{I_K}{I_{SC}}\right)_{MAX} = 1 + \frac{V_{OUT}}{V_{BEON(Q3)}} \text{ for } R_{SC} = \infty \qquad (4.15)$$

For these reasons, foldback ratios greater than 2:1 or 3:1 are not usually practical for the lower output voltage regulators.

D. PARALLELING PASS ELEMENT TRANSISTORS

Occasionally, it will not be possible to obtain a transistor with sufficient safe-operating-area. In these cases it is necessary to parallel two or more transistors. Even if a single transistor with sufficient capability is available, it is possible that paralleling two smaller transistors is more economical.

In order to insure that the collector currents of the paralleled transistors are approximately equal, the configuration of Figure 4-7 can be used. Emitter ballasting resistors are used to force collector current sharing between Q1 and Q2. The collector current mismatch can be determined by considering the following:

From Figure 4-7,

$$V_{BE1} + V_1 = V_{BE2} + V_2 \qquad (4.16)$$

and $$\Delta V_{BE} = \Delta V \qquad (4.17)$$

where $\Delta V_{BE} = V_{BE1} - V_{BE2}$

and $\Delta V = V_2 - V_1$

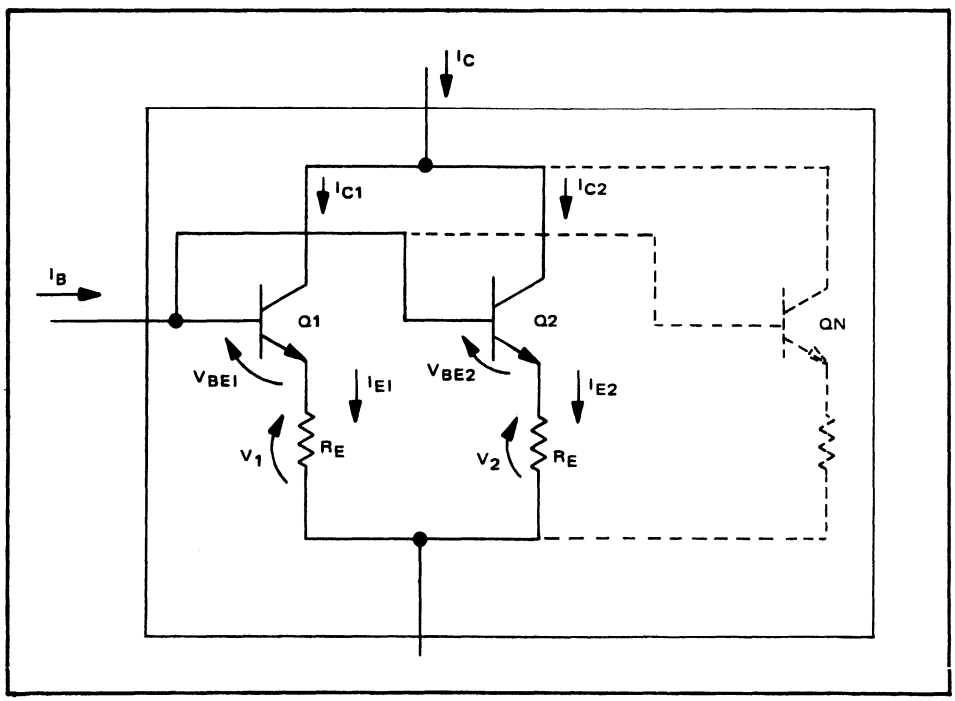


Figure 4-7. Paralleling Pass Element Transistors

Assuming $I_{E1} \simeq I_{C1}$ and $I_{E2} \simeq I_{C2}$, the collector current mismatch is given by,

$$\frac{I_{C2} - I_{C1}}{I_{C2}} = \frac{\left(\frac{V_2}{R_E}\right) - \left(\frac{V_1}{R_E}\right)}{\left(\frac{V_2}{R_E}\right)} = \frac{V_2 - V_1}{V_2} = \frac{\Delta V}{V_2} \qquad (4.18)$$

$$= \frac{\Delta V_{BE}}{V_2} \qquad (4.19)$$

and,

$$\text{percent collector current mismatch} = \frac{\Delta V_{BE}}{V_2} \times 100\% \qquad (4.20)$$

From Equation (4.20), the collector current mismatch is dependent on ΔV_{BE} and V_2. Since ΔV_{BE} is usually acceptable, V_2 should be 1.0 V to 0.5 V, respectively. R_E is therefore given by:

$$R_E = \frac{0.5 \text{ to } 1.0 \text{ V}}{I_{C1}} = \frac{0.5 \text{ V to } 1.0 \text{ V}}{I_{C2}} = \frac{0.5 \text{ V to } 1.0 \text{ V}}{I_C/2} \qquad (4.21)$$

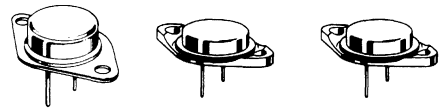
E. TRANSISTOR SELECTION GUIDE

As an aid in selecting an appropriate series pass element, the following selection guide has been included.

Selection By Package

Metal Packages

CASE 1-04, 1-06 — 40 mil pins (TO-204AA)
CASE 11-01, 11-03 — 40 mil pins (TO-204AA)
CASE 197-01 — 60 mil pins (TO-204AE TYPE)



TO-204AA/AE

I_{C}Cont Amps Max	$V_{CEO(sus)}$ Volts Min	Device Type NPN	Device Type PNP	h_{FE} Min/Max	@ I_C Amp	Resistive Switching t_s μs Max	Resistive Switching t_f μs Max	Resistive Switching @ I_C Amp	f_T MHz Min	P_D (Case) Watts @ 25°C
2.5	800	MJ8501		7.5 min	0.5	4	2	1		125
	1500*	BU205		2 min		2	0.75 typ	2	4 typ	36
		MJ12002		1.11 min	2		1	2	4 typ	75
3.5	325	2N3902		30/90	1	1.2 typ	0.1 typ	1	2.8	100
4	1500*	MJ12003		2.5 min	3		1	3		100
5	200	MJ410		30/90	1				2.5	100
	250	MJ3029		30 min	0.4		1	3		125
	300	MJ411		30/90	1				2.5	100
	400	2N6543		7/35	3	4	0.8	3	6	100
		MJ13070		8 min	3	1.5	0.5	3		125
	450	MJ16002		5 min	5	3	0.3	3		125
		MJ16004		7 min	5	2.7	0.35	3		125
		2N6834		10/30	3	2.7	0.35	3	15	125
	500	MJ16002A		5 min	5	3	0.3	3		125
	700	MJ8502		7.5 min	1	4	2	2.5		150
	800	MJ8503		7.5 min	1	4	2	2.5		150
	850*	MJ12020		5 min	5		0.13 typ	3	15	125
	1500*	BU208		2.25 min	4.5		0.6 typ	4.5	4 typ	60
		BU208A		2.25 min	4.5	8 typ	0.4 typ	4.5	4 typ	90
		BU208D†		2.25 min	4.5		0.6 typ	4.5	4 typ	60
		MJ12004		2.5 min	4.5		1	4.5	4	100

(continued)

$|h_{fe}|$ @ 1 MHz, ## Darlington
* $V_{(BR)CEX}$ or $V_{(BR)CES}$
† D Suffix on this device signifies internal C-E Diode

BIPOLAR POWER TRANSISTORS — METAL PACKAGES (continued)

TO-204AA/AE (continued)

I_CCont Amps Max	$V_{CEO(sus)}$ Volts Min	Device Type NPN	Device Type PNP	h_{FE} Min/Max	@ I_C Amp	Resistive Switching t_s μs Max	Resistive Switching t_f μs Max	Resistive Switching @ I_C Amp	f_T MHz Min	P_D (Case) Watts @ 25°C
6	100	2N5758		25/100	3	0.7 typ	0.5 typ	3	1	150
	120	2N5759		20/80	3	0.7 typ	0.5 typ	3	1	150
	140	2N5760		15/60	3	0.7 typ	0.5 typ	3	1	150
	375	BU326		30 typ	0.6	3.5	1**	2.5	6	90
	400	BU326A		30 typ	0.6	3.5	1**	2.5	6	90
7	300	MJ3041##		250 min	2.5					175
	350	MJ3042##		250 min	2.5					175
7.5	80	2N3448		40/120	5	2	0.35	5	10	115
8	60	MJ1000##	MJ900##	1k min	3					90
		2N6055##	2N6053##	750/18k	4	1.5 typ	1.5 typ	4	4#	100
	80	MJ1001##	MJ901##	1k min	3					90
		2N6056##	2N6054##	750/18k	4	1.5 typ	1.5 typ	4	4#	100
	250	2N6306		15/75	3	1.6	0.4	3	5	125
	300	2N6307		15/75	3	1.6	0.4	3	5	125
	350	2N6308		12/60	3	1.6	0.4	5	5	125
	400	2N6545		7/35	5	4	1	5	6	125
			MJ6503	15 min	2	2	0.5	4		125
		MJ13080		8 min	5	1.5	0.5	5		150
	450	MJ16006		5 min	8	2.5	0.25	5		150
		MJ16008		7 min	8	2.2	0.25	5		150
		2N6835		10/30	5	2.5	0.25	5	10	150
	500	MJ16006A		5 min	8	3	0.4	5		150
	850*	MJ12021		5 min	8		0.1 typ	5		150
	1400*	MJ10011##		20 min	4		1	4		80
	1500*	MJ12005		5 min	5		1	5		100
9	400	BUX47		7 min	6	2	0.4	6		150
	450	BUX47A		7 min	5	2	0.4	5		150
10	40	2N6383##	2N6648##	1k/20k	5				20#	100
	60	BD311	BD312	25 min	5				4	115
			2N3789	15 min	3	0.3 typ	0.4 typ	5	4	150
		2N3715	2N3791	30 min	3	0.3 typ	0.4 typ	5	4	150
		2N5877	2N5875	20/100	4	1	0.8	4	4	150
		2N6384##		1k/20k	5				20#	100
		MJ3000##	MJ2500##	1k min	5					150
	80	2N3714	2N3790	15 min	3	0.3 typ	0.4 typ	5	4	150
		2N3716	2N3792	30 min	3	0.3 typ	0.4 typ	5	4	150
		2N5878	2N5876	20/100	4	1	0.8	4	4	150
		2N6385##		1k/20k	5				20#	100
		MJ3001##	MJ2501##	1k min	5					150
	140	2N5634		15/60	5	0.9 typ	0.9 typ	5	1	150
		2N3442		20/70	4					117

* $V_{(BR)CEX}$, # $|h_{fe}|$ @ 1 MHz, ## Darlington

(continued)

JAN, JTX, JTXV Available

TO-204AA/AE (continued)

I_CCont Amps Max	$V_{CEO(sus)}$ Volts Min	Device Type NPN	Device Type PNP	h_{FE} Min/Max	@ I_C Amp	Resistive Switching t_s µs Max	Resistive Switching t_f µs Max	Resistive Switching @ I_C Amp	f_T MHz Min	P_D (Case) Watts @ 25°C
10	250	MJ15011	MJ15012	20/100	2					200
	325	BUX43		8 min	5	2.2	0.9	5	8	120
		MJ413		20/80	0.5				2.5	125
		MJ423		30/90	1				2.5	125
		MJ431		15/35	2.5				2.5	125
	350	BU323##		150 min	6	7.5 typ	5.2 typ	6		175
		MJ13014		8/20	5	2	0.5	5		150
		MJ10002##		3/300	5	2.5	1	5	10#	150
		MJ10006##		30/300	5	1.5	0.5	5	10#	150
	400	BU323A##		150 min	6	7.5 typ	5.2 typ	6		175
		MJ10007##		30/300	5	1.5	0.5	5	10#	150
		MJ10012##		100/2k	6	15	15	6		175
		MJ13015		8/20	5	2	0.5	5		150
	600	MJ10014##		10/250	10	2.5	0.8	10		175
	700	MJ8504		7.5 min	1.5	4	2	5		175
	800	MJ8505		7.5 min	1.5	4	2	5		175
		MJ16018		4 min	5	4.5 typ	0.2 typ	5		150
	950*	MJ12010		4.2 min	5		1	5		100
12	60	2N6057##	2N6050##	750/18k	6	1.6 typ	1.5 typ	6	4#	150
	80	2N6058##	2N6051##	750/18k	6	1.6 typ	1.5 typ	6	4#	150
	100	2N6059##	2N6052##	750/18k	6	1.6 typ	1.5 typ	6	4#	150
	250	BUX42		8 min	6	2	0.4	6	8	120
15	60	2N3055	MJ2955	20/70	4	0.7 typ	0.3 typ	4	2.5	115
		2N3055A	MJ2955A	20/70	4				0.8	115
		2N6576##		2k/20k	4	2	7	10	10–200#	120
		2N5881	2N5879	20/100	6	1	0.8	6	4	160
	80	2N5882	2N5880	20/100	6	1	0.8	6	4	160
	90	2N6577##		2k/20k	4	2	7	10	10-200#	120
	120	MJ15015	MJ15016	20/70	4				1	180
		2N6578##		2k/20k	4	2	7	10	10-200#	120
	140	MJ15001	MJ15002	25/150	4				2	200
	150	MJ11018##	MJ11017##	100 min	15				3#	175
	200	BUX41		8 min	8	1.5	0.4	8	8	120
		2N6249		10/50	10	3.5	1	10	2.5	175
		MJ11020##	MJ11019##	100 min	15				3#	175
	250	MJ11022##	MJ11021##	100 min	15				3#	175
	275	2N6250		8/50	10	3.5	1	10	2.5	175
	300	2N6546		6/30	10	4	0.7	10	6 to 24	175
	325	BUX13		8 min	8	2.5	0.8	8	8	150
	400	BUX48		8 min	10	2	0.4	10		175
		2N6547		6/30	10	4	0.7	10	6 to 24	175
		MJ13090		8 min	10	2.5	0.5	10		175
	450	BUX48A		8 min	8	2	0.4	10		175
		MJ16010		5 min	15	1.2 typ	0.2 typ	10		175

* $V_{(BR)CEX}$, # $|h_{fe}|$ @ 1 MHz, ## Darlington

(continued)

JAN, JTX, JTXV Available

BIPOLAR POWER TRANSISTORS — METAL PACKAGES (continued)

TO-204AA/AE (continued)

I_C Cont Amps Max	$V_{CEO(sus)}$ Volts Min	Device Type NPN	Device Type PNP	h_{FE} Min/Max	@ I_C Amp	Resistive Switching t_s μs Max	Resistive Switching t_f μs Max	Resistive Switching @ I_C Amp	f_T MHz Min	P_D (Case) Watts @ 25°C
15	450	MJ16012		7 min	15	0.9 typ	0.15 typ	10		175
		2N6836		10/30	10	3	0.35	10	10	175
	500	MJ16010A		5 min	15	3	0.4	10		175
	850*	MJ12022		5 min	15		0.1 typ	10		175
16	80	BD315	BD316	25 min	5				1	200
	100	BD317	BD318	25 min	5				1	200
		2N5629	2N6029	25/100	8	1.2 typ	1.2 typ	8	1	200
	120	2N5630	2N6030	20/80	8	1.2 typ	1.2 typ	8	1	200
	140	2N3773	2N6609	15/60	8	1.1 typ	1.5 typ	8	4	150
		2N5631	2N6031	15/60	8	1.2 typ	1.2 typ	8	1	200
	200	MJ15022	MJ15023	15/60	8				5	250
	250	MJ15024	MJ15025	15/60	8				5	250
18	160	BUX41N		8 min	12	1.2	0.25	12	8	120
20	60	2N3772		15/60	10				2	150
		2N6282##	2N6285##	750/18k	10	2.5 typ	2.5 typ	10	4#	160
	75	2N5039		20/100	10	1.5	0.5	10	60	140
	80	2N5302	2N5745	15/60	10	2	1	10	2	200
		2N6283##	2N6286##	750/18k	10	2.5 typ	2.5 typ	10	4#	160
	90	2N5038		20/100	12	1.5	0.5	12	60	140
	100	2N6284##	2N6287##	750/18k	10	2.5 typ	2.5 typ	10	4#	160
	125	BUX40		8 min	15	1	0.25	15	8	120
	140	MJ15003	MJ15004	25/150	5				2	250
	160	BUV11N		10 min	15	1.2	0.25	15	8	150
	200	BUV11		10 min	12	1.8	0.4	12	8	150
		MJ13330		8/40	10	3.5	0.7	10	5 to 40	175
	250	BUV12		10 min	10	1.5	0.5	10	8	150
		MJ13331		8/40	10	3.5	0.7	10	5 to 40	175
	350	MJ10000##		40/400	10	3	1.8	10	10#	175
		MJ10004##		40/400	10	1.5	0.5	10	10#	175
	400	BUV24		8 min	12	3	0.9	12	8	250
		MJ10001##		40/400	10	3	1.8	10	10#	175
		MJ10005##		40/400	10	1.5	0.5	10	10#	175
		MJ13333		10/60	5	4	0.7	10		175
	450	MJ10008##		30/300	10	2	0.6	10	8#	175
		MJ16014		5 min	20	2.7	0.35	20		250
		MJ16016		7 min	20	2.2	0.25	20		250
		2N6837		10/30	15	2.5	0.25	15		250
	500	MJ10009##		30/300	10	2	0.6	10	8#	175
		MJ13335		10/60	5	4	0.7	10		175
	700	BUT15##		15 min	12	2.5	0.8	12		175
	750	MJ10024##		50/600	20	5	1.8	10		250
	850	MJ10025##		50/600	20	5	1.8	10		250

* $V_{(BR)CEX}$, # $|h_{fe}|$ @ 1 MHz, ## Darlington

(continued)

JAN, JTX, JTXV Available

TO-204AA/AE (continued)

I_C Cont Amps Max	$V_{CEO(sus)}$ Volts Min	Device Type NPN	Device Type PNP	h_{FE} Min/Max	@ I_C Amp	Resistive Switching t_s µs Max	Resistive Switching t_f µs Max	Resistive Switching @ I_C Amp	f_T MHz Min	P_D (Case) Watts @ 25°C
24	1000	BUT36##		5 min	16	6	2.5	16		250
25	60	2N5885	2N5883	20/100	10	1	0.8	10	4	200
	80	2N5886	2N5884	20/100	10	1	0.8	10	4	200
			2N6436	30/120	10	1	0.25	10	40	200
	100	2N6338	2N6437	30/120	10	1	0.25	10	40	200
	120	2N6339	2N6438	30/120	10	1	0.25	10	40	200
	125	BUV10		10 min	20	1.2	0.25	20	8	150
		BUV10N		10 min	20	1.55	0.45	15	10	175
	140	2N6340		30/120	10	1	0.25	10	40	200
	150	2N6341		30/120	10	1	0.25	10	40	200
	500	BUT14##		15 min	16	2.8	0.8	16		175
28	400	BUT13##		20 min	20	2.6	0.8	18		175
30	40	2N3771		15/60	15				2	150
		2N5301	2N4398	15/60	15	2	1	10	2	200
	60	2N6302	2N4399	15/60	15	2	1	10	2	200
		MJ11012##	MJ11011##	1k min	20				4#	200
	90	BUX39		8 min	20	1	0.25	20	8	120
		MJ11014##	MJ11013##	1k min	20				4#	200
	100	2N6328		6/30	30				3	200
		MJ802	MJ4502	25/100	7.5				2	200
	120	MJ11016##	MJ11015##	1k min	20				4#	200
	325	BUV23•		8 min	16	1.8	0.4	16	8	250
	400	BUS98•		8 min	20	2.3	0.4	20		250
		BUX98				3	0.8	20		250
	450	BUS98A•		8 min	16	2.3	0.4	16		250
		BUX98A				3	0.8	16		250
		MJ16020•		5 min	30	1.8	0.2	20		250
		MJ16022•		7 min	30	1.5	0.15	20		250
40	160	BUV21N•		10 min	40	1	0.2	40	8	250
	200	BUV21•		10 min	25	1.8	0.4	25	8	150
	250	BUS52•		15 min	40					350
		BUV22•		10 min	20	1.1	0.35	20	8	250
	350	MJ10022•##		50/600	120	2.5	0.9	20		250
	400	MJ10023•##		50/600	10	2.5	0.9	20		250
	700	BUT35•##		15 min	24	4	1.2	24		250
50	60	2N5685•	2N5883•	15/60	25	0.5 typ	0.3 typ	25	2	300
		MJ11028•##	MJ11029•##	400 min	50					300
	80	2N5686•	2N5884•	15/60	25	0.5 typ	0.3 typ	25	2	300
			2N6377•	30/120	20	0.8	0.25	20	30	250
	90	MJ11030•##	MJ11031•##	400 min	50					300
	100	2N6274•	2N6378•	30/120	20	0.8	0.25	20	30	250
	120	2N6275•	2N6379•	30/120	20	0.8	0.25	20	30	250
		MJ11032•##	MJ11033•##	400 min	50					300
	125	BUV20•		10 min	50	1.2	0.25	50	8	250
	150	2N6277•		30/120	20	0.8	0.25	20	30	250

JAN, JTX, JTXV Available

• Modified TO-3, 60 mil pins, # $|h_{fe}|$ @ 1 MHz, ## Darlington

(continued)

BIPOLAR POWER TRANSISTORS — METAL PACKAGES (continued)

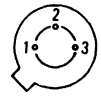
TO-204AA/AE (continued)

I_CCont Amps Max	$V_{CEO(sus)}$ Volts Min	Device Type NPN	Device Type PNP	h_{FE} Min/Max	@ I_C Amp	Resistive Switching t_s µs Max	Resistive Switching t_f µs Max	Resistive Switching @ I_C Amp	f_T MHz Min	P_D (Case) Watts @ 25°C
50	200	BUS51•		15 min	50					350
	400	MJ10015•##		10 min	40	2.5	1	20		250
	500	BUT34•## MJ10016•##		15 min 10 min	32 40	3 2.5	1.5 1	32 20		250 250
56	400	BUT33•##		20 min	36	3.3	1.6	36		250
60	60	MJ14000•	MJ14001•	15/100	50					300
	80	MJ14002•	MJ14003•	15/100	50					300
	200	MJ10020•##		75 min	15	3.5	0.5	30		250
	250	MJ10021•##		75 min	15	3.5	0.5	30		250
70	125	BUS50•		15 min	50					350

• Modified TO-3, 60 mil pins, # $|h_{fe}|$ @ 1 MHz, ## Darlington

TO-205AA (Formerly TO-5)


CASE 31-03



PIN 1. EMITTER
2. BASE
3. COLLECTOR

I_CCont Amps Max	$V_{CEO(sus)}$ Volts Min	Device Type NPN	Device Type PNP	h_{FE} Min/Max	@ I_C Amp	Resistive Switching t_s µs Max	Resistive Switching t_f µs Max	Resistive Switching @ I_C Amp	f_T MHz Min	P_D (Case) Watts @ 25°C
3	40		2N3719	25/180	1	0.4*		1	60	6
			2N3867	40/200	1.5	0.4*		1.5	60	6
	60		2N3720	25/180	1	0.4*		1	60	6
			2N3868	30/150	1.5	0.4*		1.5	60	6
	80		2N6303	30/150	1.5	0.4*		1.5	60	6

*t_{off}

TO-205AD (Formerly TO-39)

CASE 79-02

PIN 1. EMITTER
2. BASE
3. COLLECTOR
(Pin 3 connected to case)

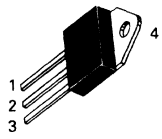
I_CCont Amps Max	$V_{CEO(sus)}$ Volts Min	Device Type NPN	Device Type PNP	h_{FE} Min/Max	@ I_C Amp	Resistive Switching t_s µs Max	Resistive Switching t_f µs Max	Resistive Switching @ I_C Amp	f_T MHz Min	P_D (Case) Watts @ 25°C
0.5	300		MJ4646	20 min	0.5	0.72*		0.05	40	5
	400		MJ4647	20 min	0.5	0.72*		0.05	30	5
4	60	2N4877		20/100	4	1.5	0.5	4	4	10
5	80	2N5336	2N6190	30/120	2	2	0.2	2	30	6
		2N5337	2N6191	60/240	2	2	0.2	2	30	6
	100	2N5338		30/120	2	2	0.2	2	30	10
		2N5339	2N6193	60/240	2	2	0.2	2	30	6

*t_{off}

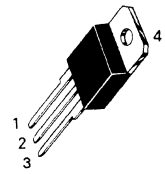
JAN, JTX, JTXV Available

Bipolar Power Transistors

Plastic Packages
TO-218AC



STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR



STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

CASE 340-02 (TO-218AC) CASE 340D-01 (TO-218)

I_CCont Amps Max	$V_{CEO(sus)}$ Volts Min	Device Type NPN	Device Type PNP	h_{FE} Min/Max	@ I_C Amp	Resistive Switching t_s μs Max	Resistive Switching t_f μs Max	Resistive Switching @ I_C Amp	f_T MHz Min	P_D (Case) Watts @ 25°C
3	750	MJH16032		4 min	3	2	1.5	2		125
	850	MJH16034		4 min	3	2	1.5	2		125
5	400	BUW11		6 min	3	4	0.8	3		125
	450	BUW11A		6 min	2.5	4	0.8	2.5		125
		MJH16002		5 min	5	3	0.3	3		100
		MJH16004		7 min	5	2.7	0.35	3		100
	500	MJH16002A		5 min	5	3	0.3	3		100
	1500*	MJH12004		2.5 min	4.5	—	1	4.5	4	100
6	375	BU426†		30 typ	0.6	2 typ	0.5 typ	2.5	6 typ	113
	400	BU426A†		30 typ	0.6	2 typ	0.5 typ	2.5	6 typ	113
8	400	BUW12		6 min	6	4	0.8	5		125
	450	BUW12A		6 min	5	4	0.8	5		125
		MJH16006		5 min	8	2.5	0.25	5		125
		MJH16008		7 min	8	2.2	0.25	5		125
	500	BUT50P##†		30 min	2	0.75 typ	0.1 typ	5		100
		MJH16006A		5 min	8	2.5	0.25	5		125
	700	BU508,A		2.25 min	4.5	8 typ	0.5 typ	4.5	7	125
		BU508D,AD		2.25 min	4.5	8 typ	0.5 typ	4.5	7	125
	750	MJH12005					0.4 typ	5	4	100
9	400	BUV47†		7 min	5	2	0.4	6		128
	450	BUV47A†		7 min	6	2	0.4	6		128
10	40	TIP33	TIP34	20 min	3				3	80
	60	BDV65##†	BDV64##†	1k min	5					125
		TIP33A	TIP34A	20 min	3				3	80
		TIP140##	TIP145##	500 min	10	2.5 typ	2.5 typ	5	4#	125
	80	BDV65A##†	BDV64A##†	1k min	5					125
		TIP33B	TIP34B	20 min	3				3	80
		TIP141##	TIP146##	500 min	10	2.5 typ	2.5 typ	5	4#	125
	100	BDV65B##†	BDV64B##†	1k min	5					125
		TIP33C	TIP34C	20 min	3				3	80
		TIP142##	TIP147##	500 min	10	2.5 typ	2.5 typ	5	4#	125
	120	BDV65C##†	BDV64C##†	1k min	5					125
	200	BU323P##†		150 min	6	15	15	6		125
	250	BU323AP##†		150 min	6	15	15	6		125
	400	MJH10012##		100/2k	6	15	15	6		118
	800	MJH16018		4 min	5	4.5 typ	0.2 typ	5		150
15	60	TIP3055	TIP2955	5 min	10				2.5	80
	150	MJH11018##	MJH11017##	400/15k	10				3#	150
	200	MJH11020##	MJH11019##	400/15k	10				3#	150
	250	MJH11022##	MJH11021##	400/15k	10				3#	150

(continued)

$|h_{fe}|$ @ 1 MHz, ## Darlington
* $V_{(BR)CEX}$ or $V_{(BR)CES}$
† These devices supplied in Case 340D-01. Consult Motorola for details.

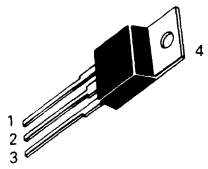
PLASTIC TO-218 (continued)

I_C Cont Amps Max	$V_{CEO(sus)}$ Volts Min	Device Type NPN	Device Type PNP	h_{FE} Min/Max	@ I_C Amp	Resistive Switching t_s μs Max	Resistive Switching t_f μs Max	Resistive Switching @ I_C Amp	f_T MHz Min	P_D (Case) Watts @ 25°C
15	400	BUV48†		8 min	10	2	0.4	10		150
		MJH13090		8 min	10	2.5	0.5	10		125
	450	BUV48A†		8 min	8	2	0.4	10		150
		MJH16010		5 min	15	1.2	0.2	10		150
		MJH16012		7 min	15	0.9	0.15	10		150
	500	BUT51P##†		40 min	5	1.1	0.16	10		125
		MJH16010A		5 min	15	3	0.4	10		150
16	100	MJE4340	MJE4350	15 min	8	1.2 typ	1.2 typ	8	1	125
	120	MJE4341	MJE4351	15 min	8	1.2 typ	1.2 typ	8	1	125
	140	MJE4342	MJE4352	15 min	8	1.2 typ	1.2 typ	8	1	125
	160	MJE4343	MJE4353	15 min	8	1.2 typ	1.2 typ	8	1	125
20	60	MJH6282##	MJH6285##	750/18k	10				4#	125
	80	MJH6283##	MJH6286##	750/18k	10				4#	125
	100	MJH6284##	MJH6287##	750/18k	10				4#	125
25	40	TIP35	TIP36	10/75	15	0.6 typ	0.3 typ	10	3	125
	45	BD249†	BD250†	10 min	15				3	125
	60	BD249A†	BD250A†	10 min	15				3	125
		TIP35A	TIP36A	10/75	15	0.6 typ	0.3 typ	10	3	125
	80	BD249B†	BD250B†	10 min	15				3	125
		TIP35B	TIP36B	10/75	15	0.6 typ	0.3 typ	10	3	125
	100	BD249C†	BD250C†	10 min	15				3	125
		TIP35C	TIP36C	10/75	15	0.6 typ	0.3 typ	10	3	125

$|h_{fe}|$ @ 1 MHz, ## Darlington
† These devices supplied in Case 340D-01. Consult Motorola for details.

PLASTIC TO-220

STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR



CASE 221A-04 (TO-220AB)

I_C Cont Amps Max	$V_{CEO(sus)}$ Volts Min	Device Type NPN	Device Type PNP	h_{FE} Min/Max	@ I_C Amp	Resistive Switching t_s μs Max	Resistive Switching t_f μs Max	Resistive Switching @ I_C Amp	f_T MHz Min	P_D (Case) Watts @ 25°C
0.5	350	MJE2360T		15 min	0.1				10 typ	30
		MJE2361T		40 min	0.1				10 typ	30
1	40	TIP29	TIP30	15/75	1	0.6 typ	0.3 typ	1	3	30
	60	TIP29A	TIP30A	15/75	1	0.6 typ	0.3 typ	1	3	30
	80	TIP29B	TIP30B	15/75	1	0.6 typ	0.3 typ	1	3	30
	100	TIP29C	TIP30C	15/75	1	0.6 typ	0.3 typ	1	3	30
	250	TIP47		30/150	0.3	2 typ	0.18 typ	0.3	10	40
	300	TIP48		30/150	0.3	2 typ	0.18 typ	0.3	10	40
	350	TIP49		30/150	0.3	2 typ	0.18 typ	0.3	10	40
	400	TIP50		30/150	0.3	2 typ	0.18 typ	0.3	10	40

BIPOLAR POWER TRANSISTORS — PLASTIC PACKAGES (continued)
PLASTIC TO-220 (continued)

I_CCont Amps Max	$V_{CEO(sus)}$ Volts Min	Device Type NPN	Device Type PNP	h_{FE} Min/Max	@ I_C Amp	Resistive Switching t_s µs Max	Resistive Switching t_f µs Max	Resistive Switching @ I_C Amp	f_T MHz Min	P_D (Case) Watts @ 25°C
2	45	BD239	BD240	15 min	1				3	30
	60	BD239A TIP110##	BD240A TIP115##	15 min 500 min	1 2	1.7 typ	1.3 typ	2	3 25#	30 50
	80	BD239B TIP111##	BD240B TIP116##	15 min 500 min	1 2	1.7 typ	1.3 typ	2	3 25#	30 50
	100	BD239C TIP112##	BD240C TIP117##	25 min 500 min	1 2	1.7 typ	1.3 typ	2	3 25#	30 50
	400	BUX84		30 min	0.1	3.5	1.4	1	4	50
	450	BUX85		30 min	0.1	3.5	1.4	1	4	50
	900	MJE1320		3 min	1	4 typ	0.8 typ	1		80
2.5	700	MJE8500		7.5 min	0.5	4	2	1		65
	750	MJE12007		1.1 min	2		1	2	4 typ	65
	800	MJE8501		7.5 min	0.5	4	2	1		65
3	40	TIP31	TIP32	25 min	1	0.6 typ	0.3 typ	1	3	40
	45	BD241	BD242	25 min	1				3	40
	60	BD241A TIP31A	BD242A TIP32A	25 min 25 min	1 1	0.6 typ	0.3 typ	1	3 3	40 40
	80	BD241B TIP31B	BD242B TIP32B	25 min 25 min	1 1	0.6 typ	0.3 typ	1	3 3	40 40
	100	BD241C TIP31C	BD242C TIP32C	25 min 25 min	1 1	0.6 typ	0.3 typ	1	3 3	40 40
	750	MJE16032		4 min	3	2	1.5	2		80
	850	MJE16034		4 min	3	2	1.5	2		80
4	45	2N6121 BD533	2N6124 BD534	25/100 25 min	1.5 2	0.4 typ	0.3 typ	1.5	2.5 3	40 50
	60	2N6122 BD535 MJE800T##	2N6125 BD536 MJE700T##	25/100 25 min 750 min	1.5 2 1.5	0.4 typ	0.3 typ	1.5	2.5 3 1#	40 50 40
	80	2N6123 BD537	 BD538	20/80 15 min	1.5 2	0.4 typ	0.3 typ	1.5	2.5 3	40 50
	300	MJE13004		6/30	3	3	0.7	3	4	60
	400	MJE13005		6/30	3	3	0.7	3	4	60
5	60	TIP120##	TIP125##	1k min	3	1.5 typ	1.5 typ	3	4#	65
	80	TIP121##	TIP126##	1k min	3	1.5 typ	1.5 typ	3	4#	65
	100	TIP122##	TIP127##	1k min	3	1.5 typ	1.5 typ	4	4#	75
	250	2N6497		10/75	2.5	1.8	0.8	2.5	5	80
	300	2N6498		10/75	2.5	1.8	0.8	2.5	5	80
	400	MJE13070		8 min	3	1.5	0.5	3		80
	450	BUS46P MJE16002 MJE16004		7 min 5 min 7 min	3 5 5	1.5 3 2.7	0.5 0.3 0.35	2 3 3		75 80 80
	700	MJE8502		7.5 min	1	4	2	2.5		80
	800	MJE8503		7.5 min	1	4	2	2.5		80
6	40	TIP41	TIP42	15/75	3	0.4 typ	0.15 typ	3	3	65
	45	BD243	BD244	15 min	3				3	65
	60	BD243A TIP41A	BD244A TIP42A	15 min 15/75	3 3	0.4 typ	0.15 typ	3	3 3	65 65
	80	BD243B TIP41B	BD244B TIP42B	15 min 15/75	3 3	0.4 typ	0.15 typ	3	3 3	65 65
	100	BD243C TIP41C	BD244C TIP42C	15 min 15/75	3 3	0.4 typ	0.15 typ	3	3 3	65 65
7	30	2N6288	2N6111	30/150	3	0.4 typ	0.15 typ	3	4	40

$|h_{fe}|$ @ 1 MHz, ## Darlington

(continued)

PLASTIC TO-220 (continued)

I_C Cont Amps Max	$V_{CEO(sus)}$ Volts Min	Device Type NPN	Device Type PNP	h_{FE} Min/Max	@ I_C Amp	Resistive Switching t_s μs Max	Resistive Switching t_f μs Max	Resistive Switching @ I_C Amp	f_T MHz Min	P_D (Case) Watts @ 25°C
7	45	BD795	BD796	25 min	3				3	65
	50	2N6290	2N6109	30/150	2.5	0.4 typ	0.15 typ	3	4	40
	60	BD797	BD798	25 min	3				3	65
	70	2N6292	2N6107	30/150	3	0.4 typ	0.15 typ	3	4	40
	80	BD799	BD800	15 min	3				3	65
	100	BD801	BD802	15 min	3				3	65
	150	BU407,D		30 min	1.5		0.75	5	10	60
	200	BU406,D		30 min	1.5		0.75	5	10	60
	375	BU522##		250 min	2.5				7.5	75
	425	BU522A##		250 min	2.5				7.5	75
	450	BU522B##		250 min	2.5				7.5	75
8	40	2N6386##		1k/20k	3				20#	65
	45	BDX53##	BDX54##	750 min	3				4#	60
		BD895##	BD896##	750 min	3				1#	70
		BD895A##	BD896A##	750 min	4				1#	70
	60	2N6043##	2N6040##	1k/10k	4	1.5 typ	1.5 typ	3	4#	75
		BDX53A##	BDX54A##	750 min	3				4#	60
		BD897##	BD898##	750 min	3				1#	70
		BD897A##	BD898A##	750 min	4				1#	70
		TIP100##	TIP105##	1k/20k	3	1.5 typ	1.5 typ	3	4#	80
	80	2N6044##	2N6041##	1k/10k	4	1.5 typ	1.5 typ	3	4#	75
		BDX53B##	BDX54B##	750 min	3				4#	60
		BD899##	BD900##	750 min	3				1#	70
		BD899A##	BD900A##	750 min	4				1#	70
		TIP101##	TIP106##	1k/20k	3	1.5 typ	1.5 typ	3	4#	80
	100	2N6045##	2N6042##	1k/10k	3	1.5 typ	1.5 typ	3	4#	75
		BDX53C##	BDX54C##	750 min	3				4#	60
		BD901##	BD902##	750 min	3				1#	70
		TIP102##	TIP107##	1k/20k	3	1.5 typ	1.5 typ	3	4#	80
	120	BDX53D##	BDX54D##	750 min	3				4#	60
		MJE15028	MJE15029	20 min	4				30	50
	150	MJE15030	MJE15031	20 min	4				30	50
		BU807##		100 min	5	0.55 typ	0.2 typ	5		60
	200	BU806##		100 min	5	0.55 typ	0.2 typ	5		60
	300	MJE13006		5/30	5	3	0.7	5	4	80
		MJE5740##		200 min	4	8 typ	2 typ	6		80
			MJE5850	15 min	2	2	0.5	4		80
	350	MJE5741##		200 min	4	8 typ	2 typ	6		80
			MJE5851	15 min	2	2	0.5	4		80
	400	MJE5742##		200 min	4	8 typ	2 typ	6		80
		MJE13007		5/30	5	3	0.7	5	4	80
			MJE5852	15 min	2	2	0.5	4		80
		MJE16080		5 min	8	2	0.5	5		80
	450	MJE16081		5 min	8	2	0.5	5		80
10	30		D45H1	20 min	4					50
			D45H2	40 min	4					50
	40	D44E1##		1000 min	5	2 typ	0.5 typ	10		50
	45	BDX33##	BDX34##	750 min	4				3	70
		BD805	BD806	15 min	4				1.5	90
			D45H4	20 min	4					50
		D44H5	D45H5	40 min	4					50
	60	BDX33A##	BDX34A##	750 min	4				3	70
		BD807	BD808	15 min	4				1.5	90

$|h_{fe}|$ @ 1 MHz, ## Darlington

(continued)

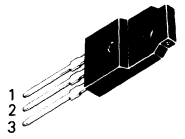
BIPOLAR POWER TRANSISTORS — PLASTIC PACKAGES (continued)

PLASTIC TO-220 (continued)

I_CCont Amps Max	$V_{CEO(sus)}$ Volts Min	Device Type NPN	Device Type PNP	h_{FE} Min/Max	@ I_C Amp	Resistive Switching t_s μs Max	Resistive Switching t_f μs Max	Resistive Switching @ I_C Amp	f_T MHz Min	P_D (Case) Watts @ 25°C
10	60	D44H7	D45H7	20 min	4					50
		D44H8	D45H8	40 min	4					50
			D45H9	40 min	4					50
		MJE2801T		25/100	3					75
		MJE3055T	MJE2955T	20/70	4					75
		2N6387##	2N6667##	1k/20k	5				20#	65
		SE9300##	SE9400##	1k min	4				1#	70
	80	BDX33B##	BDX34B##	750 min	3				3	70
		BD809	BD810	15 min	4				1.5	90
		D44E3		1000 min	5	2 typ	0.5 typ	10		50
			D45H12	40 min	4					50
		2N6388##	2N6668##	1k/20k	5				20#	65
		D44H10	D45H10	20 min	4	0.5 typ	0.14 typ	5	50 typ	50
		D44H11	D45H11	40 min	4	0.5 typ	0.14 typ	5	50 typ	50
		SE9301##	SE9401##	1k min	4				1#	70
	100	BDX33C##	BDX34C##	750 min	3				3	70
		SE9302##	SE9402##	1k min	4				1#	70
12	300	MJE13008		6/30	8	3	0.7	8	4	100
	400	MJE13009		6/30	8	3	0.7	8	4	100
15	30	D44VH1	D45VH1	20 min	4	0.7	0.09	8	50 typ	83
	40	2N6486	2N6489	20/150	5	0.6 typ	0.3 typ	5	5	75
	45	D44VH4	D45VH4	20 min	4	0.5	0.09	8	50 typ	83
	60	2N6487	2N6490	20/150	5	0.6 typ	0.3 typ	5	5	75
		D44VH7		20 min	4	0.5	0.09	8	50 typ	83
		MJE5220	MJE5230	20 min	4	0.7	0.1	8		83
	80	2N6488	2N6491	20/150	5	0.6 typ	0.3 typ	5	5	75
		D44VH10	D45VH10	20 min	4	0.5	0.09	8	50 typ	83
		MJE5221	MJE5231	20 min	4	0.7	0.1	8		83

$|h_{fe}|$ @ 1 MHz, ## Darlington

PLASTIC Full Pak (TO-220 Type)



CASE 221C-02

I_CCont Amps Max	$V_{CEO(sus)}$ Volts Min	Device Type NPN	Device Type PNP	h_{FE} Min/Max	@ I_C Amp	Resistive Switching t_s μs Max	Resistive Switching t_f μs Max	Resistive Switching @ I_C Amp	f_T MHz Min	P_D (Case) Watts @ 25°C
1	250	MJF47		30/150	0.3	2 typ	0.17 typ	0.3	10	28
5	100	MJF122##	MJF127##	2000 min	3	1.5 typ	1.5 typ	3	4#	28
8	80		MJF6107	30/90	2	0.5 typ	0.13 typ	2	4	35
	100	MJF102##	MJF107##	3000 min	3	1.5 typ	1.5 typ	3	4#	35
	150	MJF15030	MJF15031	40 min	3	1 typ	0.15 typ	3	30	35
10	60	MJF3055	MJF2955	20/100	4				2	40

$|h_{fe}|$ @ 1 MHz, ## Darlington

SECTION 5
LINEAR REGULATOR CONSTRUCTION AND LAYOUT

An important, and often neglected, aspect of the total regulator circuit design is the actual layout and component placement of the circuit. In order to obtain excellent transient response performance, high frequency transistors are used in modern integrated circuit voltage regulators. Proper attention to circuit layout is therefore necessary in order to prevent regulator instability or oscillations, or degraded performance.

In this section, guidelines will be given on proper regulator layout and placement of circuit components. In addition, topics such as remote voltage sensing and semiconductor mounting techniques will also be considered.

1. General Layout and Component Placement Considerations

As mentioned previously, modern integrated circuit regulators are necessarily high bandwidth devices in order to obtain good transient response characteristics. To insure stable closed loop operation, all these devices are frequency compensated, either internally or externally. This compensation can easily be upset by unwanted stray circuit capacitances and lead inductances, resulting in spurious oscillations. Therefore, it is important that the circuit lead lengths be short and the layout as tight as possible. Particular attention should be paid to locating the compensation and bypass capacitors as close to the IC as possible. Lead lengths associated with the external pass element(s), if used, should also be minimized.

Often overlooked is the stray inductance associated with the input leads to the regulator circuit. If the lead length from the input supply filter capacitor to the regulator input is more than a couple of inches, a 0.01-1.0μF high frequency type capacitor (tantalum, ceramic, etc.) should be used to bypass the supply leads close to the regulator input pins.

2. Ground Loops and Remote Voltage Sensing

Ground Loops

Regulator performance can also suffer if ground loops in the circuit wiring are not avoided. The most common ground loop problem occurs when the return lead of the input supply filter capacitor is improperly located, as shown in Figure 5-1. If this return lead is physically connected between the load return and the regulator circuit ground point (''B''), a ripple voltage component (60 or 120 Hz) can be induced on the load voltage, V_L. This is due to the high peaks of the filter capacitor ripple current, i_{ripple}, flowing through the lead resistance between the load and regulator. These peaks can be 5 to 15 times the value of load current. Since the regulator will only keep constant the voltage between its sense lead and ground point, points ''A'' and ''B'' in Figure 5-1, this additional ripple voltage, V_{LEAD}, will appear at the load.

This problem can be avoided by proper placement and connection of the filter capacitor return load as shown in Figure 5-2.

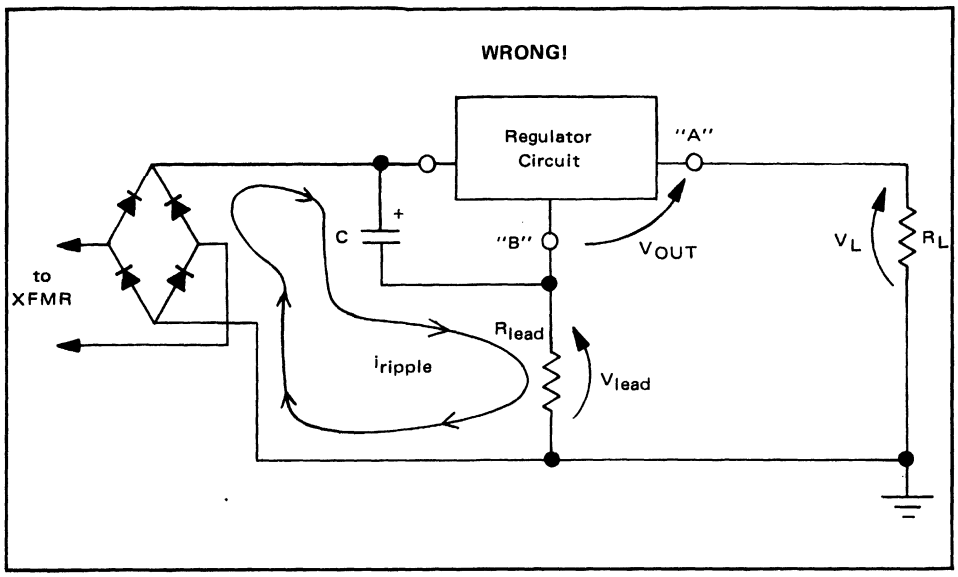


Figure 5-1. Filter Capacitor Ground Loop

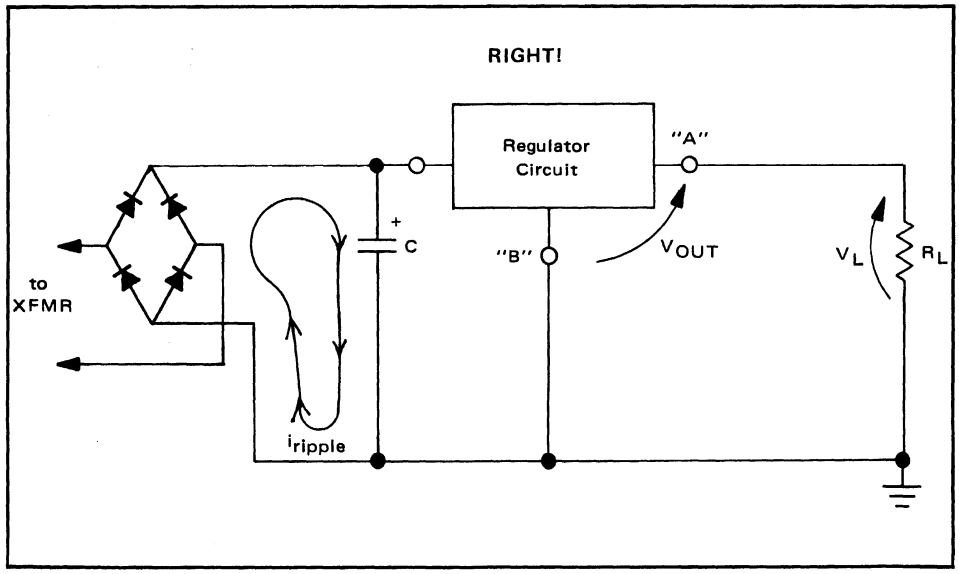


Figure 5-2.

Remote Voltage Sensing

Closely related to the above ground loop problem, is resistance in the current carrying leads to the load. This can cause poorer than expected load regulation in cases where the load currents are large or where the load is located some distance from the regulator. This is illustrated in Figure 5-3. As stated previously, the regulator circuit will keep the voltage present between its sense and ground pins constant. From Figure 5-3 we can see that any lead resistance between these points and the load will cause the load voltage, V_L, to vary with varying load current, i_L. This effectively lowers the load regulation of the circuit.

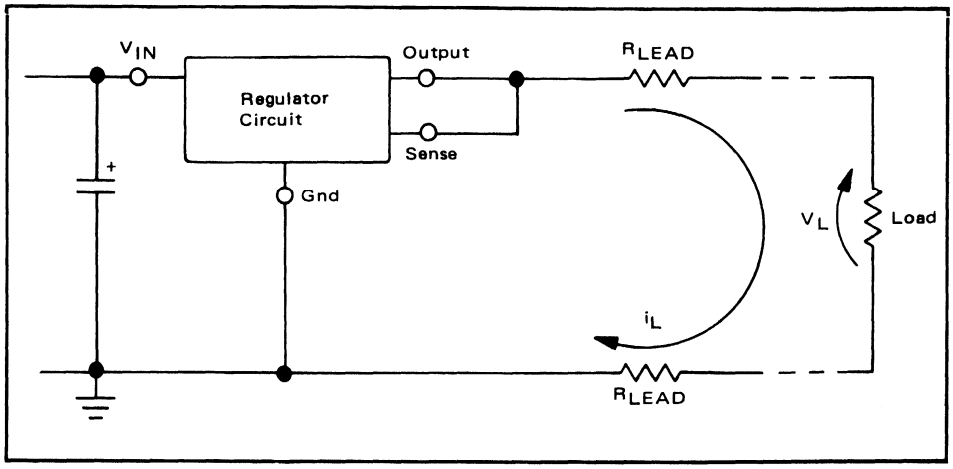


Figure 5-3. Effects of Resistance in Output Leads

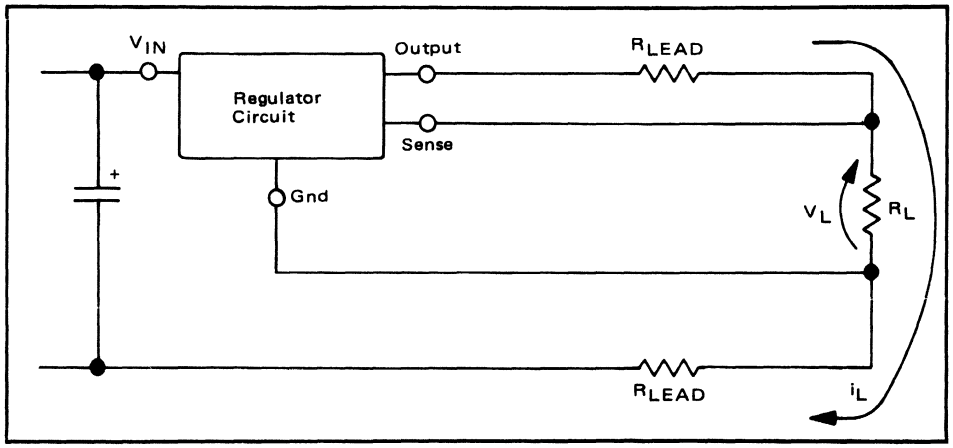


Figure 5-4. Remote Voltage Sensing

This problem can be avoided by use of remote sense leads, as shown in Figure 5-4. The voltage drops in the high current carrying leads now have no effect on the load voltage, V_L. However, since the sense and ground leads are usually rather long, care must be exercised that their associated lead inductance is minimized, or loop instability may result. The ground and sense leads should be formed into a twisted pair lead to minimize their lead industance and noise pickup.

3. Mounting Considerations for Power Semiconductors

Current and power ratings of semiconductors are inseparably linked to their thermal environment. Except for lead-mounted parts used at low currents, a heat exchanger is required to prevent the junction temperature from exceeding its rated limit, thereby running the risk of a high failure rate. Furthermore, the semiconductor industry's field history indicated that the failure rate of most silicon semiconductors decreases approximately by one-half for a decrease in junction

temperature from 160°C to 135°C.[1] Guidelines for designers of military power supplies impose a 110°C limit upon junction temperature.[2] Proper mounting minimizes the temperature gradient between the semiconductor case and the heat exchanger.

Most early life field failures of power semiconductors can be traced to faulty mounting procedures. With metal packaged devices, faulty mounting generally causes unnecessarily high junction temperature, resulting in reduced component lifetime, although mechanical damage has occurred on occasion from improperly mounting to a warped surface. With the widespread use of various plastic-packaged semiconductors, the prospect of mechanical damage is very significant. Mechanical damage can impair the case moisture resistance or crack the semiconductor die.

Figure 5-5 shows an example of doing nearly everything wrong. A tab mount TO-220 package is shown being used as a replacement for a TO-213AA (TO-66) part which was socket mounted. To use the socket, the leads are bent — an operation which, if not properly done, can crack the package, break the internal

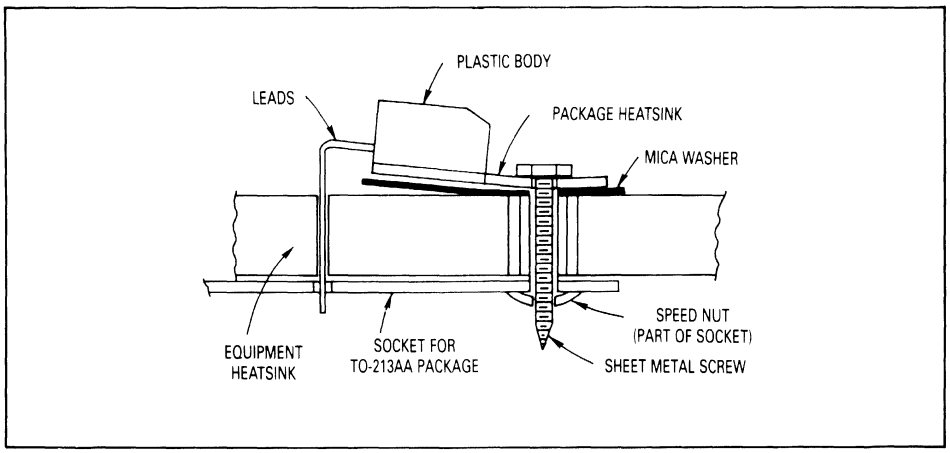


Figure 5-5. Extreme Case of Improperly Mounting A Semiconductor (Distortion Exaggerated)

(1) MIL-HANDBOOK — 2178, SECTION 2.2.
(2) "Navy Power Supply Reliability — Design and Manufacturing Guidelines" NAVMAT P4855-1, Dec. 1982 NAVPUBFORCEN, 5801 Tabor Ave., Philadelphia, PA 19120.

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bonding wires, or crack the die. The package is fastened with a sheet-metal screw through a 1/4″ hole containing a fiber-insulating sleeve. The force used to tighten the screw tends to pull the package into the hole, possibly causing enough distortion to crack the die. In addition the contact area is small because of the area consumed by the large hole and the bowing of the package; the result is a much higher junction temperature than expected. If a rough heatsink surface and/or burrs around the hole were displayed in the illustration, most but not all poor mounting practices would be covered.

In many situations the case of the semiconductor must be electrically isolated from its mounting surface. The isolation material is, to some extent, a thermal isolator as well, which raises junction operating temperatures. In addition, the possibility of arc-over problems is introduced if high voltages are present. Various regulating agencies also impose creepage distance specifications which further complicates design. Electrical isolation thus places additional demands upon the mounting procedure.

Proper mounting procedures usually necessitate orderly attention to the following:

1. Preparing the mounting surface
2. Applying a thermal grease (if required)
3. Installing the insulator (if electrical isolation is desired)
4. Fastening the assembly
5. Connecting the terminals to the circuit

In this note, mounting procedures are discussed in general terms for several generic classes of packages. As newer packages are developed, it is probable that they will fit into the generic classes discussed in this note. Unique requirements are given on data sheets pertaining to the particular package. The following classes are defined:

Flange Mount
Plastic Body Mount
Tab Mount
Surface Mount

Appendix A contains a brief review of thermal resistance concepts. Appendix B discusses measurement difficulties with interface thermal resistance tests.

Mounting Surface Preparation

In general, the heatsink mounting surface should have a flatness and finish comparable to that of the semiconductor package. In lower power applications, the heatsink surface is satisfactory if it appears flat against a straight edge and is free from deep scratches. In high-power applications, a more detailed examination of the surface is required. Mounting holes and surface treatment must also be considered.

Surface Flatness

Surface flatness is determined by comparing the variance in height (Δh) of the test specimen to that of a reference standard as indicated in Figure 5-6. Flatness is normally specified as a fraction of the Total Indicator Reading (TIR). The mounting surface flatness, i.e, Δh/TIR, if less than 4 mils per inch, normal for extruded aluminum, is satisfactory in most cases.

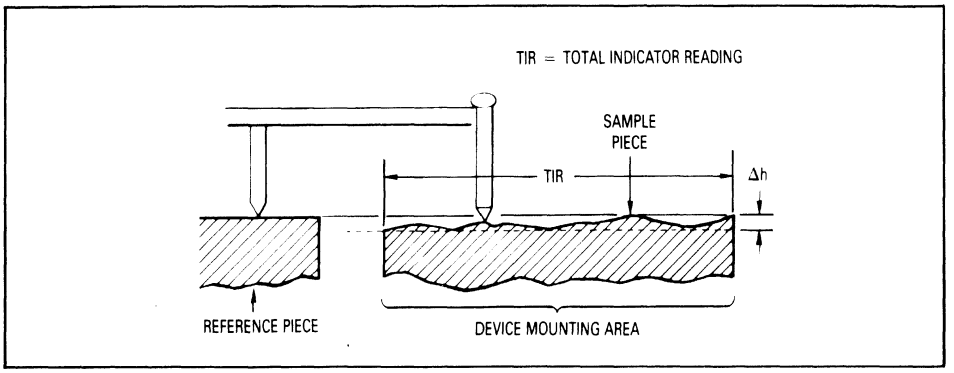

Figure 5-6. Surface Flatness Measurement

Surface Finish

Surface finish is the average of the deviations both above and below the mean value of surface height. For minimum interface resistance, a finish in the range of 50 to 60 microinches is satisfactory; a finer finish is costly to achieve and does not significantly lower contact resistance. Tests conducted by Thermalloy using a copper TO-204 (TO-3) package with a typical 32-microinch finish, showed that heatsink finishes between 16 and 64 μ-in caused less than $\pm 2.5\%$ difference in interface thermal resistance when the voids and scratches were filled with a thermal joint compound.[3] Most commercially available cast or extruded heatsinks will require spotfacing when used in high-power applications. In general, milled or machined surfaces are satisfactory if prepared with tools in good working condition.

Mounting Holes

Mounting holes generally should only be large enough to allow clearance of the fastener. The larger thick flange type packages having mounting holes removed from the semiconductor die location, such as the TO-204AA, may successfully be used with larger holes to accommodate an insulating bushing, but many plastic encapsulated packages are intolerant of this condition. For these packages, a smaller screw size must be used such that the hole for the bushing does not exceed the hole in the package.

Punched mounting holes have been a source of trouble because if not properly done, the area around a punched hole is depressed in the process. This "crater"

(3) Catalog #87-HS-9 (1987), page 8, Thermalloy, Inc., P.O. Box 810839, Dallas, Texas 75381-0839.

in the heatsink around the mounting hole can cause two problems. The device can be damaged by distortion of the package as the mounting pressure attempts to conform it to the shape of the heatsink indentation, or the device may only bridge the crater and leave a significant percentage of its heat-dissipating surface out of contact with the heatsink. The first effect may often be detected immediately by visual cracks in the package (if plastic), but usually an unnatural stress is imposed, which results in an early-life failure. The second effect results in hotter operation and is not manifested until much later.

Although punched holes are seldom acceptable in the relatively thick material used for extruded aluminum heatsinks, several manufacturers are capable of properly utilizing the capabilities inherent in both fine-edge blanking or sheared-through holes when applied to sheet metal as commonly used for stamped heatsinks. The holes are pierced using Class A progressive dies mounted on four-post die sets equipped with proper pressure pads and holding fixtures.

When mounting holes are drilled, a general practice with extruded aluminum, surface cleanup is important. Chamfers must be avoided because they reduce heat transfer surface and increase mounting stress. However, the edges must be broken to remove burrs which cause poor contact between device and heatsink and may puncture isolation material.

Surface Treatment

Many aluminum heatsinks are black-anodized to improve radiation ability and prevent corrosion. Anodizing results in significant electrical but negligible thermal insulation. It need only be removed from the mounting area when electrical contact is required. Heatsinks are also available which have a nickel plated copper insert under the semiconductor mounting area. No treatment of this surface is necessary.

Another treated aluminum finish is iridite, or chromate-acid dip, which offers low resistance because of its thin surface, yet has good electrical properties because it resists oxidation. It need only be cleaned of the oils and films that collect in the manufacture and storage of the sinks, a practice which should be applied to all heatsinks.

For economy, paint is sometimes used for sinks; removal of the paint where the semiconductor is attached is usually required because of paint's high thermal resistance. However, when it is necessary to insulate the semiconductor package from the heatsink, hard anodized or painted surfaces allow an easy installation for low voltage applications. Some manufacturers will provide anodized or painted surfaces meeting specific insulation voltage requirements, usually up to 400 volts.

It is also necessary that the surface be free from all foreign material, film, and oxide (freshly bared aluminum forms an oxide layer in a few seconds). Immediately prior to assembly, it is a good practice to polish the mounting area with No. 000 steel wool, followed by an acetone or alcohol rinse.

Interface Decisions

When any significant amount of power is being dissipated, something must be done to fill the air voids between mating surfaces in the thermal path. Otherwise the interface thermal resistance will be unnecessarily high and quite dependent upon the surface finishes.

For several years, thermal joint compounds, often called grease, have been used in the interface. They have a resistivity of approximately 60°C/W/in whereas air has 1200°C/W/in. Since surfaces are highly pock-marked with minute voids, use of a compound makes a significant reduction in the interface thermal resistance of the joint. However, the grease causes a number of problems, as discussed in the following section.

To avoid using grease, manufacturers have developed dry conductive and insulating pads to replace the more traditional materials. These pads are conformal and therefore partially fill voids when under pressure.

Thermal Compounds (Grease)

Joint compounds are a formulation of fine zinc or other conductive particles in a silicone oil or other synthetic base fluid which maintains a grease-like consistency with time and temperature. Since some of these compounds do not spread well, they should be evenly applied in a very thin layer using a spatula or lintless brush, and wiped lightly to remove excess material. Some cyclic rotation of the package will help the compound spread evenly over the entire contact area. Some experimentation is necessary to determine the correct quantity; too little will not fill all the voids, while too much may permit some compound to remain between well mated metal surfaces where it will substantially increase the thermal resistance of the joint.

To determine the correct amount, several semiconductor samples and heatsinks should be assembled with different amounts of grease applied evenly to one side of each mating surface. When the amount is correct a very small amount of grease should appear around the perimeter of each mating surface as the assembly is slowly torqued to the recommended value. Examination of a dismantled assembly should reveal even wetting across each mating surface. In production, assemblers should be trained to slowly apply the specified torque even though an excessive amount of grease appears at the edges of mating surfaces. Insufficient torque causes a significant increase in the thermal resistance of the interface.

To prevent accumulation of airborne particulate matter, excess compound should be wiped away using a cloth moistened with acetone or alcohol. These solvents should not contact plastic-encapsulated devices, as they may enter the package and cause a leakage path or carry in substances which might attack the semiconductor chip.

The silicone oil used in most greases has been found to evaporate from hot surfaces with time and become deposited on other cooler surfaces. Consequently, manufacturers must determine whether a microscopically thin coating of silicone oil on the entire assembly will pose any problems. It may be necessary to enclose components using grease. The newer synthetic base greases show far less tendency to migrate or creep than those made with a silicone oil base. However, their currently observed working temperature range are less, they are slightly poorer on thermal conductivity and dielectric strength and their cost is higher.

Data showing the effect of compounds on several package types under different mounting conditions is shown in Table 5-1. The rougher the surface, the more valuable the grease becomes in lowering contact resistance; therefore, when mica insulating washers are used, use of grease is generally mandatory. The joint compound also improves the breakdown rating of the insulator.

Table 5-1
Approximate Values for Interface Thermal Resistance Data from Measurements Performed in Motorola Applications Engineering Laboratory

Dry interface values are subject to wide variation because of extreme dependence upon surface conditions. Unless otherwise noted the case temperature is monitored by a thermocouple located directly under the die reached through a hole in the heatsink. (See Appendix B for a discussion of Interface Thermal Resistance Measurements.)

Package Type and Data		Interface Thermal Resistance (°C/W)						
JEDEC Outlines	Description	Test Torque In-Lb	Metal-to-Metal		With Insulator			See Note
			Dry	Lubed	Dry	Lubed	Type	
TO-204AA (TO-3)	Diamond Flange	6	0.5	0.1	1.3	0.36	3 mil Mica	1
TO-220AB	Thermowatt	8	1.2	1.0	3.4	1.6	2 mil Mica	1, 2

NOTES: 1. See Figures 5-7 and 5-8 for additional data on TO-204AA and TO-220 packages.
2. Screw not insulated. See Figure 5-12.

Conductive Pads

Because of the difficulty of assembly using grease and the evaporation problem, some equipment manufacturers will not, or cannot, use grease. To minimize the need for grease, several vendors offer dry conductive pads which approximate performance obtained with grease. Data for a greased bare joint and a joint using Grafoil, a dry graphite compound, is shown in the data of Figure 5-7. Grafoil is claimed to be a replacement for grease when no electrical isolation is required; the data indicates it does indeed perform as well as grease. Another conductive pad available from Aavid is called KON-DUX. It is made with a unique, grain oriented, flake-like structure (patent pending). Highly compressible, it becomes formed to the surface roughness of both the heatsink and semiconductor. Manufacturer's data shows it to provide an interface thermal resistance better than a metal interface with filled silicone grease. Similar dry conductive pads are available from other manufacturers. They are a fairly recent development; long term problems, if they exist, have not yet become evident.

Insulation Considerations

Since most power semiconductors use are vertical device construction it is common to manufacture power semiconductors with the output electrode (anode, collector or drain) electrically common to the case; the problem of isolating this terminal from ground is a common one. For lowest overall thermal resistance, which is quite important when high power must be dissipated, it is best to isolate the entire heatsink/semiconductor structure from ground, rather than to use an insulator between the semiconductor and the heatsink. Heatsink isolation is not always possible, however, because of EMI requirements, safety reasons, instances where a chassis serves as a heatsink or where a heatsink is common to several non-isolated packages. In these situations insulators are used to isolate the individual components from the heatsink. Newer packages, such as the Motorola Full Pak and EMS modules, contain the electrical isolation material within, thereby saving the equipment manufacturer the burden of addressing the isolation problem.

Insulator Thermal Resistance

When an insulator is used, thermal grease is of greater importance than with a metal-to-metal contact, because two interfaces exist instead of one and some materials, such as mica, have a hard, markedly uneven surface. With many isolation materials reduction of interface thermal resistance of between 2 to 1 and 3 to 1 are typical when grease is used.

Data obtained by Thermalloy, showing interface resistance for different insulators and torques applied to TO-204 (TO-3) and TO-220 packages, are shown in Figure 5-7, for bare and greased surfaces. Similar materials to those shown are available from several manufacturers. It is obvious that with some arrangements, the interface thermal resistance exceeds that of the semiconductor (junction to case).

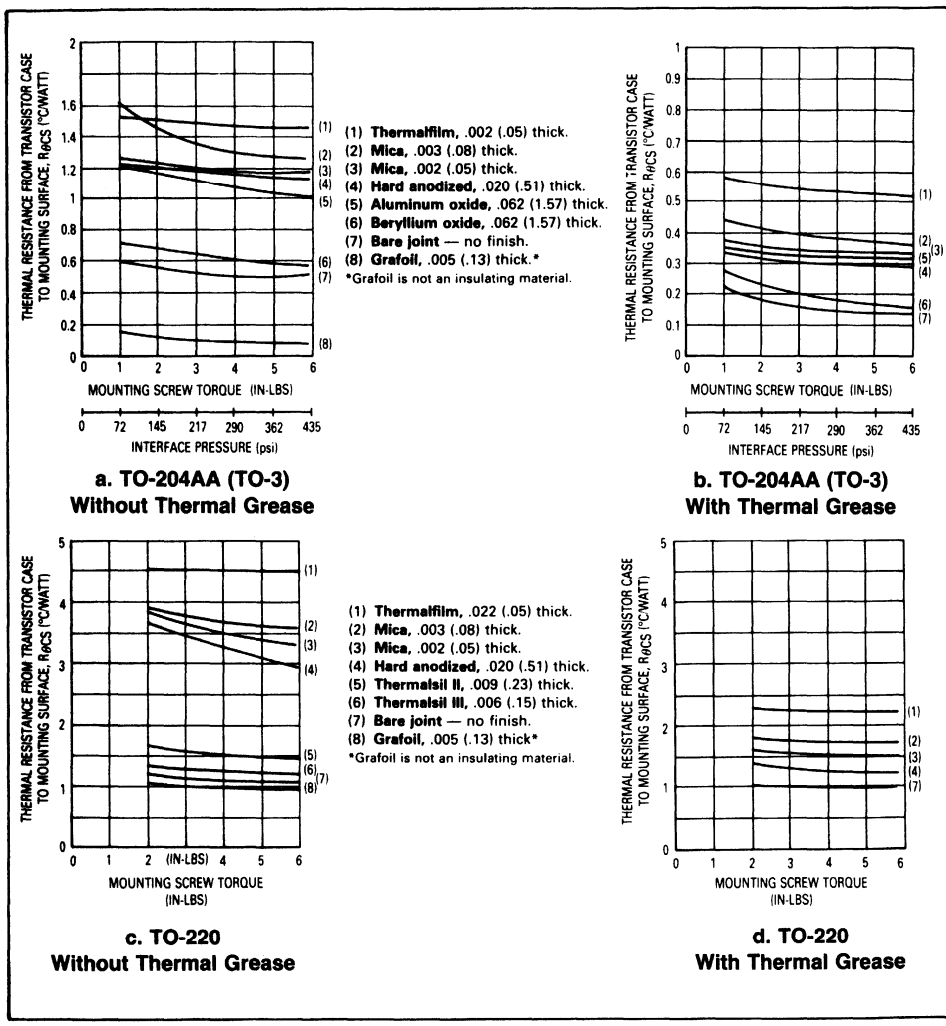

Figure 5-7. Interface Thermal Resistance for TO-204, TO-3 and TO-220 Packages using Different Insulating Materials as a Function of Mounting Screw Torque (Data Courtesy Thermalloy)

Referring to Figure 5-7, one may conclude that when high power is handled, beryllium oxide is unquestionably the best. However, it is an expensive choice. (It should not be cut or abraided, as the dust is highly toxic.) Thermafilm is a filled polyimide material which is used for isolation (variation of Kapton). It is a popular material for low power applications because of its low cost ability to withstand high temperatures, and ease of handling in contrast to mica which chips and flakes easily.

A number of other insulating materials are also shown. They cover a wide range of insulation resistance, thermal resistance and ease of handling. Mica has been widely used in the past because it offers high breakdown voltage and fairly low thermal resistance at a low cost but it certainly should be used with grease.

Silicone rubber insulators have gained favor because they are somewhat conformal under pressure. Their ability to fill in most of the metal voids at the interface reduces the need for thermal grease. When first introduced, they suffered from cut-through after a few years in service. The ones presently available have solved this problem by having imbedded pads of Kapton or fiberglass. By comparing Figures 5-7c and 5-7d, it can be noted that Thermasil, a filled silicone rubber, without grease, has about the same interface thermal resistance as greased mica for the TO-220 package.

A number of manufacturers offer silicone rubber insulators. Table 5-2 shows measured performance of a number of these insulators under carefully controlled, nearly identical conditions. The interface thermal resistance extremes are over 2:1 for the various materials. It is also clear that some of the insulators are much more tolerant than others of out-of-flat surfaces. Since the tests were performed, newer products have been introduced. The Bergquist K-10 pad, for example, is described as having about 2/3 the interface resistance of the Sil Pad 1000 which would place its performance close to the Chomerics 1671 pad. AAVID also offers an isolated pad called Rubber-Duc, however it is only available vulcanized to a heatsink and therefore was not included in the comparison. Published data from AAVID shows $R\theta cs$ below 0.3°C/W for pressures above 500 psi. However, surface flatness and other details are not specified so a comparison cannot be made with other data in this note.

Table 5-2. Thermal Resistance of Silicone Rubber Pads

Manufacturer	Product	$R_{\theta CS}$ @ 3 Mils*	$R_{\theta CS}$ @ 7.5 Mils*
Wakefield	Delta Pad 173-7	.790	1.175
Bergquist	Sil Pad K-4	.752	1.470
Stockwell Rubber	1867	.742	1.015
Bergquist	Sil Pad 400-9	.735	1.205
Thermalloy	Thermalsil II	.680	1.045
Shin-Etsu	TC-30AG	.664	1.260
Bergquist	Sil Pad 400-7	.633	1.060
Chomerics	1674	.592	1.190
Wakefield	Delta Pad 174-9	.574	.755
Bergquist	Sil Pad 1000	.529	.935
Ablestik	Thermal Wafers	.500	.990
Thermalloy	Thermalsil III	.440	1.035
Chomerics	1671	.367	.655

*Test Fixture Deviation from flat from Thermalloy EIR86-1010.

The thermal resistance of some silicone rubber insulators is sensitive to surface flatness when used under a fairly rigid base package. Data for a TO-204AA (TO-3) package insulated with Thermasil is shown on Figure 5-8. Observe that the "worst case" encountered (7.5 mils) yields results having about twice the thermal resistance of the "typical case" (3 mils), for the more conductive insulator. In order for Thermasil III to exceed the performance of greased mica, total surface flatness must be under 2 mils, a situation that requires spot finishing.

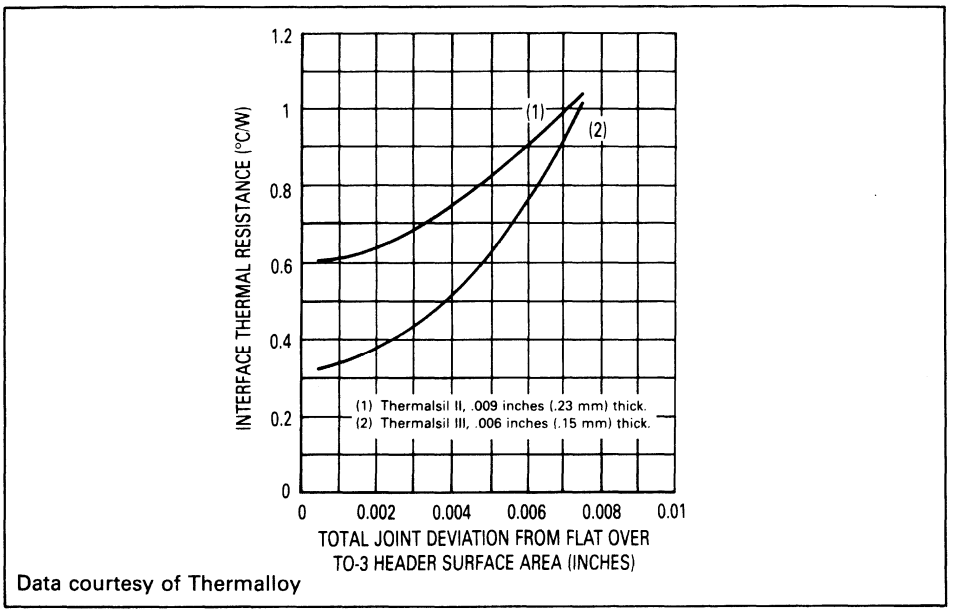

Figure 5-8. Effect of Total Surface Flatness on Interface Resistance Using Silicon Rubber Insulators

Silicon rubber insulators have a number of unusual characteristics. Besides being affected by surface flatness and initial contact pressure, time is a factor. For example, in a study of the Cho-Therm 1688 pad thermal interface impedance dropped from 0.90°C/W to 0.70°C/W at the end of 1000 hours. Most of the change occurred during the first 200 hours where $R\theta CS$ measured 0.74°C/W. The torque on the conventional mounting hardware had decreased to 3 in-lb from an initial 6 in-lb. With non-conformal materials, a reduction in torque would have increased the interface thermal resistance.

Because of the difficulties in controlling all variables affecting tests of interface thermal resistance, data from different manufacturers is not in good agreement. Table 5-3 shows data obtained from two sources. The relative performance is the same, except for mica which varies widely in thickness. Appendix B discusses the variables which need to be controlled. At the time of this writing ASTM Committee D9 is developing a standard for interface measurements.

The conclusions to be drawn from all this data is that some types of silicon rubber pads, mounted dry, will out perform the commonly used mica with grease. Cost may be a determining factor in making a selection.

Table 5-3. Performance of Silicon Rubber Insulators Tested per MIL-I-49456

Material	Measured Thermal Resistance (°C/W)	
	Thermalloy Data(1)	Berquist Data(2)
Bare Joint, greased	0.033	0.008
BeO, greased	0.082	—
Cho-Therm, 1617	0.233	—
Q Pad (non-insulated)	—	0.009
Sil-Pad, K-10	0.263	0.200
Thermasil III	0.267	—
Mica, greased	0.329	0.400
Sil-Pad 1000	0.400	0.300
Cho-therm 1674	0.433	—
Thermasil II	0.500	—
Sil-Pad 400	0.533	0.440
Sil-Pad K-4	0.583	0.440

(1) From Thermalloy EIR 87-1030
(2) From Berquist Data Sheet

Insulation Resistance

When using insulators, care must be taken to keep the mating surfaces clean. Small particles of foreign matter can puncture the insulation, rendering it useless or seriously lowering its dielectric strength. In addition, particularly when voltages higher than 300 V are encountered, problems with creepage may occur. Dust and other foreign material can shorten creepage distances significantly; so having a clean assembly area is important. Surface roughness and humidity also lower insulation resistance. Use of thermal grease usually raises the withstand voltage of the insulation system but excess must be removed to avoid collecting dust. Because of these factors, which are not amenable to analysis, hi-pot testing should be done on prototypes and a large margin of safety employed.

Insulated Electrode Packages

Because of the nuisance of handling and installing the accessories needed for an insulated semiconductor mounting, equipment manufacturers have longed for cost-effective insulated packages since the 1950's. The first to appear were stud mount types which usually have a layer of beryllium oxide between the stud hex and the can. Although effective, the assembly is costly and requires manual mounting and lead wire soldering to terminals on top of the case. In the late eighties, a number of electrically isolated parts became available from various semiconductor manufacturers. These offerings presently consist of multiple chips and integrated circuits as well as the more conventional single chip devices.

The newer insulated packages can be grouped into two categories. The first has insulation between the semiconductor chips and the mounting base; an exposed area of the mounting base is used to secure the part. The second category contains parts which have a plastic overmold covering the metal mounting base. The Full Pak, Case 221C, illustrated in Figure 5-13, is an example of parts in the second category.

Parts in the first category — those with an exposed metal flange or tab — are mounted the same as their non-insulated counterparts. However, as with any mounting system where pressure is bearing on plastic, the overmolded type should be used with a conical compression washer, described later in this note.

Fastener and Hardware Characteristics

Characteristics of fasteners, associated hardware, and the tools to secure them determine their suitability for use in mounting the various packages. Since many problems have arisen because of improper choices, the basic characteristics of several types of hardware are discussed next.

Compression Hardware

Normal split ring lock washers are not the best choice for mounting power semiconductors. A typical #6 washer flattens at about 50 pounds, whereas 150 to 300 pounds is needed for good heat transfer at the interface. A very useful piece of hardware is the conical, sometimes called a Belleville washer, compression washer. As shown in Figure 5-9, it has the ability to maintain a fairly constant pressure over a wide range of its physical deflection — generally 20% to 80%. When installing, the assembler applies torque until the washer depresses to half its original height. (Tests should be run prior to setting up the assembly line to determine the proper torque for the fastener used to achieve 50% deflection.) The washer will absorb any cyclic expansion of the package, insulating washer or other materials caused by temperature changes. Conical washers are the key to successful mounting of devices requiring strict control of the mounting force or when plastic hardware is used in the mounting scheme. They are used with the large face contacting the packages. A new variation of the conical washer includes it as part of a nut assembly. Called a Sync Nut, the patented device can be soldered to a PC board and the semiconductor mounted with a 6-32 machine screw.[4]

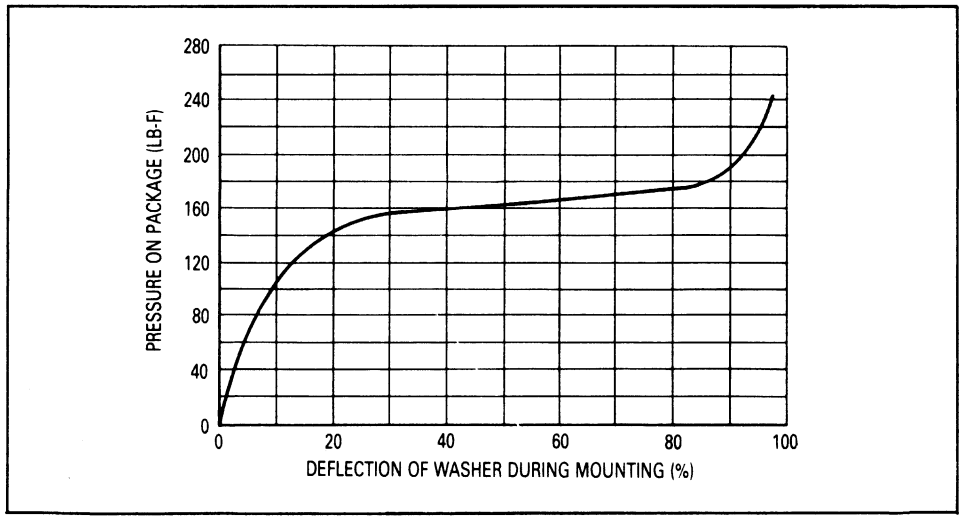

Figure 5-9. Characteristics of the Conical Compression Washers Designed for Use with Plastic Body Mounted Semiconductors

(4) ITW Shakeproof, St. Charles Road, Elgin, IL 60120.

Clips

Fast assembly is accomplished with clips. When only a few watts are being dissipated, the small board-mounted or free-standing heat dissipators with an integral clip, offered by several manufacturers, result in a low cost assembly. When higher power is being handled, a separate clip may be used with larger heatsinks. In order to provide proper pressure, the clip must be specially designed for a particular heatsink thickness and semiconductor package.

Clips are especially popular with plastic packages such as the TO-220 and TO-126. In addition to fast assembly, the clip provides lower interface thermal resistance than other assembly methods when it is designed for proper pressure to bear on the top of the plastic over the die. The TO-220 package usually is lifted up under the die location when mounted with a single fastener through the hole in the tab because of the high pressure at one end.

Machine Screws

Machine screws, conical washers, and nuts (or sync-nuts) can form a trouble-free fastener system for all types of packages which have mounting holes. However, proper torque is necessary. Torque ratings apply when dry; therefore, care must be exercised when using thermal grease to prevent it from getting on the threads as inconsistent torque readings result. Machine screw heads should not directly contact the surface of plastic packages types as the screw heads are not sufficiently flat to provide properly distributed force. Without a washer, cracking of the plastic case may occur.

Self-Tapping Screws

Under carefully controlled conditions, sheet-metal screws are acceptable. However, during the tapping-process with a standard screw, a volcano-like protrusion will develop in the metal being threaded; an unacceptable surface that could increase the thermal resistance may result. When standard sheet metal screws are used, they must be used in a clearance hole to engage a speed-nut. If a self tapping process is desired, the screw type must be used which roll-forms machine screw threads.

Rivets

Rivets are not a recommended fastener for any of the plastic packages. When a rugged metal flange-mount package is being mounted directly to a heatsink, rivets can be used provided press-riveting is used. Crimping force must be applied slowly and evenly. Pop-riveting should never be used because the high crimping force could cause deformation of most semiconductor packages. Aluminum rivets are much preferred over steel because less pressure is required to set the rivet and thermal conductivity is improved.

The hollow rivet, or eyelet, is preferred over solid rivets. An adjustable, regulated pressure press is used such that a gradually increasing pressure is used to pan the eyelet. Use of sharp blows could damage the semiconductor die.

Solder

Until the advent of the surface mount assembly technique, solder was not considered a suitable fastener for power semiconductors. However, user demand has led to the development of new packages for this application. Acceptable soldering methods include conventional belt-furnace, irons, vapor-phase reflow,

and infrared reflow. It is important that the semiconductor temperature not exceed the specified maximum (usually 260°C) or the die bond to the case could be damaged. A degraded die bond has excessive thermal resistance which often leads to a failure under power cycling.

Adhesives

Adhesives are available which have coefficients of expansion compatible with copper and aluminum.[5] Highly conductive types are available; a 10 mil layer has approximately 0.3°C/W interface thermal resistance. Different types are offered: high strength types for non-field-servicable systems or low strength types for field-serviceable systems. Adhesive bonding is attractive when case mounted parts are used in wave soldering assembly because thermal greases are not compatible with the conformal coatings used and the greases foul the solder process.

Plastic Hardware

Most plastic materials will flow, but differ widely in this characteristic. When plastic materials form parts of the fastening system, compression washers are highly valuable to assure that the assembly will not loosen with time and temperature cycling. As previously discussed, loss of contact pressure will increase interface thermal resistance.

Fastening Techniques

Each of the various classes of packages in use requires different fastening techniques. Details pertaining to each type are discussed in following sections. Some general considerations follow.

To prevent galvanic action from occurring when devices are used on aluminum heatsinks in a corrosive atmosphere, many devices are nickel- or gold-plated. Consequently, precautions must be taken not to mar the finish.

Another factor to be considered is that when a copper based part is rigidly mounted to an aluminum heatsink, a bimetallic system results which will bend with temperature changes. Not only is the thermal coefficient of expansion different for copper and aluminum, but the temperature gradient through each metal also causes each component to bend. If bending is excessive and the package is mounted by two or more screws the semiconductor chip could be damaged. Bending can be minimized by:

1. Mounting the component parallel to the heatsink fins to provide increased stiffness.
2. Allowing the heatsink holes to be a bit oversized so that some slip between surfaces can occur as temperature changes.
3. Using a highly conductive thermal grease or mounting pad between the heatsink and semiconductor to minimize the temperature gradient and allow for movement.

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(5) Robert Batson, Elliot Fraunglass and James P. Moran, "Heat Dissipation Through Thermalloy Conductive Adhesives," EMTAS '83. Conference, February 1–3, Phoenix, AZ; Society of Manufacturing Engineers, One SME Drive, P.O. Box 930, Dearborn, MI 48128.

Flange Mount

Few known mounting difficulties exist with the smaller flange mount packages, such as the TO-204 (TO-3). The rugged base and distance between die and mounting holes combine to make it extremely difficult to cause any warpage unless mounted on a surface which is badly bowed or unless one side is tightened excessively before the other screw is started. It is therefore good practice to alternate tightening of the screws so that pressure is evenly applied. After the screws are finger-tight the hardware should be torqued to its final specification in at least two sequential steps. A typical mounting installation for a popular flange type part is shown in Figure 5-10. Machine screws (preferred) self-tapping screws, eyelets, or rivets may be used to secure the package using guidelines in the previous section. "Fastener and Hardware Characteristics."

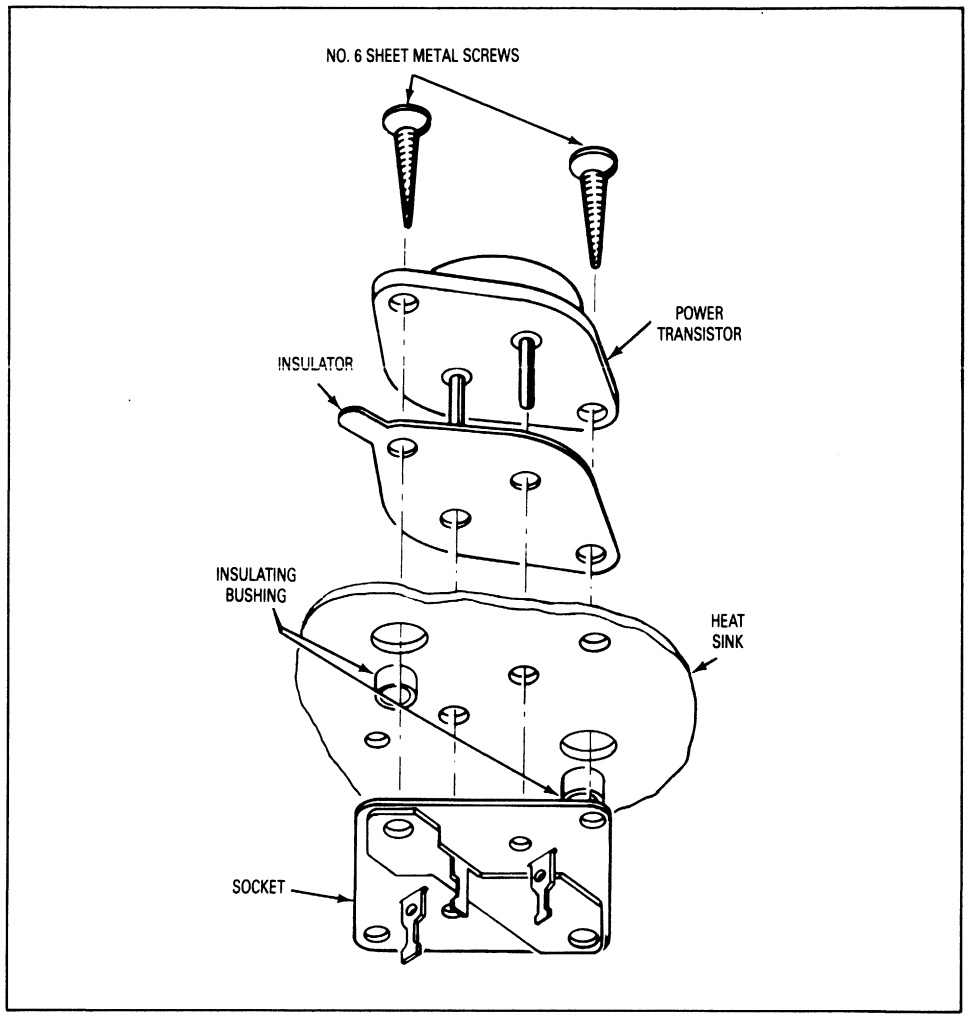


Figure 5-10. Hardware Used for a TO-204AA (TO-3) Flange Mount Part

Tab Mount

The tab mount class is composed of a wide array of packages as illustrated in Figure 5-11. Mounting considerations for all varieties are similar to that for the popular TO-220 package, whose suggested mounting arrangements and hardware are shown in Figure 5-12. The rectangular washer shown in Figure 5-12a is used to minimize distortion of the mounting flange; excessive distortion could cause damage to the semiconductor chip. Use of the washer is only important when the size of the mounting hole exceeds 0.140 inch (6–32 clearance). Larger holes are needed to accommodate the lower insulating bushing when the screw is electrically connected to the case; however, the holes should not be larger than necessary to provide hardware clearance and should never exceed a diameter of 0.250 inch. Flange distortion is also possible if excessive torque is used during mounting. A maximum torque of 8 inch-pounds is suggested when using a 6–32 screw.

Care should be exercised to assure that the tool used to drive the mounting screw never comes in contact with the plastic body during the driving operation. Such contact can result in damage to the plastic body and internal device connections. To minimize this problem, Motorola TO-220 packages have a chamfer on one end. TO-220 packages of other manufacturers may need a spacer or combination spacer and isolation bushing to raise the screw head above the top surface of the plastic.

The popular TO-220 Package and others of similar construction lift off the mounting surface as pressure is applied to one end. (See Appendix B, Figure B1.) To counter this tendency, at least one hardware manufacturer offers a hard plastic cantilever beam which applies more even pressure on the tab.[6] In addition, it separates the mounting screw from the metal tab. Tab mount parts may also be effectively mounted with clips as shown in Figure 5-14c. To obtain high pressure without cracking the case, a pressure spreader bar should be used under the clip. Interface thermal resistance with the cantilever beam or clips can be lower than with screw mounting.

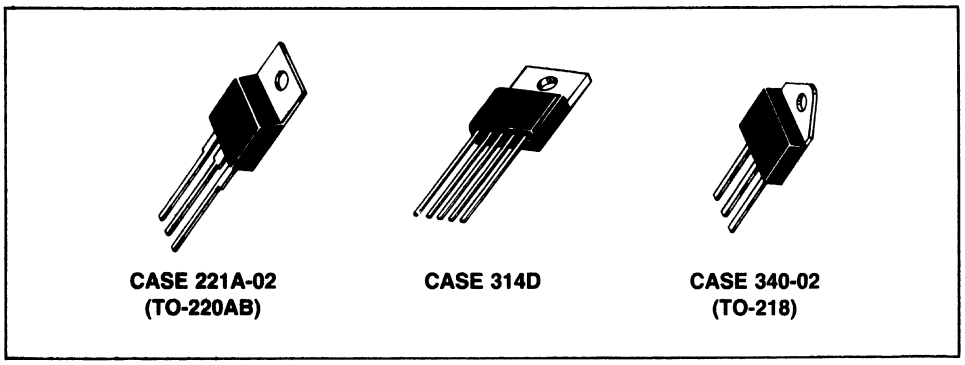


Figure 5-11. Several Types of Tab-Mount Parts

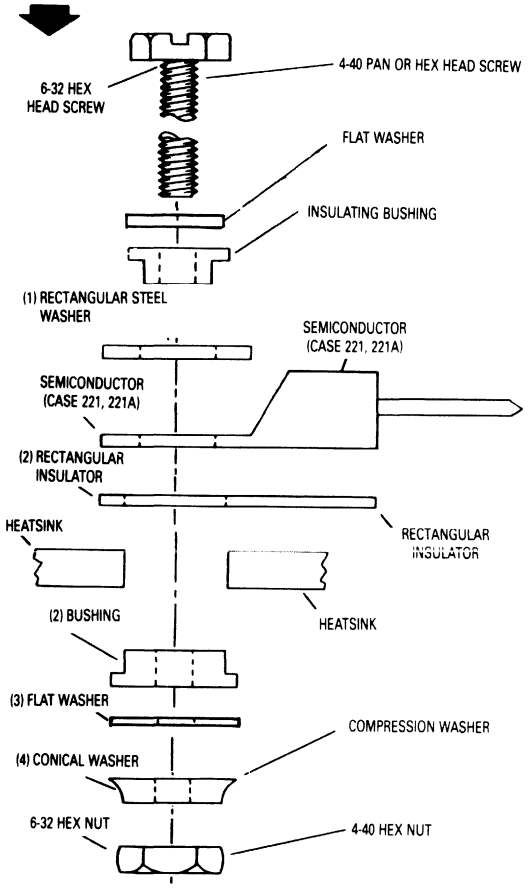
(6) Catalog, Edition 18, Richco Plastic Company, 5825 N. Tripp Ave., Chicago, IL 60546.

a) Preferred Arrangement for Isolated or Non-isolated Mounting. Screw is at Semiconductor Case Potential. 6-32 Hardware is Used.

Choose from Parts Listed Below.

b) Alternate Arrangement for Isolated Mounting when Screw must be at Heatsink Potential. 4-40 Hardware is Used.

Use Parts Listed Below.



(1) Used with thin chassis and/or large hole.
(2) Used when isolation is required.
(3) Required when nylon bushing is used.

Figure 5-12. Mounting Arrangements for Tab Mount TO-220

Plastic Body Mount

The Full Pak plastic power packages shown in Figure 5-13 are typical of packages in this group. They have been designed to feature minimum size with no compromise in thermal resistance.

The Full Pak (Case 221C-01) is similar to a TO-220 except that the tab is encased in plastic. Because the mounting force is applied to plastic, the mounting procedure differs from a standard TO-220 and is similar to that of the Thermopad.

Several types of fasteners may be used to secure these packages; machine screws, eyelets, or clips are preferred. With screws or eyelets, a conical washer should be used which applies the proper force to the package over a fairly wide range of deflection and distributes the force over a fairly large surface area. Screws should not be tightened with any type of air-driven torque gun or equipment which may cause high impact. Characteristics of a suitable conical washer is shown in Figure 5-9.

The Full Pak, (Case 221C, 221D and 340B) permits the mounting procedure to be greatly simplified over that of a standard TO-220. As shown in Figure 5-14c, one properly chosen clip, inserted into two slotted holes in the heatsink,

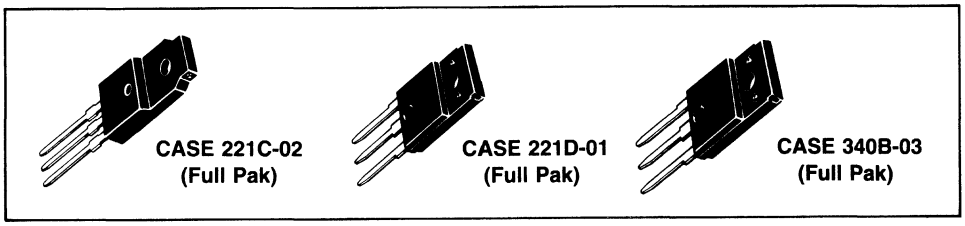


Figure 5-13. Plastic Body-Mount Packages

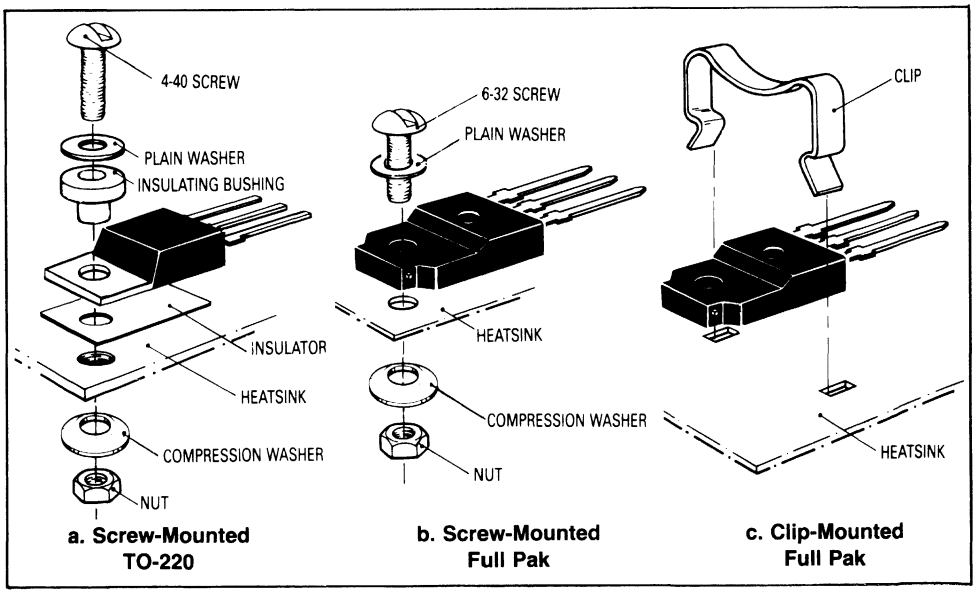


Figure 5-14. Mounting Arrangements for the Full Pak as Compared to a Conventional TO-220

is all the hardware needed. Even though clip pressure is much lower than obtained with a screw, the thermal resistance is about the same for either method. This occurs because the clip bears directly on top of the die and holds the package flat while the screw causes the package to lift up somewhat under the die. (See Figure B1 of Appendix B.) The interface should consist of a layer of thermal grease or a highly conductive thermal pad. Of course, screw mounting shown in Figure 5-14b may also be used but a conical compression washer should be included. Both methods afford a major reduction in hardware as compared to the conventional mounting method with a TO-220 package which is shown in Figure 5-14a.

Surface Mount

Although many of the tab mount parts have been surface mounted, special small footprint packages for mounting power semiconductors using surface mount assembly techniques have been developed. The DPAK, shown in Figure 5-15, for example, will accommodate a die up to 112 mils x 112 mils, and has a typical thermal resistance around 2°C/W junction to case. The thermal resistance values of the solder interface is well under 1°C/W. The printed circuit board also serves as the heatsink.

Standard Glass-Epoxy 2-ounce boards do not make very good heatsinks because the thin foil has a high thermal resistance. As Figure 5-16 shows, thermal

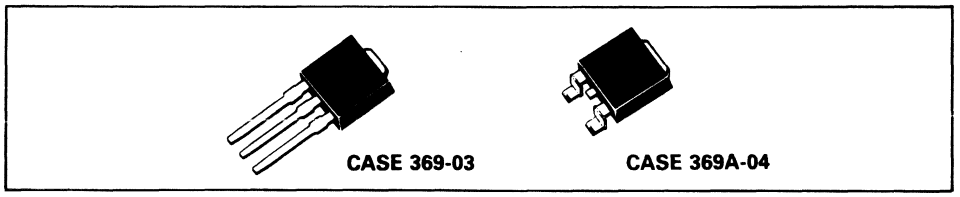


Figure 5-15. Surface Mount D-PAK Parts

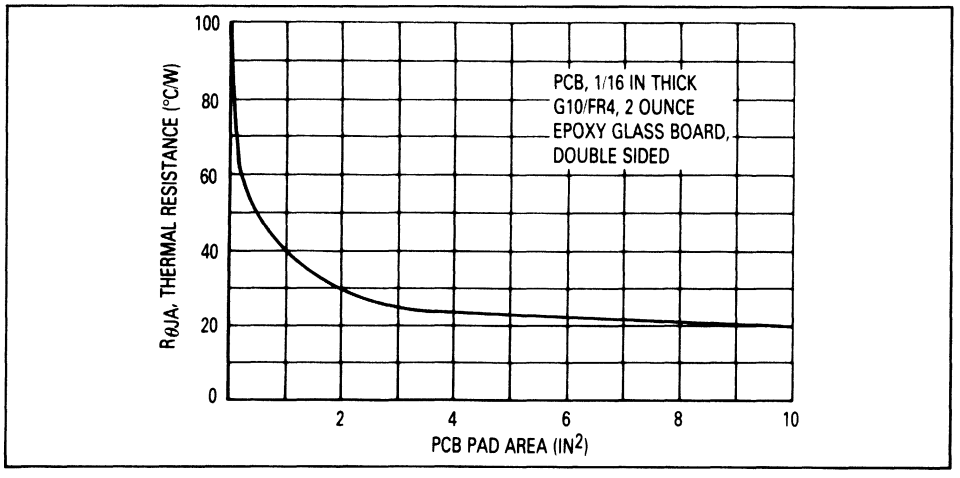


Figure 5-16. Effect of Footprint Area on Thermal Resistance of DPAK Mounted on a Glass-Epoxy Board

(7) Herb Fick, "Thermal Management of Surface Mount Power Devices," Powerconversion and Intelligent Motion, August 1987.

resistance assymtotes to about 20°C/W at 10 square inches of board area, although a point of diminishing returns occurs at about 3 square inches.

Boards are offered that have thick aluminum or copper substrates. A dielectric coating designed for low thermal resistance is overlayed with one or two ounce copper foil for the preparation of printed conductor traces. Tests run on such a product indicate that case to substrate thermal resistance is in the vicinity of 1°C/W, exact values depending upon board type.[7] The substrate may be an effective heatsink itself, or it can be attached to a conventional finned heatsink for improved performance.

Since DPAK and other surface mount packages are designed to be compatible with surface mount assembly techniques, no special precautions are needed other than to insure that maximum temperature/time profiles are not exceeded.

Free Air and Socket Mounting

In applications where average power dissipation is on the order of a watt or so, most power semiconductors may be mounted with little or no heatsinking. The leads of the various metal power packages are not designed to support the packages; their cases must be firmly supported to avoid the possibility of cracked seals around the leads. Many plastic packages may be supported by their leads in applications where high shock and vibration stresses are not encountered and where no heatsink is used. The leads should be as short as possible to increase vibration resistance and reduce thermal resistance. As a general practice however, it is better to support the package. A plastic support for the TO-220 Package and other similar types is offered by heatsink accessory vendors.

In certain situations, in particular where semiconductor testing is required or prototypes are being developed, sockets are desirable. Manufacturers have provided sockets for many of the packages available from Motorola. The user is urged to consult manufacturers' catalogs for specific details. Sockets with Kelvin connections are necessary to obtain accurate voltage readings across semiconductor terminals.

Connecting and Handling Terminals

Pins, leads, and tabs must be handled and connected properly to avoid undue mechanical stress which could cause semiconductor failure. Change in mechanical dimensions as a result of thermal cycling over operating temperature extremes must be considered. Standard metal, plastic, and RF stripline packages each have some special considerations.

Metal Packages

The pins of metal packaged devices using glass to metal seals are not designed to handle any significant bending or stress. If abused, the seals could crack. Wires may be attached using sockets, crimp connectors or solder, provided the data sheet ratings are observed. When wires are attached directly to the pins, flexible or braided leads are recommended in order to provide strain relief.

Plastic Packages

The leads of the plastic packages are somewhat flexible and can be reshaped although this is not a recommended procedure. In many cases, a heatsink can be chosen which makes lead-bending unnecessary. Numerous lead- and tab-forming

options are available from Motorola on large quantity orders. Preformed leads remove the users risk of device damage caused by bending.

If, however, lead-bending is done by the user, several basic considerations should be observed. When bending the lead, support must be placed between the point of bending and the package. For forming small quantities of units, a pair of pliers may be used to clamp the leads at the case, while bending with the fingers or another pair of pliers. For production quantities, a suitable fixture should be made.

The following rules should be observed to avoid damage to the package.

1. A leadbend radius greater than 1/32 inch for TO-220.
2. No twisting of leads should be done at the case.
3. No axial motion of the lead should be allowed with respect to the case.

The leads of plastic packages are not designed to withstand excessive axial pull. Force in this direction greater than 4 pounds may result in permanent damage to the device. If the mounting arrangement imposes axial stress on the leads, a condition which may be caused by thermal cycling, some method of strain relief should be devised. When wires are used for connections, care should be exercised to assure that movement of the wire does not cause movement of the lead at the lead-to-plastic junctions. Highly flexible or braided wires are good for providing strain relief.

Wire-wrapping of the leads is permissible, provided that the lead is restrained between the plastic case and the point of the wrapping. The leads may be soldered; the maximum soldering temperature, however, must not exceed 260°C and must be applied for not more than 5 seconds at a distance greater than 1/8 inch from the plastic case.

Cleaning Circuit Boards

It is important that any solvents or cleaning chemicals used in the process of degreasing or flux removal do not affect the reliability of the devices. Alcohol and unchlorinated Freon solvents are generally satisfactory for use with plastic devices, since they do not damage the package. Hydrocarbons such as gasoline and chlorinated Freon may cause the encapsulant to swell, possibly damaging the transistor die.

When using an ultrasonic cleaner for cleaning circuit boards, care should be taken with regard to ultrasonic energy and time of application. This is particularly true if any packages are free-standing without support.

Thermal System Evaluation

Assuming that a suitable method of mounting the semiconductor without incurring damage has been achieved, it is important to ascertain whether the junction temperature is within bounds.

In applications where the power dissipated in the semiconductor consists of pulses at a low duty cycle, the instantaneous or peak junction temperature, not average temperature, may be the limiting condition. In this case, use must be made of transient thermal resistance data. For a full explanation of its use, see Motorola Application Note, AN569.

Other applications, notably switches driving highly reactive loads, may create severe current crowding conditions which render the traditional concepts of thermal resistance or transient thermal impedance invalid. In this case, transistor safe

operating area, thyristor di/dt limits, or equivalent ratings as applicable, must be observed.

Fortunately, in many applications, a calculation of the average junction temperature is sufficient. It is based on the concept of thermal resistance between the junction and a temperature reference point on the case. (See Appendix A.) A fine wire thermocouple should be used, such as #36 AWG, to determine case temperature. Average operating junction temperature can be computed from the following equation:

$$T_J = T_C + R\theta_{JC} \times P_D$$

where T_J = junction temperature (°C)
T_C = case temperature (°C)
$R\theta_{JC}$ = thermal resistance junction-to-case as specified on the data sheet (°C/W)
P_D = power dissipated in the device (W)

The difficulty in applying the equation often lies in determining the power dissipation. Two commonly used empirical methods are graphical integration and substitution.

Graphical Integration

Graphical integration may be performed by taking oscilloscope pictures of a complete cycle of the voltage and current waveforms, using a limit device. The pictures should be taken with the temperature stabilized. Corresponding points are then read from each photo at a suitable number of time increments. Each pair of voltage and current values are multiplied together to give instantaneous values of power. The results are plotted on linear graph paper, the number of squares within the curve counted, and the total divided by the number of squares along the time axis. The quotient is the average power dissipation. Oscilloscopes are available to perform these measurements and make the necessary calculations.

Substitution

This method is based upon substituting an easily measurable, smooth dc source for a complex waveform. A switching arrangement is provided which allows operating the load with the device under test, until it stabilizes in temperature. Case temperature is monitored. By throwing the switch to the "test" position, the device under test is connected to a dc power supply, while another pole of the switch supplies the normal power to the load to keep it operating at full power level. The dc supply is adjusted so that the semiconductor case temperature remains approximately constant when the switch is thrown to each position for about 10 seconds. The dc voltage and current values are multiplied together to obtain average power. It is generally necessary that a Kelvin connection be used for the device voltage measurement.

Appendix A
Thermal Resistance Concepts

The basic equation for heat transfer under steady-state conditions is generally written as:

$$q = hA\Delta T \quad (1)$$

where q = rate of heat transfer or power dissipation (P_D)
h = heat transfer coefficient,
A = area involved in heat transfer,
ΔT = temperature difference between regions of heat transfer.

However, electrical engineers generally find it easier to work in terms of thermal resistance, defined as the ratio of temperature to power. From Equation 1, thermal resistance, $R\theta$, is

$$R\theta = \Delta T/q = 1/hA \quad (2)$$

The coefficient (h) depends upon the heat transfer mechanism used and various factors involved in that particular mechanism.

An analogy between Equation (2) and Ohm's Law is often made to form models of heat flow. Note that T could be thought of as a voltage thermal resistance corresponds to electrical resistance (R); and, power (q) is analogous to current (I). This gives rise to a basic thermal resistance model for a semiconductor as indicated by Figure A1.

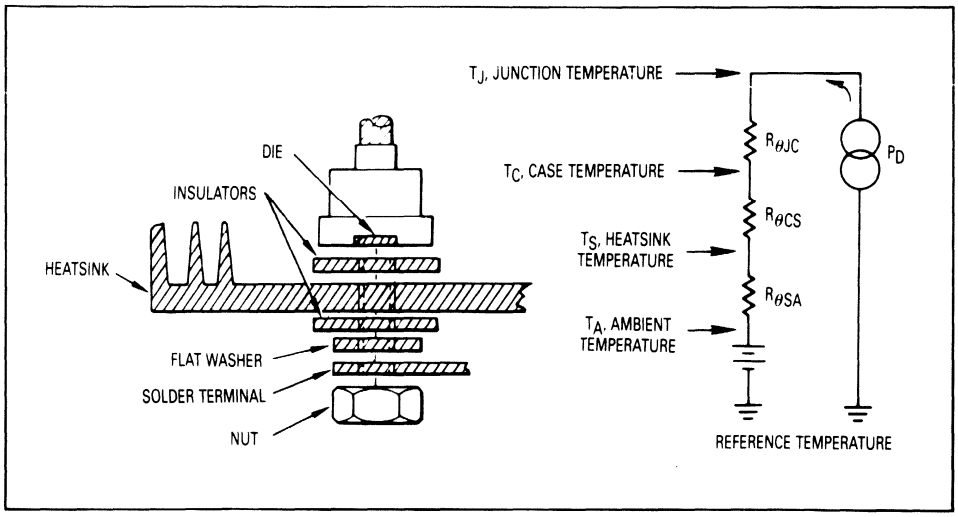


Figure A-1. Basic Thermal Resistance Model Showing Thermal to Electrical Analogy for a Semiconductor

The equivalent electrical circuit may be analyzed by using Kirchoff's Law and the following equation results:

$$T_J = P_D(R\theta_{JC} + R\theta_{CS} + R\theta_{SA}) + T_A \quad (3)$$

where T_J = junction temperature,
P_D = power dissipation
$R\theta_{JC}$ = semiconductor thermal resistance (junction to case),
$R\theta_{CS}$ = interface thermal resistance (case to heatsink),
$R\theta_{SA}$ = heatsink thermal resistance (heatsink to ambient),
T_A = ambient temperature.

The thermal resistance junction to ambient is the sum of the individual components. Each component must be minimized if the lowest junction temperature is to result.

The value for the interface thermal resistance, $R\theta_{CS}$, may be significant compared to the other thermal-resistance terms. A proper mounting procedure can minimize $R\theta_{CS}$.

The thermal resistance of the heatsink is not absolutely constant; its thermal efficiency increases as ambient temperature increases and it is also affected by orientation of the sink. The thermal resistance of the semiconductor is also variable; it is a function of biasing and temperature. Semiconductor thermal resistance specifications are normally at conditions where current density is fairly uniform. In some applications such as in RF power amplifiers and short-pulse applications, current density is not uniform and localized heating in the semiconductor chip will be the controlling factor in determining power handling ability.

Appendix B
Measurement of Interface Thermal Resistance

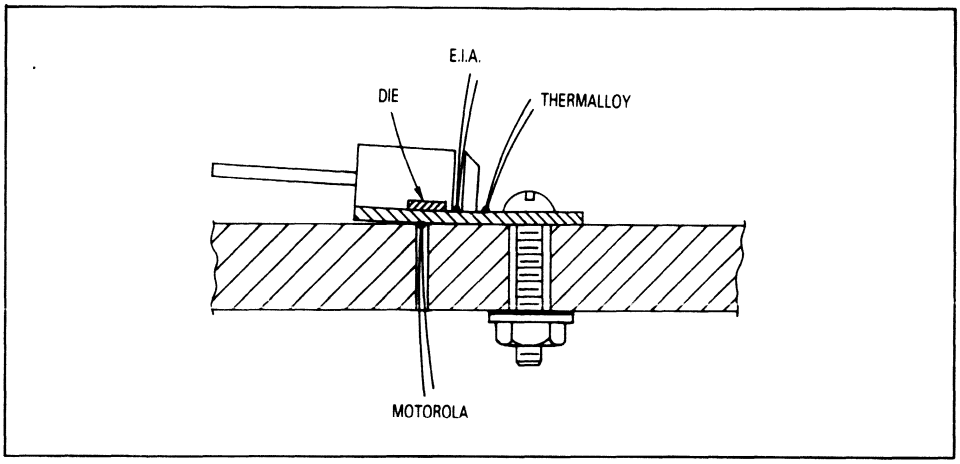
Measuring the interface thermal resistance $R\theta_{CS}$ appears deceptively simple. All that's apparently needed is a thermocouple on the semiconductor case, a thermocouple on the heatsink, and a means of applying and measuring DC power. However, $R\theta_{CS}$ is proportional to the amount of contact area between the surfaces and consequently is affected by surface flatness and finish and the amount of pressure on the surfaces. The fastening method may also be a factor. In addition, placement of the thermocouples can have a significant influence upon the results. Consequently, values for interface thermal resistance presented by different manufacturers are not in good agreement. Fastening methods and thermocouple locations are considered in this Appendix.

When fastening the test package in place with screws, thermal conduction may take place through the screws, for example, from the flange ear on a TO-204AA package directly to the heatsink. This shunt path yields values which are artificially low for the insulation material and dependent upon screw head contact area and screw material. MIL-I-49456 allows screws to be used in tests for interface thermal resistance probably because it can be argued that this is "application oriented."

Thermalloy takes pains to insulate all possible shunt conduction paths in order to more accurately evaluate insulation materials. The Motorola fixture uses an insulated clamp arrangement to secure the package which also does not provide a conduction path.

As described previously, some packages, such as a TO-220, may be mounted with either a screw through the tab or a clip bearing on the plastic body. These two methods often yield different values for interface thermal resistance. Another discrepancy can occur if the top of the package is exposed to the ambient air where radiation and convection can take place. To avoid this, the package should be covered with insulating foam. It has been estimated that a 15 to 20% error in $R\theta CS$ can be incurred from this source.

Another significant cause for measurement discrepancies is the placement of the thermocouple to measure the semiconductor case temperature. Consider the TO-220 package shown in Figure B1. The mounting pressure at one end causes the other end — where the die is located — to lift off the mounting surface slightly. To improve contact, Motorola TO-220 Packages are slightly concave. Use of a spreader bar under the screw lessens the lifting, but some is inevitable with a package of this structure. Three thermocouple locations are shown:



B-1. JEDEC TO-220 Package Mounted to Heatsink Showing Various Thermocouple Locations and Lifting Caused by Pressure at One End

a. The Motorola location is directly under the die reached through a hole in the heatsink. The thermocouple is held in place by a spring which forces the thermocouple into intimate contact with the bottom of the semi's case.

b. The JEDEC location is close to the die on the top surface of the package base reached through a blind hole drilled through the molded body. The thermocouple is swaged in place.

c. The Thermalloy location is on the top portion of the tab between the molded body and the mounting screw. The thermocouple is soldered into position.

Temperatures at the three locations are generally not the same. Consider the situation depicted in the figure. Because the only area of direct contact is around the mounting screw, nearly all the heat travels horizontally along the tab from the die to the contact area. Consequently, the temperature at the JEDEC location is hotter than at the Thermalloy location and the Motorola location is even hotter.

Since junction-to-sink thermal resistance must be constant for a given test setup, the calculated junction-to-case thermal resistance values decrease and case-to-sink values increase as the "case" temperature thermocouple readings become warmer. Thus the choice of reference point for the "case" temperature is quite important.

There are examples where the relationship between the thermocouple temperatures are different from the previous situation. If a mica washer with grease is installed between the semiconductor package and the heatsink, tightening the screw will not bow the package; instead, the mica will be deformed. The primary heat conduction path is from the die through the mica to the heatsink. In this case, a small temperature drop will exist across the vertical dimension of the package mounting base so that the thermocouple at the EIA location will be the hottest. The thermocouple temperature at the Thermalloy location will be lower but close to the temperature at the EIA location as the lateral heat flow is generally small. The Motorola location will be coolest.

The EIA location is chosen to obtain the highest temperature on the case. It is of significance because power ratings are supposed to be based on this reference point. Unfortunately, the placement of the thermocouple is tedious and leaves the semiconductor in a condition unfit for sale.

The Motorola location is chosen to obtain the highest temperature of the case at a point where, hopefully, the case is making contact to the heatsink. Once the special heatsink to accommodate the thermocouple has been fabricated, this method lends itself to production testing and does not mark the device. However, this location is not easily accessible to the user.

The Thermalloy location is convenient and is often chosen by equipment manufacturers. However, it also blemishes the case and may yield results differing up to 1°C/W for a TO-220 package mounted to a heatsink without thermal grease and no insulator. This error is small when compared to the thermal resistance of heat dissipaters often used with this package, since power dissipation is usually a few watts. When compared to the specified junction-to-case values of some of the higher power semiconductors becoming available, however, the difference becomes significant and it is important that the semiconductor manufacturer and equipment manufacturer use the same reference point.

Another EIA method of establishing reference temperatures utilizes a soft copper washer (thermal grease is used) between the semiconductor package and the heatsink. The washer is flat to within 1 mil/inch, has a finish better than 63 μ-inch, and has an imbedded thermocouple near its center. This reference includes the interface resistance under nearly ideal conditions and is therefore application-oriented. It is also easy to use but has not become widely accepted.

A good way to improve confidence in the choice of case reference point is to also test for junction-to-case thermal resistance while testing for interface thermal resistance. If the junction-to-case values remain relatively constant as insulators are changed, torque varied, etc., then the case reference point is satisfactory.

SECTION 6
LINEAR REGULATOR DESIGN EXAMPLE

As an illustration of the use of the material contained in the preceeding sections, the following regulator design example is given.

Regulator Performance Requirements

Output Voltage, $V_O = +10V \pm .1V$

Output Current, Io = 1A, current limited

Load Regulation, $\leq .1\%$ for Io = 10mA to 750mA

Line Regulation, $\leq .1\%$

Output ripple, $\leq$ 2mV p-p

Max Ambient Temperature, $T_A \leq +70°C$

Supply will have common loads to a negative supply

1. IC Regulator Selection: Study of the available regulators given in the selection guide of Section 17 reveals that the MC1723C would meet the regulation performance requirements. This regulator must be current boosted to obtain the required 1A output current. A rough cost estimate shows that an MC1723C/ series pass element combination is the most economical approach.

2. Circuit Configuration: In Section 3, an appropriate circuit configuration is found. This is the MC1723 NPN boost configuration of Figure 3-4A.

3. Determination of Component Values: Using the equations given in Figure 3-4A, the values of C_{REF}, R1, R2, R3 and R_{SC} are determined.

a. C_{REF} is chosen to be $0.1\mu F$ for low noise operation.

b. R1 + R2 is chosen to be $\approx$ 10K.

c. R2 is then given by: $R2 \approx \frac{7v}{V_o}(R1 + R2) = .7\ (10K) = 7K$

d. Since V_{REF} can vary by as much as $\pm$ 5% for the MC1723C, R2 should be made variable by at least that much, so that Vo can be set to the required value of $+10V \pm .1V$. R2 is therefore chosen to consist of a 62K resistor and a 2K trimpot.

e. R1 = 10K − R2 = 10K − 7K = 3K

f. $R_{SC} \approx \frac{0.6V}{Isc} = \frac{0.6V}{1A} = .6\Omega;\ .56\Omega$, 1W chosen for R_{SC}.

g. R3 = R1 || R2 $\cong$ 2.2K

4. Determination of Input Voltage, V_{IN}: There are two basic constraints on the input voltage: (1) the device limits for minimum and maximum V_{IN} and (2) the minimum input-output voltage differential. These limits are found on the device data sheet (Section 18.) to be:

$$9.5V \leq V_{IN} \leq 40V \text{ and } (V_{IN} - V_O) \geq 3V$$

For the configuration of Figure 3-5A, ($V_{IN} - V_O$) is given by:

$$(V_{IN} - V_O) = [V_{IN} - (V_O + 2\phi)] \geq 3V \text{ where } \phi = V_{BEON} \approx 0.6V$$

Note that ($V_{IN} - V_O$) is defined on the device data sheet to be the differential between the input and output pins. Since the base-emitter junction drops of Q1 and Rsc have been added to the circuit, they must be added to the minimum value of ($V_{IN} - V_O$). Therefore,

$$V_{IN} \geq V_O + 2\phi + 3V = 10 + 1.2 + 3$$

$$V_{IN} \geq 14.2V$$

This condition also satisfies the requirement for a minimum V_{IN} of 9.5V.

b. In order to simplify the design of the input supply (see Section 8), V_{IN} is chosen to be 16V average with a 3V p-p ripple at full load and up to 25V at no load. This assures that the input voltage is always above the required minimum value of 14.2V. Now, the output ripple can be determined. The MC1723C has a typical ripple rejection ratio of −74 db, as given on its data sheet. With an input ripple of 3V p-p, the output ripple would be less than 1m V p-p, which meets the regulator output ripple requirements.

5. Determination of regulator package and available output current: Referring to the MC1723 data sheet (Section 18), there are two package styles to choose from. Since the two packages have different thermal characteristics, the amount of available output current will be different for each.

This can be found from:

$$T_J = T_A + \theta_{JA} P_D \text{ (Eq. 6.1 from Section 15)}$$

where θ_{JA} = heatsink and/or pkg total junction-to-ambient thermal resistance

$P_D = V_{IN} \times (I_O + I_{IB})$

I_{IB} = quiescent current of IC regulator

I_O = IC regulator output current

solving for I_O:

$$I_O = \left[\frac{(T_J - T_A)}{\theta_{JA} V_{IN}}\right] - I_{IB} \qquad (6.1)$$

From the device data sheet, we can find the values of T_J, θ_{JA}, and I_{IB}. Eq 6.1 can then be solved. The results are summarized below for an unheatsinked MC1723CL (ceramic DIP), an unheatsinked MC1723CG (metal can), and an infinitely heatsinked MC1723CG packages.

TABLE 6-1

	MC1723CL	MC1723CG	MC1723CG
Heatsink	**None**	**None**	**Infinite**
T_J	175°C	150°C	150°C
T_A	70°C	70°C	70°C
θ_{JA}	150°C/W	184°C/W	70°C/W
I_{IB}	4mA	4mA	4mA
I_O	40mA	23mA	67mA

A choice must now be made. Since it is desirable to have as much available current as possible to drive Q1 (thereby lowering its gain (h_{fe}) requirements), an infinitely heatsinked MC1723CG is the most desirable choice. However, the construction of an infinite heatsink is hardly practical. Therefore, the choice is between an unheatsinked MC1723CL and an MC1723CG with some form of heatsinking. The unheatsinked MC1723CL is chosen since this approach is the least complex.

6. Selection of the Series Pass Element, Q1: The transistor type chosen for Q1 must have the following characteristics (see Section 4):

a. $V_{CEO} \geq V_{INMAX}$

b. $I_{CMAX} \geq I_{SC}$

c. $h_{fe} \geq \frac{I_{SC}}{I_O}$ @ $V_{CE} = V_{IN} - V_O - \phi$

where $\phi = V_{BEON} \approx 0.6V$

d. $P_{DMAX} \geq V_{IN}, \times I_{SC}$

e. θ_{JC} such to allow practical heatsinking

f. SOA such that it can withstand

$$V_{CE} = V_{IN} \text{ @ } I_C = I_{SC}$$

for this example:

$V_{CEO} \geq 25V$

$I_{CMAX} \geq 1A$

$h_{fe} \geq 25$ @ $V_{CE} = 5V$ @ $I_C = 1A$

$P_{DMAX} \geq 16W$

$\theta_{JC} = 1.52°C/W$

SOA: 1A @ 16V

A 2N3055 transistor is chosen as a suitable device for Q1 using the selection guide of Section 4 and the transistor data sheets (available from device manufacturer).

7. Q1 Heatsink Calculation

$$T_J = T_A + \theta_{JA} P_D \text{ (Eq 15.1 from Section 15)}$$

where $P_D = V_{IN} \times I_{SC}$

$$\theta_{JA} = \theta_{JC} + \theta_{CS} + \theta_{SA} \text{ (Eq 6.2)}$$

solving for θ_{SA}:

$$\theta_{SA} = \left[\frac{T_J - T_A}{P_D}\right] - (\theta_{JC} + \theta_{CS}) \qquad (6.2)$$

From the 2N3055 data sheet, $T_J = 200°C$ and $\theta_{JC} = 1.52°C/W$. The transistor will be mounted with thermal grease directly to the heatsink. Therefore, θ_{CS} is found to be 0.1°C/W from Table 15-1.

Solving 6.2:

$$\theta_{SA} = \left[\frac{200°C - 70°C}{16V \times 1A}\right] - (1.52 + 0.1)\,°C/W$$

$$\leq 6.6°C/W$$

A commercial heatsink is now chosen from Table 15-2 or a custom designed using the methods given in Section 15. For this example, a thermalloy 6003 heatsink having a θcs of 6.2°C/W was used.

8. Clamp Diode: Since the regulator can power a load which is also connected to a negative supply, a 1N4001 diode is connected to the output for protection. (See general design considerations, Section 3H.) The complete circuit schematic is shown in Figure 6-1.

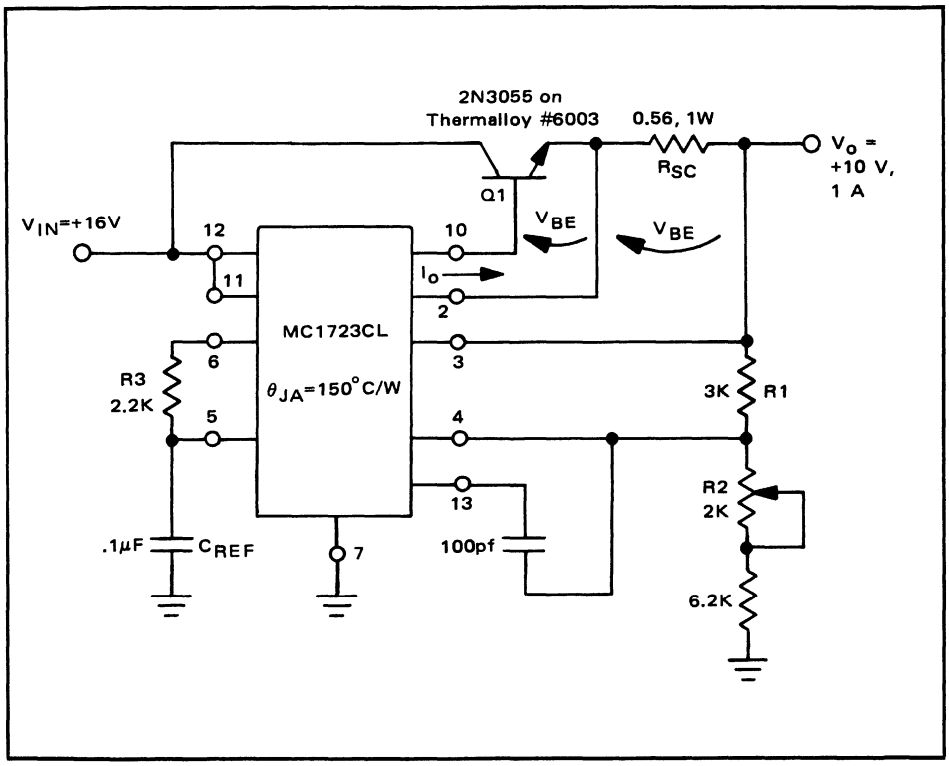


Figure 6-1. +10V, 1A Design Example

9. Construction Input Supply Design: The input supply is now designed using the information contained in Section 8 and the regulator circuit is constructed using the guidelines given in Section 5.

SECTION 7

LINEAR REGULATOR CIRCUIT TROUBLESHOOTING CHECKLIST

Occasionally the designer's prototype regulator circuit will not operate properly. If problems do occur, the trouble can be traced to a design error in 99.9% of the cases. As a troubleshooting aid to the designer, the following guide is presented.

Of course, it would be difficult, if not impossible, to devise a troubleshooting guide which would cover all possible situations. However, the checklist provided will help the designer pinpoint the problem in the majority of cases. To use the guide, first locate the problem's symptom(s) and then carefully recheck the regulator design in the area indicated using the information contained in the referenced handbook section.

SYMPTOM	DESIGN AREA TO CHECK	REFER TO SECTION
Regulator Oscillates	1. Layout	5
	2. Compensation capacitor too small	3, 18
	3. Input leads not bypassed	5
	4. External pass element parasitically oscillating	5
Loss of Regulation at Light Loads	1. Emitter-Base resistor in "PNP" type boost configuration too large	4
	2. Absence of 1 mA "minimum" load (see load regulation test spec on device data sheet)	18
	3. Improper circuit configuration	3
Loss of Regulation at Heavy Loads	1. Input Voltage too low (V_{INMIN}, $\lvert V_{IN} - V_O \rvert_{MIN}$)	2, 3, 18 17
	2. External pass element gain too low	4
	3. Current limit too low	3
	4. Line resistance between sense points and load	5
	5. Inadequate heatsinking	15
IC Regulator or Pass Element Fails after Warm-Up or at High T_A	1. Inadequate heatsinking	15
	2. Input Voltage Transient (V_{INMAX}, V_{CEO})	2, 4, 5, 17, 18
Pass Element Fails During Short Circuit	1. Insufficient pass element ratings (SOA, I_{CMAX})	4
	2. Inadequate heatsinking	15

TROUBLESHOOTING CHECKLIST

SYMPTOM	DESIGN AREA TO CHECK	REFER TO SECTION
IC Regulator Fails During Short Circuit	1. IC current or SOA capability exceeded 2. Inadequate heatsinking	2, 18
IC Regulator Fails During Power Up	1. Input voltage transient (V_{INMAX}) 2. IC current or SOA capability exceeded as load (capacitor) is charged up.	2, 18 2, 18
IC Regulator Fails During Power-Down	1. Regulator reverse biased	3
Output Voltage Does Not Come Up During Power-Up or After Short Circuit	1. Output polarity reversal 2. Load has "latched-up" in some manner (usually seen with op amps, current sources, etc.)	3
Excessive 60 or 120 Hz Output Ripple	1. Input supply filter capacitor ground loop	5

If, after carefully rechecking the circuit, the designer is not successful in resolving the problem, seek assistance from the factory by contacting the nearest Motorola Sales office.

SECTION 8
DESIGNING THE INPUT SUPPLY

Most input supplies used to power series pass regulator circuits consist of a 60 Hz, single phase step-down transformer followed by a rectifier circuit whose output is smoothed by a choke or capacitor input filter. The type of rectifier circuit used can be either a half-wave, full-wave, or full-wave bridge type, as shown in Figure 8-1. The half-wave circuit is used in low current applications, while the full-wave is preferrable in high-current, low output voltage cases. The full-wave bridge is usually used in all other high-current applications.

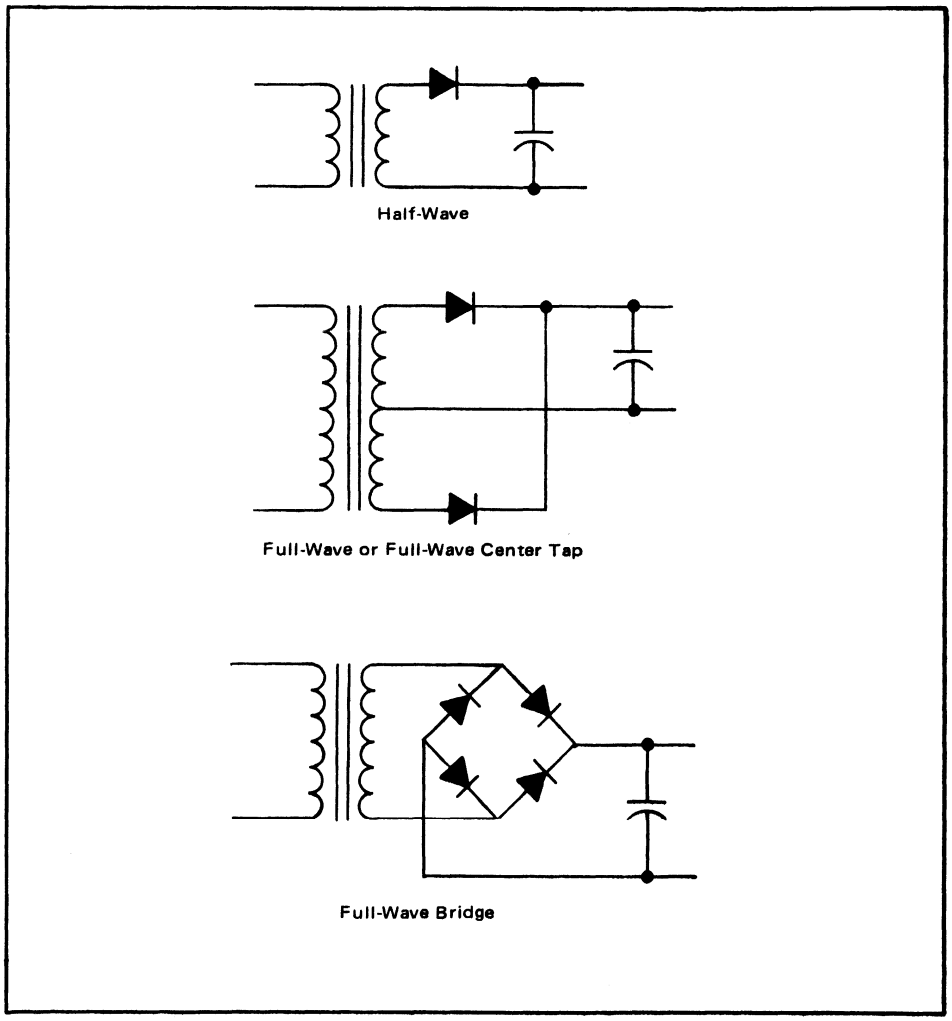


Figure 8-1. Rectification Schemes

In this section, specification of the filter capacitor, rectifier and transformer ratings will be discussed. The specifications for the choke input filter will not be considered since the simpler capacitor input type is more commonly used in series regulated circuits. A detailed description of this type of filter can be found in the reference listed at the end of this section.

1. Design of Capacitor-Input Filters

The best practical procedure for the design of capacitor-input filters still remains based on the graphical data presented by Schade[1] in 1943. The curves shown in Figures 8-2 through 8-5 give all the required design information for half-wave and full-wave rectifier circuits. Whereas Schade originally also gave curves for the impedance of vacuum-tube rectifiers, the equivalent values for semiconductor diodes must be substituted. However, the rectifier forward drop often assumes more significance than the dynamic resistance in low-voltage supply applications, as the dynamic resistance can generally be neglected when compared with the sum of the transformer secondary-winding resistance plus the reflected primary-winding resistance. The forward drop may be of considerable importance, however, since it is about 1 V, which clearly cannot be ignored in supplies of 12 V or less.

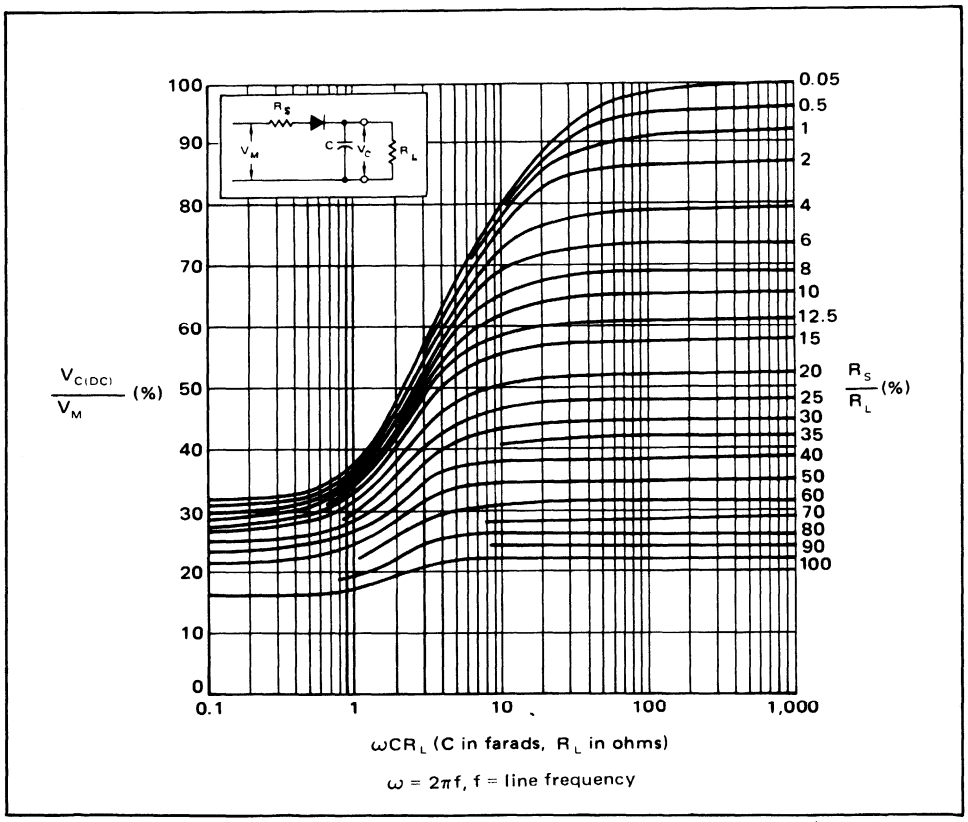


Figure 8-2. Relation of applied alternating peak voltage to direct output voltage in half-wave capacitor-input circuits. *(From O. H. Schade, Proc. IRE, vol. 31, p. 356, 1943.)*

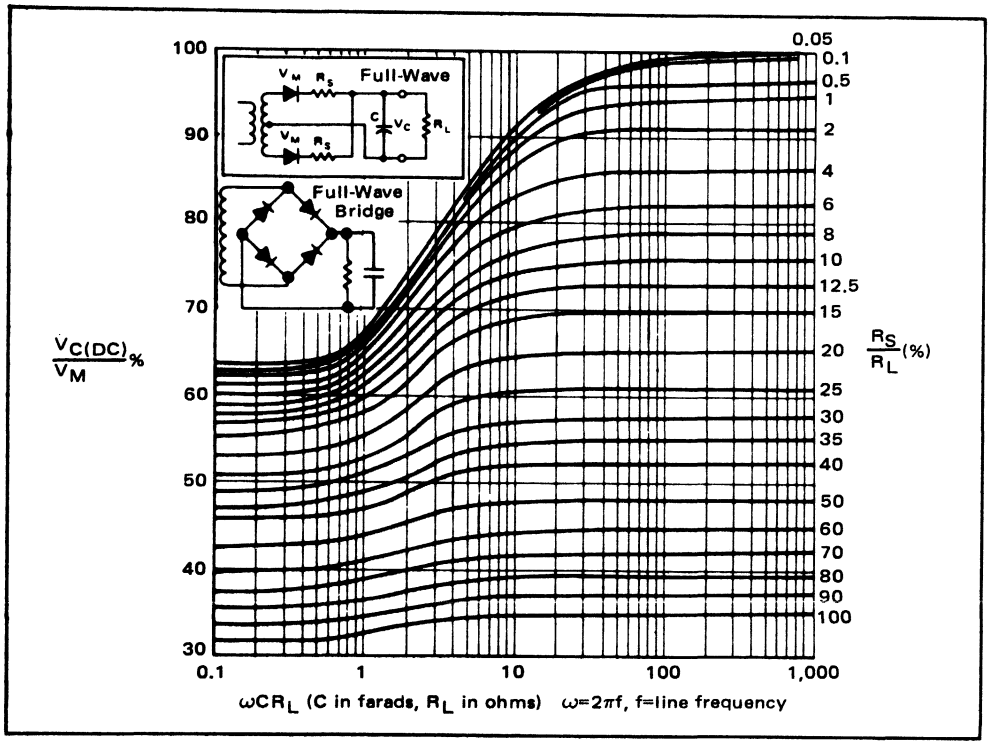


Figure 8-3. Relation of applied alternating peak voltage to direct output voltage in full-wave capacitor-input circuits. *(From O. H. Schade, Proc. IRE, vol. 31, p. 356, 1943.)*

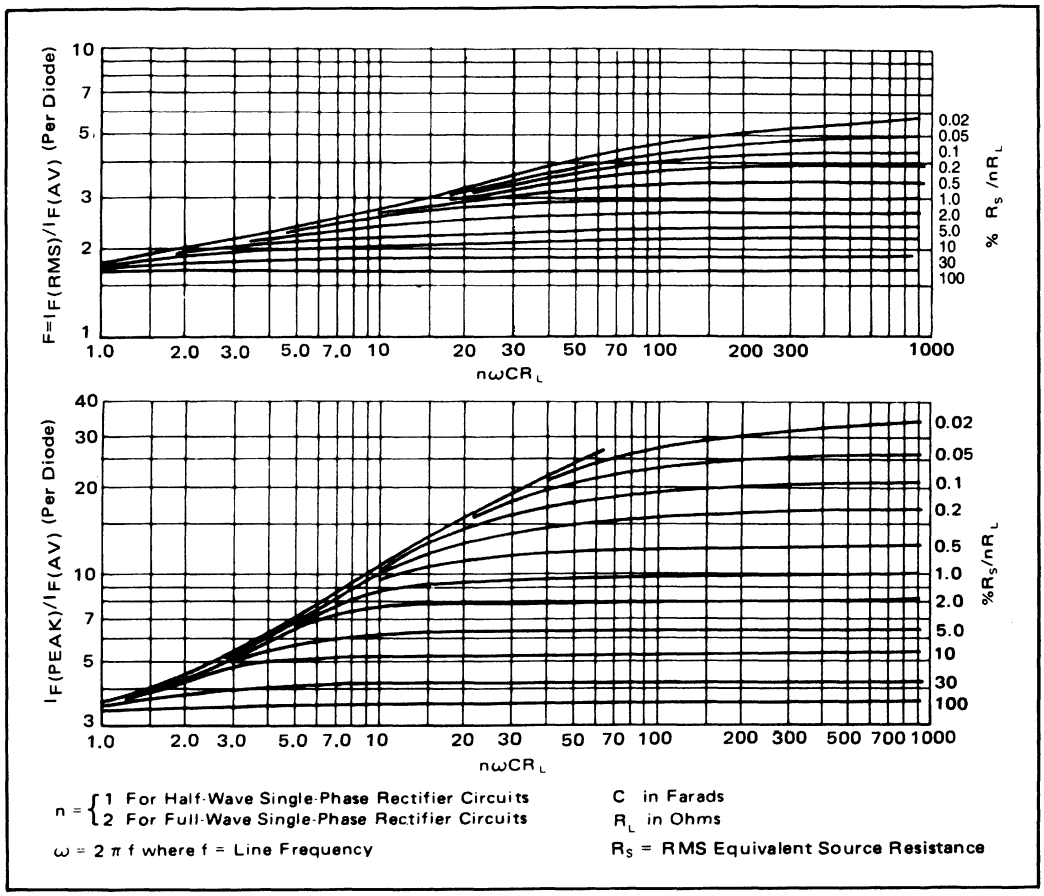


Figure 8-4. Relation of RMS and peak to average diode current in capacitor-input circuits.
(From O. H. Schade, Proc. IRE, vol. 31, p. 356, 1943.)

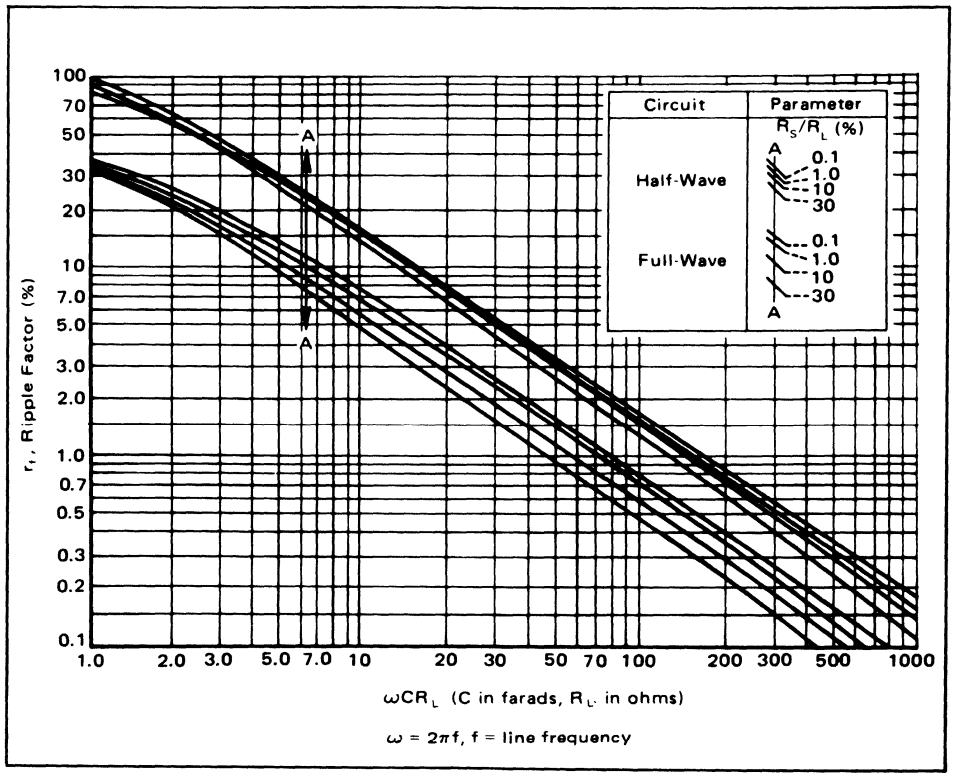


Figure 8-5. Root-mean-square ripple voltage for capacitor-input circuits. *(From O H Schade, Proc. IRE, vol. 31, p. 356, 1943.)*

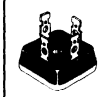
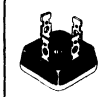
Returning to the above curves, the full-wave circuit will be considered. Figure 8-3 shows that a circuit must operate with $\omega CR_L \geq 10$ in order to hold the voltage reduction to less than 10 percent and $\omega CR_L \geq 40$ to obtain less than 2 percent reduction. However, it will also be seen that these voltage-reduction figures require Rs/RL, where Rs is now the total series resistance, to be about 0.1% which, if attainable, causes repetitive peak-to-average current ratios from 10 to 17 respectively, as can be seen from Figure 8-4. These ratios can be satisfied by many diodes; however, they may not be able to tolerate the turn-on surge current generated when the input-filter capacitor is discharged and the transformer primary is energized at the peak of the input waveform. The rectifier is then required to pass a surge current determined by the peak secondary voltage less the rectifier forward drop and limited only by the series resistance Rs. In order to control this turn-on surge, additional resistance must often be provided in series with each rectifier. It becomes evident, then, that a compromise must be made between voltage reduction on the one hand and diode surge rating and hence average current-carrying capacity on the other hand. If small voltage reduction, that is good voltage regulation, is required, a much larger diode is necessary than that demanded by the average current rating.

Surge Current

The capacitor-input filter allows a large surge to develop, because the reactance of the transformer leakage inductance is rather small. The maximum instantaneous surge current is approximately V_M/R_s and the capacitor charges with a time constant $\tau \approx R_s C_1$. As a rough — but conservative — check, the surge will not damage the diode if V_M/R_s is less than the diode I_{FSM} rating and τ is less than 8.3 ms. It is wise to make Rs as large as possible and not pursue tight voltage regulation; therefore, not only will the surge be reduced but rectifier and transformer ratings will more nearly approach the dc power requirements of the supply.

As an aid in the selection of a suitable rectifier or bridge, the brief selection guide of Table 8-1 is included.

TABLE 8-1

	Io, AVERAGE RECTIFIED FORWARD CURRENT (Amperes) Io, DC OUTPUT CURRENT							
	1.0	1.5	3.0			6.0	25	35
	59-04 (DO-15) Plastic		60 Metal	267 Plastic		194-04 Plastic	309A-03	309A-02
								
V_{RRM} (Volts)								
50	†1N4001	**1N5391	1N4719	**MR500	1N5400	**MR750	MDA2500	MDA3500
100	†1N4002	**1N5392	1N4720	**MR501	1N5401	**MR751	MDA2501	MDA3501
200	†1N4003	1N5393 *MR5059	1N4721	**MR502	1N5402	**MR752	MDA2502	MDA3502
400	†1N4004	1N5395 *MR5060	1N4722	**MR504	1N5404	**MR754	MDA2504	MDA3504
600	†1N4005	1N5397 *MR5061	1N4723	**MR506	1N5406	**MR756	MDA2506	MDA3506
800	†1N4006	1N5398	1N4724	MR508		MR758		MDA3508
1000	†1N4007	1N5399	1N4725	MR510		MR760		MDA3510
I_{FSM} (Amps)	30	50	300	100	200	400	400	400
T_A @ Rated Io (°C)	75	T_L = 70	75	95	T_L = 105	60		
Tc @ Rated Io (°C)							55	55
T_J (Max) (°C)	175	175	175	175	175	175	175	175

Dimensions given are nominal

† Package Size: 0.120" Max Diameter by 0.260" Max Length.
* 1N5059 series equivalent Avalanche Rectifiers.
** Avalanche versions available, consult factory.

2. Design Procedure

A. From the regulator circuit design (see Section 6), we know:

$V_{C(DC)}$ = The required full load average DC output voltage of the capacitor input filter

$V_{Ripple(p\text{-}p)}$ = the maximum full load peak-to-peak ripple voltage

V_m = the maximum no load output voltage

I_o = the full-load filter output current

f = the input AC line frequency

B. From Figure 8-5, we can determine a range of minimum capacitor values to obtain sufficient ripple attenuation. First determine r_f:

$$r_f = \frac{V_{Ripple(p\text{-}p)}}{2\sqrt{2}\,V_{C(DC)}} \times 100\% \tag{8.1}$$

a range for ωCR_L can now be found from Figure 8-5.

C. Next, determine the range of R_S/R_L from Figure 8-2 or 8-3 using $V_{C(DC)}$ and the values for ωCR_L found in part B. If the range of ωCR_L values initially determined from Figure 8-5 is above $\simeq$ 10, R_S/R_L can be found from Figures 8-2 and 8-3 using the lowest ωCR_L value. Otherwise, several iterations between Figures 8-2 or 8-3 and 8-5 may be necessary before an exact solution for R_S/R_L and ωCR_L for a given r_f and $V_{C(DC)}/V_m$ can be found.

D. Once ωCR_L is found, the value of the filter capacitor, C, can be determined from:

$$C = \frac{\omega CR_L}{2\pi f\left(\frac{V_{C(DC)}}{I_O}\right)} \tag{8.2}$$

E. The rectifier requirements may now be determined:

1. Average Current Per Diode

$$I_{F(AVG)} = I_o \text{ for half-wave rectification} \tag{8.3}$$
$$= I_o/2 \text{ for full-wave rectification}$$

2. RMS and Peak repetitive rectifier current ratings can be determined from Figure 8-4.

3. The rectifier PIV rating is 2 V_m for the half-wave and full wave circuits, V_m for the full-wave bridge circuit. In addition, a minimum safety margin of 20% to 50% is advisable due to the possibility of line transients.

4. Maximum Surge Current

$$I_{SURGE} = V_m/(R_S + ESR) \tag{8.4}$$

where ESR = minimum equivalent series resistance of filter capacitor from its data sheet

F. Transformer Specification

1. Secondary Leg RMS Voltage

$$V_S = \{V_m + (n)\ 1.0\}/\sqrt{2} \tag{8.5}$$

where $n = 1$ for half-wave and full-wave

$n = 2$ for full-wave bridge

2. Total resistance of secondary and any external resistors to be equal to Rs found from Figures 8-2, -3, and -4 (see Part C).

3. Secondary RMS Current

$$\begin{aligned} \text{Half-Wave} &= I_{rms} \\ \text{Full-Wave} &= I_{rms} \\ \text{Full-Wave Bridge} &= \sqrt{2}\, I_{rms} \end{aligned} \tag{8.6}$$

where I_{rms} = rms rectifier current (from part E.1 and E.2).

4. Transformer VA rating

$$\begin{aligned} \text{Half-Wave} &= V_S\, I_{rms} \\ \text{Full-Wave} &= 2\, V_S\, I_{rms} \\ \text{Full-Wave Bridge} &= V_S\, I_{rms}\, (\sqrt{2}) \end{aligned} \tag{8.7}$$

where I_{rms} = rms rectifier current (from part E.1 and E.2)

and V_S = Secondary Leg RMS Voltage

3. Design Example

A. Find the values for the filter capacitor, transformer rectifier ratings, given:

Full-Wave Bridge Rectification

$$\begin{aligned} V_{C(DC)} &= 16V \\ V_{RIPPLE\ (p\text{-}p)} &= 3\ V \\ V_M &= 25\ V \\ I_o &= 1\ A \\ f &= 60\ Hz \end{aligned}$$

B. Using Equation (8.1)

$$r_f = \frac{3}{2\sqrt{2}\,(16)} \times 100\% = 6.6\%$$

from Figure 8-5, $\omega C R_L \simeq 7$ to 15

C. Using $\omega CR_L = 10$, R_S/R_L is found from Figure 8-3 using:

$$\frac{V_{C(DC)}}{V_M} = \frac{16}{25} = .64 = 64\%$$

$$\therefore R_S/R_L = 20\% \text{ or } R_S = .2 \times R_L = .2\left(\frac{V_{C(DC)}}{I_O}\right) = .2\ (16)$$

$$R_S = 3.2\ \Omega$$

D. From Equation (8.2), the filter capacitor size is found:

$$C = \frac{\omega C R_L}{2\pi f\left(\frac{V_{C(DC)}}{I_O}\right)} = \frac{10}{2\pi(60)16} = 1658\ \mu F$$

E. The rectifier ratings are now specified:

1. $I_{F(AVG)} = I_O/2 = 0.5$ A from Eq (8.3)
2. $I_{F(RMS)} = 2 \times I_{F(AVG)} = 1$ A from Fig. 8-4
3. $I_{F(PEAK)} = 5.2 \times I_{F(AVG)} = 2.6$ A from Fig. 8-4
4. PIV = $V_M = 25$ V (use 50 V for safety margin)
5. $I_{SURGE} = V_M/(R_S + ESR) \simeq 25/3.2 = 7.8$ A from Eq (8.4) (neglecting capacitor ESR)

F. The transformer should have the following ratings:

1. $V_S = \{V_M + n(1.0)\}/\sqrt{2} = (25 + 2)/\sqrt{2} = 19$ VRMS {from Eq (8.5)}
2. Secondary Resistance should be 3.2 Ω.
3. Secondary RMS current rating should be 1.4 A {from Eq (8.6)}
4. From Eq. (8.7), the transformer should have a 27 VA rating.

It should be noted that, in order to simplify the procedure, the above design does not allow for line voltage variations or component tolerances. The designer should take these factors into account when designing his input supply. Typical tolerances would be: Line Voltage = +10% to −15% and Filter Capacitors = +75% to −10%.

REFERENCES

1. O. H. Schaade, Proc. IRE, Vol. 31, 1943.
2. Motorola Silicon Rectifier Manual, 1980.

SECTION 9
AN INTRODUCTION TO SWITCHING POWER SUPPLIES

The Switching Power Supply continues to increase in popularity and is one of the fastest growing markets in the world of power conversion. Its performance and size advantages meet the needs of today's modern and compact electronic equipment and the increasing variety of components directed at these applications makes new designs even more practical.

This guide is intended to provide the designer with an overview of the more popular inverter circuits, their basic theory of operation, and some of the subtle characteristics involved in selecting a circuit and the appropriate components. Also included are valuable design tips on both the major passive and active components needed for a successful design. Finally, a complete set of selector guides to Motorola's Switchmode components is provided which gives a detailed listing of the industry's most comprehensive line of semiconductor products for switching power supplies.

Comparison with Linear Regulators

The primary advantages of a switching power supply are efficiency, size, and weight. It is also a more complex design, cannot meet some of the performance capabilities of linear supplies and generates a considerable amount of electrical noise. However switchers are being accepted in the industry, particularly where size and efficiency are of prime importance. Performance continues to improve and for most applications they are usually cost competitive down to the 20 W power level.

In the past the switcher's advantage versus the linear regulator was in the high power arena where passive components such as transformers and filters were small compared to the linear regulator at the same power level. However, active component count was high and tended to make the switcher less cost effective at low power levels. In recent years, switchers have been significantly cost reduced because designers have been able to simplify the control circuits with new, cost effective integrated circuits and have found even lower cost alternatives in the passive component area.

A performance comparison chart of switching versus linear supplies is shown in Table 9-1. Switcher efficiencies run from 70 to 80% but occasionally fall to (60–65%) when linear post regulators are used for the auxiliary outputs. Some linear power supplies on the other hand, are operated with up to 50% efficiency but these are areas where line variations or hold-up time problems are minimal. Most linears operate with typical efficiencies of only 30%. The overall size reduction of a 20 kHz switcher is about 4:1 and newer designs in the 100 to 200 kHz region end up at about 8:1 (versus a linear). Other characteristics such as static regulation specs are comparable, while ripple and load transient response are usually worse. Output noise specs can be somewhat misleading. Very often a 500 mV switching spike at the output may be attenuated considerably at the

TABLE 9-1. 20 kHz Switcher versus Linear Performance

Parameter	Switcher	Linear
Efficiency	75%	30%
Size	2 W/IN^3	0.5 W/IN^3
Weight	40 W/lb.	10 W/lb.
Line and Load Regulation	0.1%	0.1%
Output Ripple V_{P-P}	50 mV	5 mV
Noise V_{P-P}	50–200 mV	—
Transient Response	1 ms	20 μs
Hold-Up Time	20–30 ms	1–2 ms

load itself due to the series inductance of the connecting cables and the additional filter capacitors found in many logic circuits. In the future, the noise generated at higher switching frequencies (100–500 kHz) will probably be easier to filter and the transient response will be faster. Hold-up time is greater for switchers because it is easier to store energy in high voltage capacitors (200–400 V) than in the lower voltage (20–50 V) filter capacitors common to linear power supplies. This is due to the fact that the physical size of a capacitor is dependent on its CV product while energy storage is proportional to CV^2.

Basic Configurations

A switching power supply is a relatively complex circuit as is shown by the four basic building blocks of Figure 9-1. It is apparent here that the heart of the supply is really the high frequency inverter. It is here that the work of chopping the rectified line at a high frequency (20–200 kHz) is done. It is here also that the line voltage is transformed down to the correct output level for use by logic or other electronic circuits. The remaining blocks support this basic function. The 60 Hz input line is rectified and filtered by one block and after the inverter steps this voltage down, the output is again rectified and filtered by another. The task of regulating the output voltage is left to the control circuit which closes the loop from the output to the inverter. Most control circuits generate a fixed frequency internally and utilize pulse width modulation techniques to implement the desired regulation. Basically, the on-time of the square wave drive to the inverter is controlled by the output voltage. As load is removed or input voltage increases, the slight rise in output voltage will signal the control circuit to deliver shorter pulses to the inverter and conversely as the load is increased or input voltage decreases, wider pulses will be fed to the inverter.

The inverter configurations used in today's switchers actually evolved from the buck and boost circuits shown in Figures 9-2a and 9-2b. In each case the regulating means and loop analysis will remain the same but a transformer is added in order to provide electrical isolation between the line and load. The forward converter family which includes the push-pull and half bridge circuits evolved from the buck regulator (Figure 9-2a). And the newest switcher, the flyback converter, actually evolved from the boost regulator. The buck circuit interrupts the line and provides a variable pulse width square wave to a simple averaging LC filter. In this case, the first order approximation of the output voltage is $V_{out} = V_{in}$ x duty cycle and regulation is accomplished by simply varying the duty cycle. This is satisfactory for most analysis work and only the transformer turns ratio will have to be adjusted slightly to compensate for IR drops, diode drops, and transistor saturation voltages.

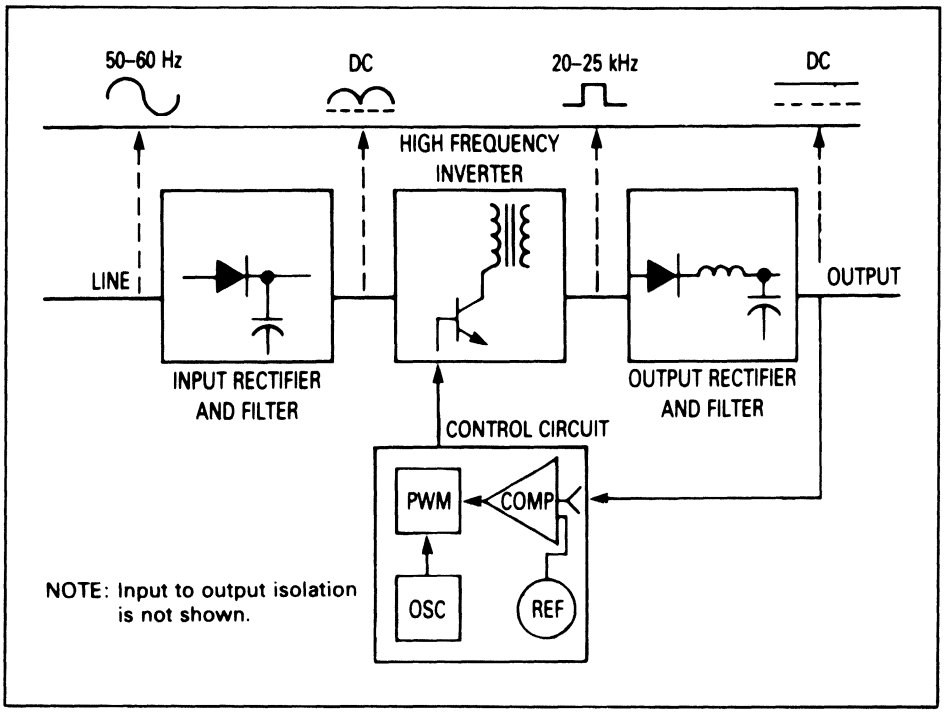


Figure 9-1. Functional Block Diagram — Switching Power Supply

Operation of the boost circuit is more subtle in that it first stores energy in a choke and then delivers this energy plus the input line to the load. However, the flyback regulators which evolved from this configuration delivers only the energy stored in the choke to the load. This method of operation is actually based on the buck boost model shown in Figure 9-2c. Here, when the switch is opened, only the stored inductive energy is delivered to the load. The true boost circuit can also regulate by stepping up (or boosting) the input voltage whereas the buck-

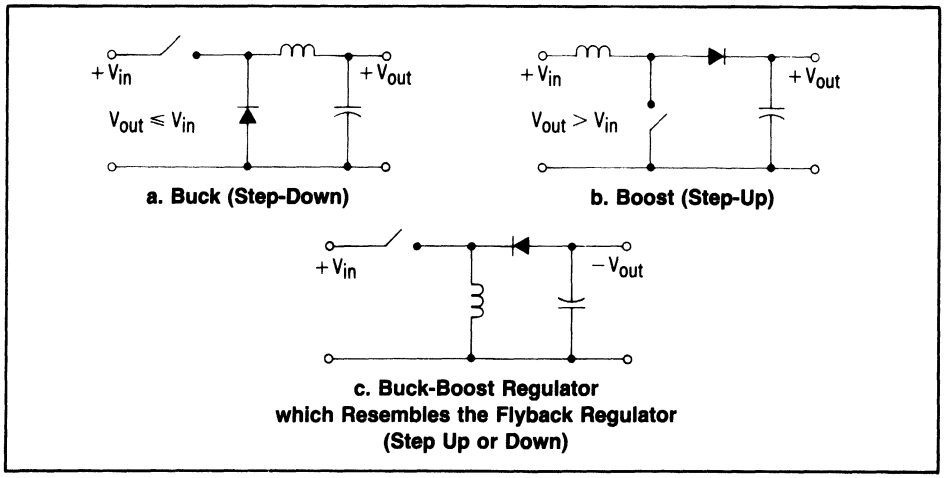


Figure 9-2. Nonisolated DC-DC Converters

boost or flyback regulator can step the input voltage up or down. Analysis of the boost regulator begins by dealing with the choke as an energy storage element which delivers a fixed amount of power to the load:

$$P_o = 1/2\ L\ I^2 f_o$$

where I = the peak choke current
f_o = the operating frequency
and L = the inductance

Because it delivers a fixed amount of power to the load regardless of load impedance (except for short circuits), the boost regulator is the designer's first choice in photoflash and capacitive-discharge (CD) automotive ignition circuits to recharge the capacitive load. It also makes a good battery charger. For an electronic circuit load, however, the load resistance must be known in order to determine the output voltage:

$$V_o = \sqrt{P_o R_L} = I \sqrt{\frac{L f_o R_L}{2}}$$

where R_L = The load resistance

In this case, the choke current is proportional to the on-time or duty cycle of the switch and regulation for fixed loads simply involves varying the duty cycle as before. However, the output also depends on the load which was not the case with buck regulators and results in a variation of loop gain with load.

For both regulators, transient response or responses to step changes in load are very difficult to analyze. They lead to what is termed a "load dump" problem. This requires that energy already stored in the choke or filter be provided with a place to go when load is abruptly removed. Practical solutions to this problem include limiting the minimum load and using the right amount of filter capacitance to give the regulator time to respond to this change.

The Future

The future offers a lot of growth potential for switchers in general and low power switchers (20–100 watts) in particular. The latter are responding to the growth in microprocessor based equipment as well as computer peripherals. Today's configurations have already been challenged by the sine wave inverter which reduces noise and improves transistor reliability but does effect a cost penalty. Also, a trend to higher switching frequencies to reduce size and cost even further has begun. The latest bipolar designs operate efficiently up to 100 kHz and the FET seems destined to own the 200 to 500 kHz range.

At this time there are a lot of safety and noise specifications. Originally governed only by MIL specs and the VDE in Europe, now both UL and the FCC have released a set of specifications that apply to electronic systems which often include switchers (see Table 9-2). It seems probable, however, that system engineers or power supply designers will be able to add the necessary line filters and EMI shields without evoking a significant cost penalty in the design.

The most optimistic note concerning switchers is in the component area. Switching power supply components have actually evolved from components used in similar applications. And it is very likely that newer and more mature products specifically for switchers will continue to appear over the next several

years. The ultimate effect of this evolution will be to further simplify, cost reduce and increase the reliability of these designs.

TABLE 9-2. SMPS Specifications

Specification	Area
VDE 0730	Safety
VDE 0806	Safety
VDE 0871	EMI
VDE 0875	EMI
MIL-STD-217D	Reliability
MIL-STD-461A	EMI
DOD-STD-1399	Harmonic Content
UL 478	Safety
FCC Class A & B	EMI
CSA C22.2	Safety
IEC 380	Safety

The synchronous rectifier is one example of a new component developed specifically for low voltage switchers. As requirements for 2 and 3 V supplies emerge for use by fine geometry VLSI chips, the only way to maintain decent conversion efficiency is to develop lower forward drop rectifiers. The differences in 3 and 5 V rectifier requirements are shown in Table 9-3. At this time, Motorola offers low V_F Schottky and area efficient TMOS III FETs for this task and is considering a variety of additional technology options. The direct approach involves using low V_F Schottkys or pinch rectifiers which will feature V_F's of 0.3 to 0.4 V. The indirect approach involves using FETs or bipolar transistors and slightly more complex circuitry like that shown in Figure 9-3. Both transistors will feature V_F's of 0.2 V and in addition the bipolar will have high EBO's (30 V) and high gain (100) with a recovery time of 100 ns.

TABLE 9-3. Synchronous Rectifier Requirements

Output Voltage	Rectifier Characteristics	
	V_F	V_R
5 V	0.5–1 V	30–60 V
3 V	0.3–0.6 V	20–40 V

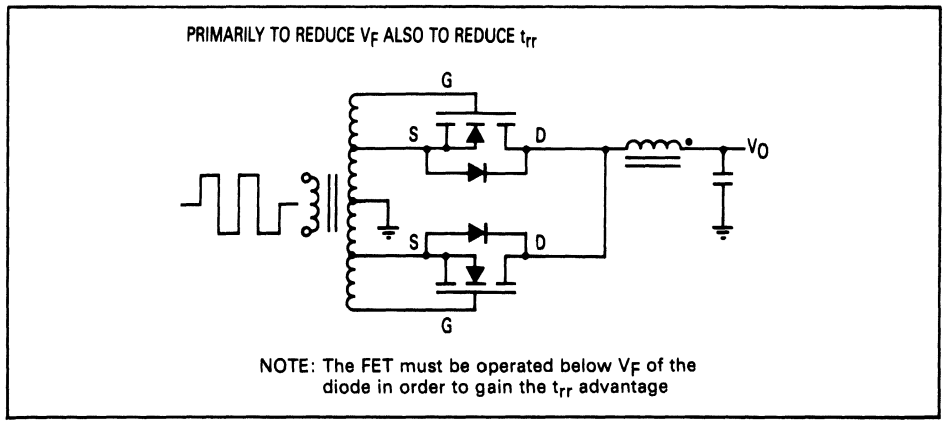


Figure 9-3. Synchronous Rectifiers for 3 Volt Power Supplies

And for designers who are not satisfied with the relatively low frequency limitations of square wave switchers, there is the SRPS. The series resonant power supply topology seems to offer the possibility of working in the 1 MHz region. If components like the relatively exotic power transformer can be cost reduced, then it will be possible for this topology to become dominant in the market. The features generally associated with this type of power supply are listed in Table 9-4 and a typical half bridge circuit is shown in Figure 9-4. In a design now being studied in Motorola's advanced products laboratory, standard FETs, Schottky's and ultrafast rectifiers all appear to work very well at 1 MHz.

TABLE 9-4. SRPS Features

Feature	Description
High Frequency	Today's line operated designs use sine waves in the 500 kHz to 1 MHz range.
Small Size	The ferrite transformer and polypropylene coupling capacitor are smaller than those found in lower frequency square wave designs.
Low Noise	Switching occurs at zero crossings which reduces component stress and lowers EMI.
Efficient	Because switching losses are reduced, efficiency is high (typically 80%).
High Peak to Average Current Ratios	Current ratings of the transistors and rectifiers are twice as high as similar flyback designs.
Special Control Circuit	PDM (density) rather than PWM (width) control is used and requires a control IC with a programmable VCO.
Market	The SRPS is expected to own 15% of the power supply market by 1990.

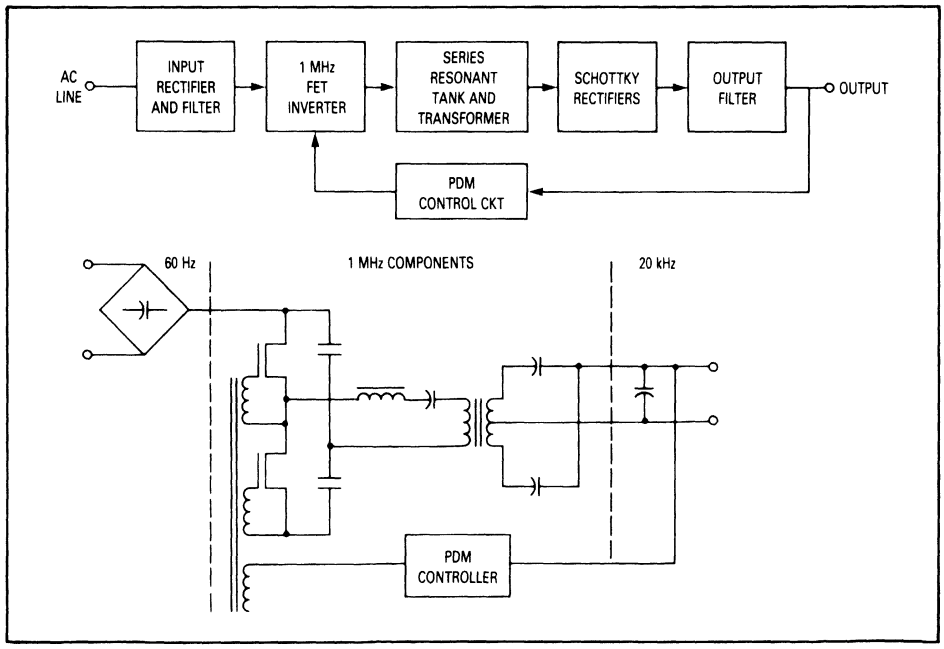


Figure 9-4. SRPS Block Diagram

SECTION 10
SWITCHING REGULATOR TOPOLOGIES

FET and Bipolar Drive Considerations

There are probably as many base drive circuits for bipolars as there are designers. Ideally, the transistor would like just enough forward drive (current) to stay in or near saturation and reverse drive that varies with the amount of stored base charge such as a low impedance reverse voltage. Many of today's common drive circuits are shown in Figure 10-1. The fixed drive circuits of 10a, b and c tend to emphasize economy, while the Baker clamp and proportional drive circuits of 10d and e emphasize performance over cost.

FET drive circuits are another alternative. The standard that has evolved at this time is shown in Figure 10-2A. This transformer coupled circuit will produce forward and reverse voltages applied to the FET gate which vary with the duty cycle as shown. For this example, a V_{GS} rating of 20 V would be adequate for the worst case condition of high logic supply (12 V) and minimum duty cycle. And yet, minimum gate drive levels of 10 V are still available with duty cycles up to 50%. If wide variations in duty cycle are anticipated, it might be wise to consider using a semi-regulated logic supply for these situations. Finally, one point that is not obvious when looking at the circuit is that FETs can be directly coupled to many ICs with only 100 mA of sink and source capability and still switch efficiently at 20 kHz. However, to achieve switching efficiently at higher frequencies, 1 to 2 amps of drive may be required on a pulsed basis in order to quickly charge and discharge the gate capacitances. A simple example will serve to illustrate this point and also show that the Miller effect, produced by C_{DG}, is the predominant speed limitation when switching high voltages (see Figure 10-2B). A FET responds instantaneously to changes in gate voltage and will begin to conduct when the threshold is reached (V_{GS} = 2 to 3 V) and be fully on with V_{GS} = 7 to 8 V. Gate waveforms will show a porch at a point just above the

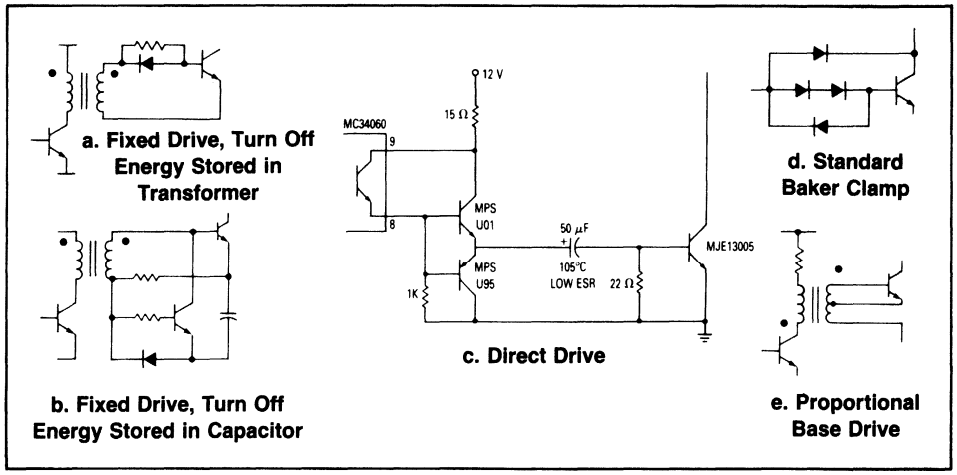


Figure 10-1. Typical Bipolar Base Drive Circuits

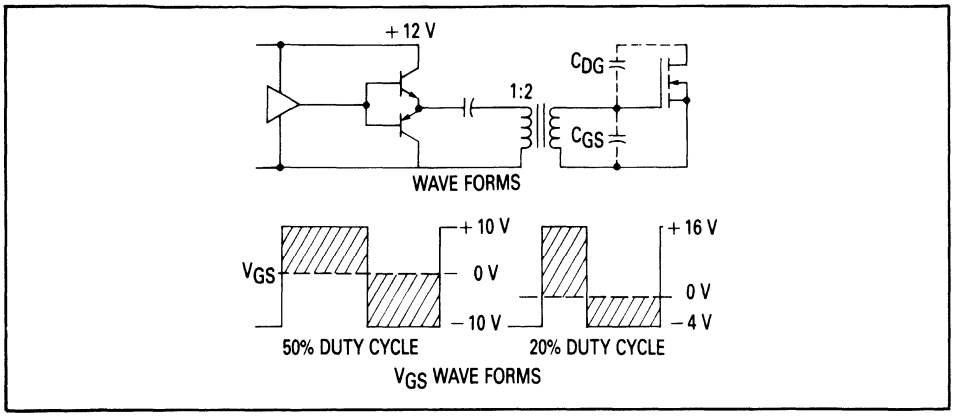


Figure 10-2A. Typical Transformer Coupled FET Drive

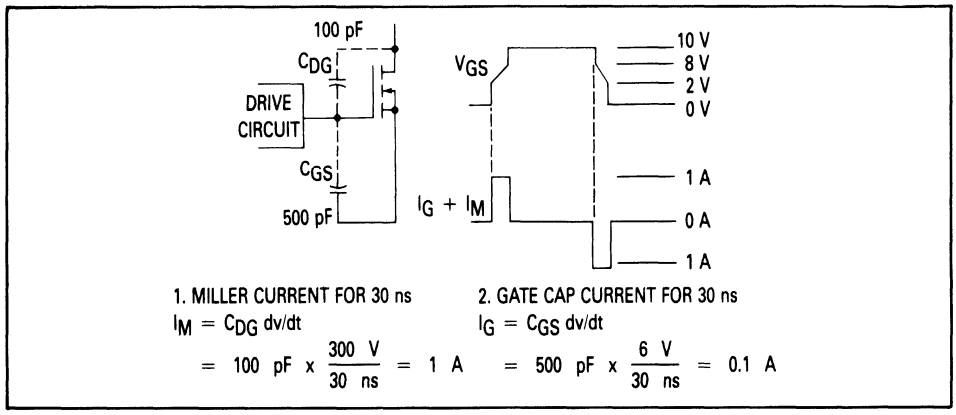


Figure 10-2B. FET Drive Current Requirements

threshold voltage which varies in duration depending on the amount of drive current available and this determines both the rise and fall times for the drain current. To estimate drive current requirements, two simple calculations with gate capacitances can be made:

1. $I_M = C_{DG}dv/dt$ and
2. $I_G = C_{GS}dv/dt$

I_M is the current required by the Miller effect to charge the drain-to-gate capacitance at the rate it is desired to move the drain voltage (and current). And I_G is usually the lesser amount of current required to charge the gate-to-source capacitance through the linear region (2 to 8 V). As an example, if 30 ns switching times are desired at 300 V where C_{DG} = 100 pF and C_{GS} = 500 pF, then

I_M = 100 pF x 300 V/30 ns = 1 A and
I_G = 500 pF x 6 V/30 ns = 0.1 A

This example shows the direct proportion of drive current capability to speed and also illustrates that for most devices, C_{DG} will have the greatest effect on switching speed and that C_{GS} is important only in estimating turn-on and turn-off delays.

Aside from its unique drive requirements, a FET is very similar to a bipolar transistor. Today's 400 V FETs compete with bipolar transistors in many switch-

ing applications. They are faster and easier to drive, but do cost more and have higher saturation, or more accurately, "on" voltages. The performance or efficiency tradeoffs are analyzed using Figure 10-3. Here, typical power losses for 10-2A switching transistors versus frequency are shown. The FET (and bipolar) losses were calculated at 100°C rather than 25°C because on resistance and switching times are highest here and 100°C is typical of many applications. These curves are asymptotes of the actual device performance, but are useful in establishing the "breakpoint" of various devices, which is the point where saturation and switching losses are equal.

Control Circuits

Over the past ten years, a variety of control IC's for SMPS have been introduced. The voltage mode controllers diagramed in Table 10-1 still dominate this market. The basic regulating function is performed in the pulse width modulator (PWM) section. Here, the dc feedback signal is compared to a fixed frequency sawtooth waveform. The result is a variable duty cycle pulse train which, with suitable buffer or interface circuits, can be used to drive the power switching transistor. Some ICs provide only a single output while others provide a phase splitter or flip-flop to alternately pulse two output channels. Additionally most ICs provide an error amplifier and reference section shown as a means to process, compare and amplify the feedback signal.

Features required by a control IC vary to some extent because of the particular needs of a designer and on the circuit configuration chosen. However, most of today's current generation ICs have evolved with the following capabilities or features:

- Programmable (to 500 kHz) Fixed Frequency Oscillator
- Linear PWM Section with Duty Cycle from 0 to 100%
- On Board Error Amplifiers
- On Board Reference Regulator
- Adjustable Dead Time
- Under Voltage (low Vcc) Inhibit
- Good Output Drive (100 to 200 mA)
- Option of Single or Dual Channel Output

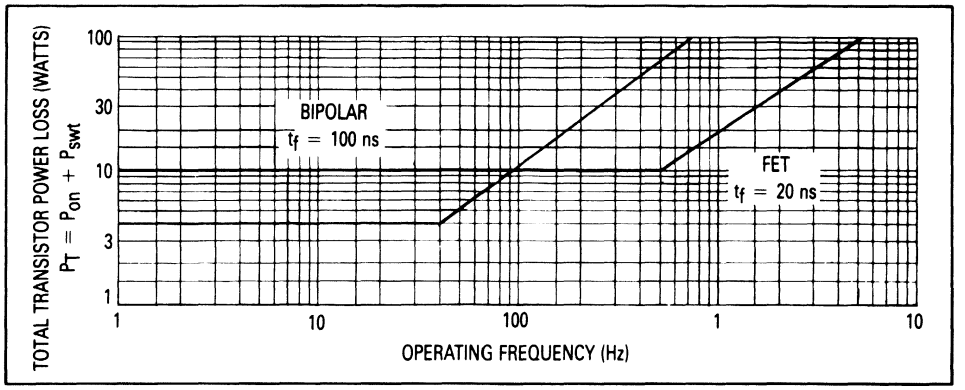


Figure 10-3. Typical Switching Losses at 300 V and 5 A (T_J = 100°C)

- Uncommitted Output Collector and Emitter or Totem Pole Drive Configuration
- Soft Start
- Digital Current Limiting
- Oscillator Sync Capability

It is primarily the cost differences in these parts that determine whether all or only part of these features will be incorporated. Most of these are evident to the designer who has already started comparing data sheets.

In addition to the control circuits listed in Table 10-2, Motorola also has two DC converter control chips, the μA78S40 and the MC34063. These chips feature an on-board 40 V, 2 A switching transistor and operate by dropping pulses from a fixed frequency, fixed duty cycle oscillator depending on load demand.

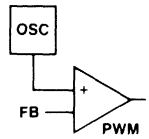
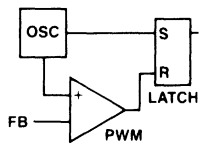
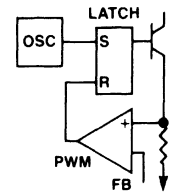
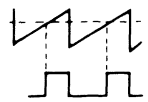
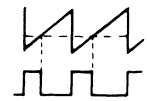
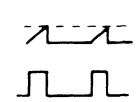
Today there is a demand for simple, low cost, single control IC's. These IC's like Motorola's MC34060 and MC34063 components are used to run the low power fly back type configurations and are usually part of a three chip rather than single chip system. The differences in these two approaches are illustrated in Figure 10-5.

When it is necessary to drive two or more power transistors, drive transformers are a practical interface element and are driven by the conventional dual channel IC's. In the case of a single transistor converter, however, it is usually more cost effective to directly drive the transistor from the IC. In this situation, an optocoupler is commonly used to couple the feedback signal from the output back to this control IC. And the error amplifier in this case is nothing more than programmable zener like Motorola's TL431.

Overvoltage Protection

Linear and switching power supplies can be protected from overvoltage with a crowbar circuit. For linear supplies, the pass transistor can fail shorted, allowing

TABLE 10-1. Basic SM Control IC's

	Type A Voltage Mode	Type B Voltage Mode with Latch	Type C Current Mode
CONTROL TECHNIQUE SCHEMATIC			
SINGLE CHANNEL PARTS	MC34060	(MPC1600)	(UC1842)
DUAL CHANNEL PARTS	TL494/594	SG1525A/27A SG1526	(MPC1600) —
FEATURES	Low Cost	Digital Current Limiting, Good Noise Immunity	Designed for Flyback, Inherent Feed Forward
PWM WAVEFORMS OUTPUT			

Note ( ) soon to be available

TABLE 10-2. Control Circuits

Over Voltage Protection (OVP)		Over-Under Voltage Protection (OUVP)
Standard	High Performance	
MC34061 MC34062 TL431	MC34061A MC3423 TL431A	MC3425

high line transformer voltage to the load. For switching power supplies, a loose or disconnectd remote sense lead can allow high voltage to the load.

The list of available circuits is shown in Table 10-2 and a typical 0 V application is shown in Figure 10-4.

This crowbar circuit (Figure 10-4) ignores noise spikes but will fire the SCR when a valid overvoltage condition is detected. The SCR will discharge C2 and either blow the fuse or cause the power supply to shut down.

For further information, see EB-78 and MC3423 data sheet.

Surge Current Protection

Many high current PWM switching supplies operate directly off the ac line. They have very large capacitive input filters with high inrush surge currents. The line circuit breaker and the rectifier bridge must be protected during turn-on.

Surge current limiting can be accomplished by adding Rs and an SCR "short" after charging C1 as shown in Figure 10-6, or by phase controlling the line voltage with a Triac.

Transformer Design

With respect to transformer design, many of today's designers would say don't try it. They'd advise using a consultant or winding house to perform this task and with good reason. It takes quite a bit of time to develop a feel for this craft and be able to use both experience and intuition to find solutions to second and third order problems. Because of these subtle problems, most designers find that after the first paper design is done, as many as four or five lab iterations may be necessary before the transformer meets the design goals. However, there is a considerable design challenge in this area and a great deal of satisfaction can be obtained by mastering it.

This component design, as do all others, begins by requesting all available literature from the appropriate manufacturers and then following this up with

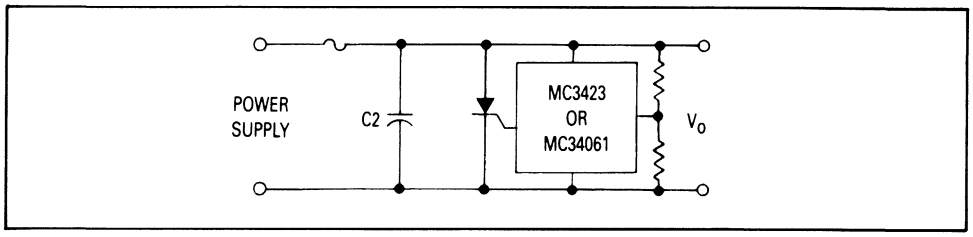
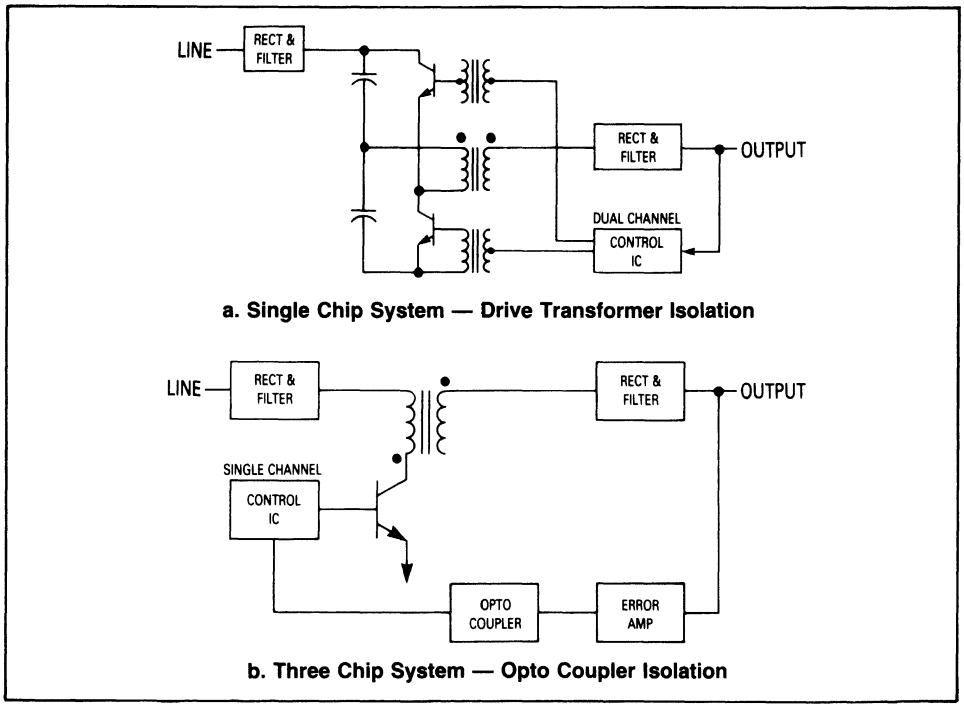


Figure 10-4. Crowbar Circuit

phone calls when specific questions arise. A partial list of companies is shown in Table 10-3. Designs below 20 W generally use pot cores but for 20 W and above E cores are preferred. E cores expose the windings to air so that heat is not trapped inside and make it easier to bring out connections for several windings. Remember that flyback designs require lower permeability cores than the others. The classic approach is to consult manufacturers charts like the one shown in Figure 10-7 and then to pick a core with the required power handling ability. Both E and EC (E cores with a round center leg) are popular now and they are available from several manufacturers. EC cores offer a performance advantage (better coupling) but standard E cores cost less and are also used in these applications. Another approach that seems to work equally well is to do a paper design of the estimated windings and turns required. Size the wire for 500 circular mils (CM) per amp and then find a core that has the required window area for this design. Now, before the windings are put on, it is a good idea to modify the turns so that they fit on one layer or an integral number of layers on that bobbin. This involves checking the turns per inch of the wire against the bobbin length. The primary generally goes on first and then the secondaries. If the primary hangs over an extra half layer, try reducing the turns or the wire size. Conversely, if the secondary does not take up a full layer, try bifilar winding (parallel) using wire half the size originally chosen; i.e., 3 wire sizes smaller like 23 versus 20. This technique ultimately results in the use of foil for the higher current (20 A) low voltage windings. Most windings can be separated with 3 mil mylar (usually yellow) tape but for good isolation, cloth is recommended between primary and secondary.



a. Single Chip System — Drive Transformer Isolation

b. Three Chip System — Opto Coupler Isolation

Figure 10-5. Control Circuit Topologies

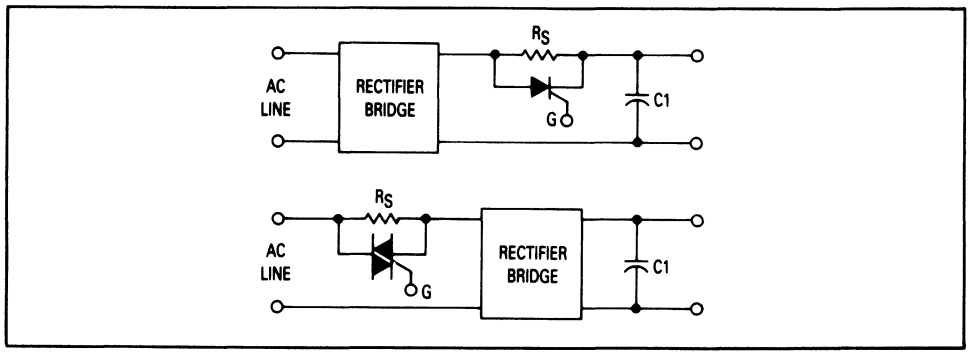


Figure 10-6. Surge Current Limiting for a Switching Power Supply

Finally, once a mechanical fit has been obtained, it is time for the circuit tests. The isolation voltage rating is strictly a mechanical problem and is one of the reasons why cloth is preferred over tape between the primary and secondary. The inductance and saturating current level of the primary are inherent to the design, and should be checked in the circuit or other suitable test fixture. Such a fixture is shown in Figure 10-8 where the transistor and diode are sized to handle the anticipated currents. The pulse generator is run at a low enough duty cycle to allow the core to reset. Pulse width is increased until the start of saturation is observed (I_{SAT}). Inductance is found using:

$$L = E/(di/dt)$$

In forward converters, the transformer generally has no gap in order to minimize the magnetizing current (I_M). For these applications the core should be chosen large enough so that the resulting LI product insures that I_M at operating voltages is less than I_{SAT}. For flyback designs, a gap is necessary and the test circuit is useful again to evaluate the effect of the gap. The gap will normally be quite large

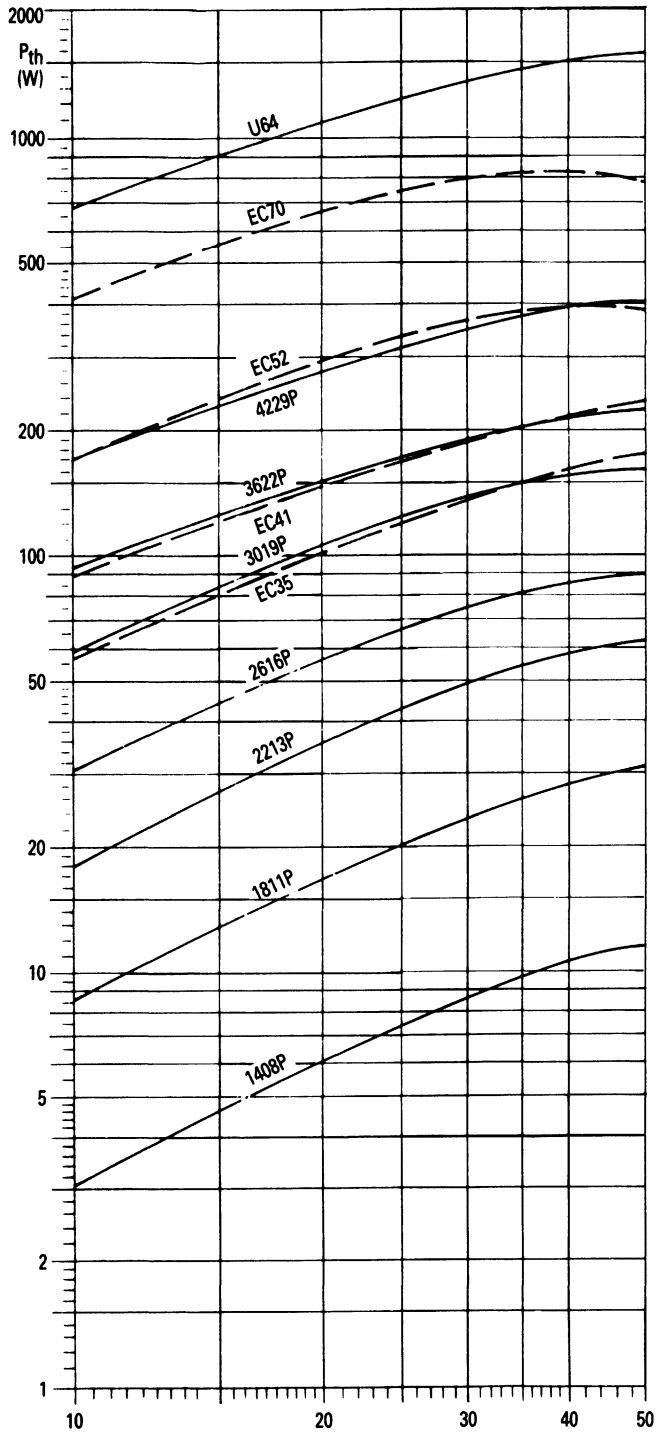
$$L_g >> L_m/u$$

where: L_g = gap length
L_m = magnetic path length
u = permeability

Under this stipulation, the gap directly controls the LI parameters and doubling it will decrease L by two and increase I_{SAT} by two until fringing effects occur. Gaps of 5 to 20 mils are common. Again, the anticipated switching currents must be less than I_{SAT} when the core is gapped for the correct inductance.

TABLE 10-3. Partial List of Core (C) and Transformer (T) Manufacturers

Company	Location	Code
Ferroxcube Inc.	Sauggerties, N.Y.	C
Indiana General	Keasby, N.J.	C
Stackpole	St. Marys, PA	C
TDK	El Segundo, CA	C
Pulse Engineering	San Diego, CA	T
Coilcraft	Cary, IL	T



NOTE: Power handling decreases by a factor of 2 in forward and 4 in flyback configurations.

Figure 10-7. Core Selection for Bridge Configurations (Reprinted from Ferroxcube Design Manual)

Transformer tests in the actual supply are usually done with a high voltage dc power supply on the primary and with a pulse generator or other manual control for the pulse width (such as using the control IC in the open loop configuration).

Here the designer must recheck three areas:

1. Core saturation
2. Correct amount of secondary voltage
3. Transformer heat rise

If problems are detected in any of these areas, the ultimate fix may be to redesign using the next larger core size. However, if problems are minimal, or none exist, it is possible to stay with the same core or even consider using the next smaller size.

Filter Capacitor Considerations

In today's 20 kHz switchers, aluminum electrolytics still predominate. The good news is that most have been characterized, improved, and cost reduced for this application. The input filter requires a voltage rating that depends on the peak line voltage; i.e., 400 to 450 V for a 220 V switcher. If voltage is increased beyond this point, the capacitor will begin to act like a zener and be thermally destroyed from high leakage currents if the rating is exceeded for enough time. In doubler circuits, voltage sharing of the two capacitors in series can be a problem. Here extra voltage capability may be needed to make up for the imbalances caused by different values of capacitance and leakage current. A bleeder resistor is normally used here not only for safety but to mask the differences in leakage current. The RMS current rating is also an important consideration for input capacitors and is an example of improvements offered by today's manufacturers. Earlier "lytics" usually lacked this rating and often overheated. Large capacitors that were not needed for performance were used just to reduce this heating. However, today's devices offer lower thermal resistance, improved connection to the foil and good RMS ratings. A partial list of manufacturers that supply both high voltage input and the lower voltage output capacitors for switchers is shown in Table 10-4. Most of the companies offer not only the standard 85°C components, but devices with up to 125°C ratings which are required because of the high ambient temperatures (55 to 85°C) that many switchers have to operate in, many times without the benefit of fans.

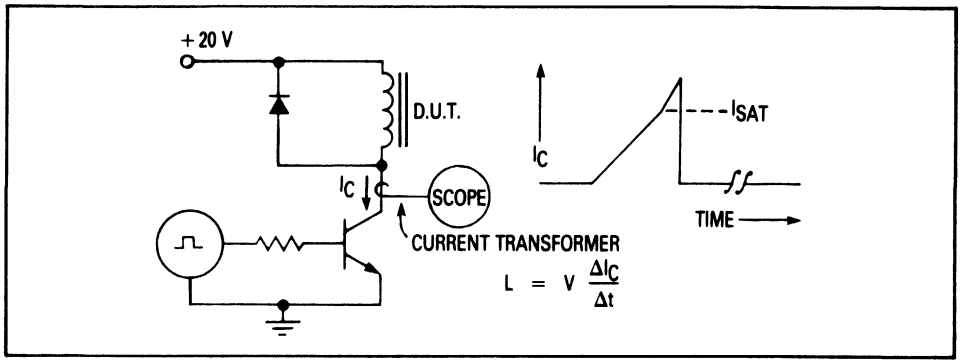


Figure 10-8. Simple Coil Tester

For output capacitors the buzz word is low ESR (equivalent series resistance). It turns out that for most capacitors even in the so-called "low ESR" series, the output ripple depends more on this resistance than on the capacitor value itself. Although typical and maximum ESR ratings are now available on most capacitors designed for switchers, the lead inductance generally is not specified except for the ultra-high frequency four terminal capacitors from some vendors. This parameter is responsible for the relatively high switching spikes that appear at the output. However, at this point in time, most designers find it less costly and more effective to add a high frequency noise filter rather than use a relatively expensive capacitor with low equivalent series inductance (ESL).

These LC noise or spike filters are made using small powdered iron toriods (1/2 to 1" OD) with distributed windings to minimize interwinding capacitance. And the output is bypassed using a small 0.1 μF ceramic or a 10 to 50 μF tantalum or both. Larger powered iron toriods are often used in the main LC output filter although the higher permeability ferrite EC and E cores with relatively large gaps can also be used. Calculations for the size of this component should take into account the minimum load so that the choke will not run "dry" as stated earlier.

TABLE 10-4. Partial List of Capacitor Companies

Company (U.S.)	Location
Sprague	North Adams, MA
MEPCO/Electra	Columbia, SC
Cornell-Dublier	Sanford, NC
Sangamo	Pickens, SC
Mallory	Indianapolis, IN

SECTION 11
SWITCHING REGULATOR COMPONENT DESIGN TIPS

Transistors

The initial selection of a transistor for a switcher is basically a problem of finding the one with voltage and current capabilities that are compatible with the application. For the final choice performance and cost tradeoffs among devices from the same or several manufacturers have to be weighed. Before these devices can be put in the circuit, both protective and drive circuits will have to be designed.

Motorola's first line of devices for switchers were trademarked "Switchmode" transistors and introduced in the early 70's with data sheets that provided all the information that a designer would need including reverse bias safe operating area (RBSOA) and performance at elevated temperature (100°C). The first series was the 2N6542 through 2N6547, TO-204 (TO-3) and was followed by the MJE13002 through MJE13009 series in a plastic TO-220 package. Finally, high voltage (1 kV) requirements were met by the metal MJ8500 thru MJ8505 series and the plastic MJE8500 series. And recently, Motorola introduced the two new families of "Switchmode" transistors shown in Table 11-1. The Switchmode II series is an advanced version of Switchmode I that features faster switching. Switchmode III is a state of the art bipolar with exceptional speed, RBSOA, and up to 1.5 kV blocking capacity. Here, device cost is somewhat higher, but system costs may be lowered because of reduced snubber requirements and higher operating frequencies. A similar argument applies to Motorola TMOS Power FETs. These devices make it possible to switch efficiently at higher frequencies (200 to 500 kHz) but the main selling point is that they are easier to drive. This latter point is the one most often made to show that systems savings are again quite possible even though the initial device cost is higher.

TABLE 11-1. Motorola High Voltage Switching Transistor Technologies

Family	Typical Device	Typical Fall Time	Approximate Switching Frequency
SWITCHMODE I	2N6545 MJE13005 MJE12007	200–500 ns	20 k
SWITCHMODE II	MJ13081	100 ns	100 k
SWITCHMODE III	MJ16010	50 ns	200 k
TMOS	MTP5N40	20 ns	500 k

Table 11-2 is a chart of the transistor voltage requirements for the various off-line converter circuits. As illustrated, the most stringent requirement for single transistor circuits (flyback and forward) is the blocking or V_{CEV} rating. Bridge circuits, on the other hand, turn on and off from the dc bus and their most critical voltage is the turn-on or $V_{CEO(sus)}$ rating.

TABLE 11-2. Power Transistor Voltage Chart

Line Voltage	Circuit			
	Flyback, Forward or Push-Pull		Half or Full Bridge	
	V_{CEV}	$V_{CEO(sus)}$	$V_{CEO(sus)}$	V_{CEV}
220	850–1 kV	450	450	450
120	450	250	250	250

Most Switchmode transistor load lines are inductive during turn-on and turn-off. Turn-on is generally inductive because the short circuit created by output rectifier reverse recovery times is isolated by leakage inductance in the transformer. This inductance effectively snubs most turn-on load lines so that the rectifier recovery (or short circuit) current and the input voltage are not applied simultaneously to the transistor. Sometimes primary interwinding capacitance presents a small current spike but usually turn-on transients are not a problem. Turn-off transients due to this same leakage inductance, however, are almost always a problem. In bridge circuits, clamp diodes can be used to limit these voltage spikes. If the resulting inductive load line exceeds the transistor's reverse bias switching capability (RBSOA) then an RC network may also be added across the primary to absorb some of this transient energy. The time constant of this network should equal the anticipated switching time of the transistor (50 to 500 ns). Resistance values of 100 to 1000 ohms in this RC network are generally appropriate. Trial and error will indicate how low the resistor has to be to provide the correct amount of snubbing. For single transistor converters, the circuits shown in Figure 11-1 are generally used. Here slightly different criteria are used to define the R and C snubber values:

$$C = \frac{I\, t_f}{V}$$

where I = The peak switching current
t_f = The transistor fall time
V = The peak switching voltage (Approximately twice the dc bus)

also $R = t_{on}/C$ (it is not necessary to completely discharge this capacitor in order to obtain the desired effects of this circuit)

where t_{on} = The minimum on-time or pulse width

and $$P_R = \frac{CV^2f}{2}$$

where P_R = The power rating of the resistor
and f = The operating frequency

In most of today's designs snubber elements are small or nonexistent and voltage spikes from energy left in the leakage inductance a more critical problem depending on how good the coupling is between the primary and clamp windings and how fast the clamp diode turns on. FETs often have to be slowed down to prevent self destruction from this spike.

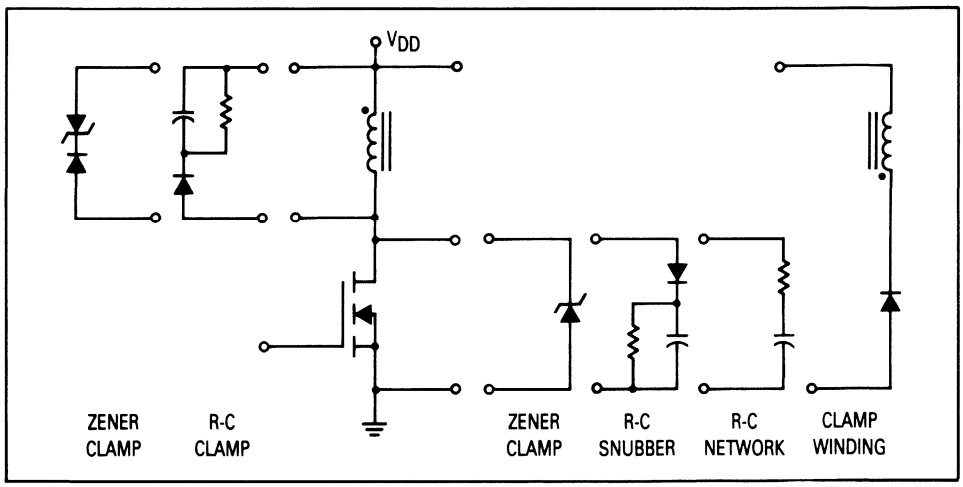


Figure 11-1. Protection Circuits for Switching Transistors

Zener and Mosorb Transient Suppressors

If necessary, protection from voltage spikes may be obtained by adding a zener and rectifier across the primary as shown in Figure 11-1. Here Motorola's 5 W zener lines with ratings up to 200 V and 10 watt TO-220 Mosorbs with ratings up to 250 V can provide the clamping or spike limiting function. If the zener must handle most of the power, its size can be estimated using:

$$P_Z = \frac{L_L I^2 f}{2}$$

where P_Z = The zener power rating

and L_L = The leakage inductance (measured with the clamp winding or secondary shorted)

I = Peak collector current

f = Operating frequency

Distinction is sometimes made between devices trademarked Mosorb (by Motorola Inc.), and standard zener/avalanche diodes used for reference, low-level regulation and low-level protection purposes. It must be emphasized that Mosorb devices are, in fact, zener diodes. The basic semiconductor technology and processing are identical. The primary difference is in the applications for which they are designed. Mosorb devices are intended specifically for transient protection purposes and are designed, therefore, with a large effective junction area that provides high pulse power capability while minimizing the total silicon use. Thus, Mosorb pulse power ratings begin at 600 watts — well in excess of low power conventional zener diodes which in many cases do not even include pulse power ratings among their specifications.

MOVs, like Mosorbs, do have the pulse power capabilities for transient suppression. They are metal oxide varistors (not semiconductors) that exhibit bidirectional avalanche characteristics, similar to those of back-to-back connected zeners. The main attributes of such devices are low manufacturing cost, the ability to absorb high energy surges (up to 600 joules) and symmetrical bidirectional "breakdown" characteristics. Major disadvantages are: high clamping factor, an

internal wear-out mechanism and an absence of low-end voltage capability. These limitations restrict the use of MOVs primarily to the protection of insensitive electronic components against high energy transients in applications above 20 volts, whereas, Mosorbs are best suited for precise protection of sensitive equipment even in the low voltage range — the same range covered by conventional zener diodes.

Rectifiers

Once components for the inverter section of a switcher have been chosen, it is time to determine how to get power into and out of this section. This is where the all-important rectifier comes into play. (See Figure 11-2.) The input rectifier is generally a standard recovery bridge that operates off the ac line and into a capacitive filter. For the output section, most designers use Schottkys for efficient rectification of the low voltage, 5 V output windings and for the higher voltage, 12 to 15 V outputs, the more economical fast recovery or ultrafast diodes are used.

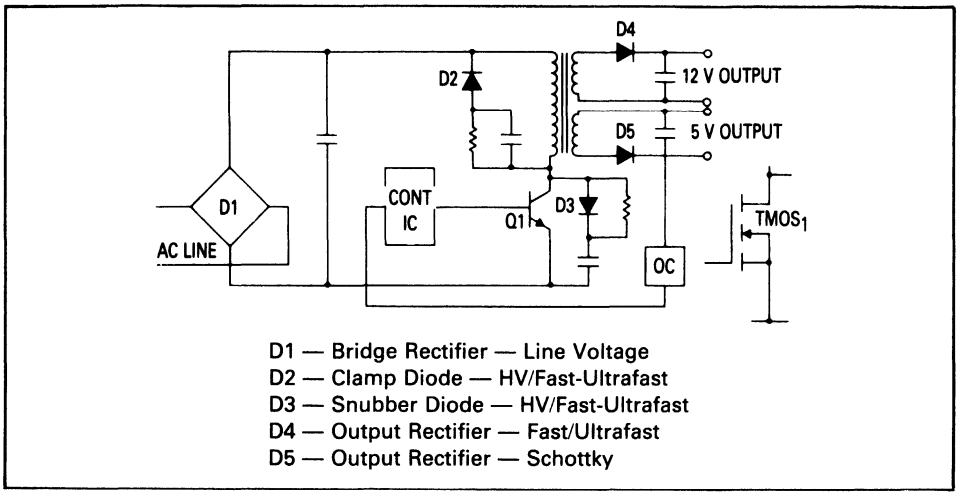


Figure 11-2. Switchmode Power Supply Flyback or Boost Design

For the process of choosing an input rectifier, it is useful to visualize the circuit shown in Figure 11-3. To reduce cost, most earlier approaches of using choke input filters, soft start relays (Triacs), or SCRs to bypass a large limiting resistor have been abandoned in favor of using small limiting resistors or thermistors and a large bridge. The bridge must be able to withstand the surge currents that exist from repetitive starts at peak line. The procedure for finding the right component and checking its fit is as follows:

1. Choose a rectifier with 2 to 5 times the average I_o required.
2. Estimate the peak surge current (I_p and time (t) using:

$$I_p = \frac{1.4\ V_{in}}{R_S} \qquad t = RsC$$

Where V_{in} is the RMS input voltage
Rs is the total series resistance, and
C is the filter capacitor size

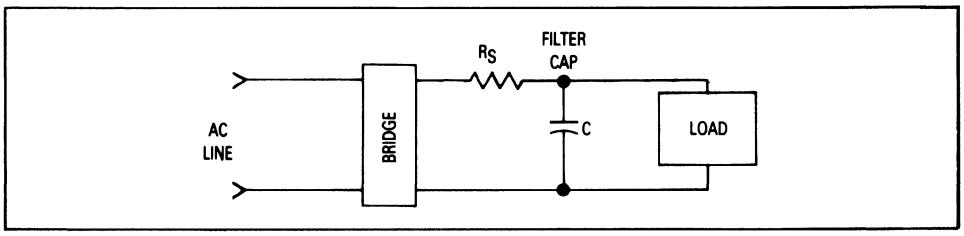


Figure 11-3. Choosing Input Rectifiers

3. Compare this current pulse to the sub cycle surge current rating (Is) of the diode itself. If the curve of Is versus time is not given on the data sheet, the approximate value for Is at a particular pulse width (t) may be calculated knowing:
   - I_{FSM} — the single cycle (8.3 ms) surge current rating and using.
   - $I^2\sqrt{t} = K$ which applies when the diode temperature rise is controlled by its thermal response as well as power (i.e., $T = K'P\sqrt{t}$ for $t <$ 8 ms.

   This gives:

   $Is^2\sqrt{t} = I^2_{FSM}\sqrt{8.3\ ms}$ or

   $$Is = I_{FSM}\left(\frac{8.3\ ms}{t}\right)^{1/4}, \text{ t is in milliseconds}$$

4. If Is <Ip, consider either increasing the limiting resistor (Rs) or utilizing a larger diode.

In the output section where high frequency rectifiers are needed, there are several types available to the designer. In addition to the Schottky (SBR) and fast recovery (FR), there is also an ultrafast recovery (UFR). Comparative performance for devices with similar current ratings is shown in Table 11-3. The obvious point here is that lower forward voltage improves efficiency and lower recovery times reduce turn-on losses in the switching transistors, but the tradeoff is higher cost. As stated earlier, Schottkys are generally used for 5 V outputs

TABLE 11-3. Motorola Rectifier Product Portfolio

Parameter	Schottky	Ultrafast	Fast Recovery	Standard Recovery
V_F (VOLTS) Forward Voltage	0.5–0.6	0.9–1	1.2–1.4	1.2–1.4
t_{rr} Reverse Recovery Time	<10 ns	25–100 ns	150 ns	1 μs
t_{rr} Form	Soft	Soft	Soft	Soft
V_R (VOLTS) dc Blocking Voltage	20–60 V	50–1000 V	50–1000 V	50–1000 V
Cost Ratio	3:1	3:1	2:1	1:1

and fast recovery and ultrafast devices for 12 V outputs and greater. The ultrafast is competing both with the Schottky where higher breakdown is needed and with the fast recovery in those applications where performance is more important than cost. Ten years ago Schottkys were very fragile and could fail short from either excessive dv/dt (1 to 5 volts per nanosecond) or reverse avalanche. Since that time, Motorola has incorporated a "guard ring" or internal zener which minimizes these earlier problems and reduces the need for RC snubbers and other external protective networks.

SECTION 12
BASIC SWITCHING POWER SUPPLY CONFIGURATIONS

The implementation of switching power supplies by the non-specialist is becoming increasingly easy due to the availability of power devices and control ICs especially developed for this purpose by the semiconductor manufacturer.

This section is meant to help in the preliminary selection of the devices required for the implementation of the listed switching power supplies.

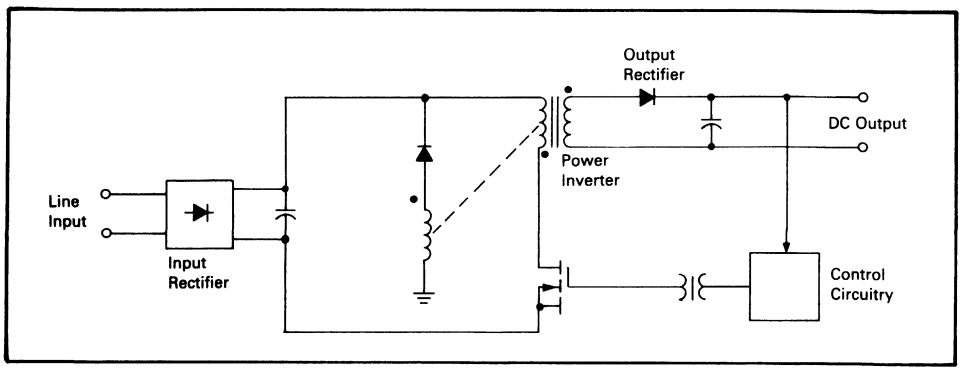
Flyback and Forward Converter Switching Power Supplies: 50–250 W

- Input line variation: V_{in} + 10%, − 20%
- Converter efficiency: η = 80%
- Output regulation by duty cycle (δ variation: δ_{max} = 0.4)
- Maximum Transistor working current:

$$I_w = \frac{2\ P_{out}}{\eta \cdot \delta_{max} \cdot V_{in(min)} \cdot \sqrt{2}} = \frac{5.5\ P_{out}}{V_{in}} \text{ (Flyback)}$$

$$= \frac{P_{out}}{\eta \cdot \delta_{max} \cdot V_{in(min)} \cdot \sqrt{2}} = \frac{2.25\ P_{out}}{V_{in}} \text{ (Forward)}$$

- Maximum transistor working voltage: $V_w = 2 \cdot V_{in(max)} \cdot \sqrt{2}$ + guardband
- Working frequency: f = 20 to 200 kHz



Basic Flyback Configuration

Table 12-1. Flyback and Forward Converter Semiconductor Selection Chart

Output Power	50 W		100 W		175 W		250 W
Input Line Voltage, V_{in}	120 V	220 V or 240 V	120 V	220 V or 240 V	120 V	220 V or 240 V	120 V
MOSFET Requirements							
Max Working Current, I_W	2.25 A	1.2 A	4.0 A	2.5 A	8.0 A	4.4 A	11.4 A
Max Working Voltage, V_{DSW}	380 V	750 V	380 V	750 V	380 V	750 V	380 V
Power MOSFETs Recommended							
Metal (TO-204AA) (TO-3)	MTM4N45	MTM2N90	MTM4N45	MTM2N90	MTM7N45	MTM4N90	MTM15N45
Plastic (TO-220AB)	MTP4N45	MTP2N90	MTP4N45	MTP2N90	—	—	—
Plastic (TO-218AC)	—	—	—	—	MTH7N45	—	—
Input Rectifiers							
Max Working Current, I_{DC}	0.4 A	0.25 A	0.4 A	0.5 A	2.35 A	1.25 A	4.6 A
Recommended Types	MDA104A	MDA106A	MDA206	MDA210	MDA970	MDA210	MDA3506
Output Rectifiers							
Recommended types for							
Output Voltage of: 5.0 V	MBR3035PT		MBR3035PT		MBR12035CT		MBR20035CT
10 V	MUR3010PT		MUR3010PT		MUR10010CT		MUR10010CT
20 V	MUR1615CT		MUR1615CT		MUR3015PT		MUR10015CT
50 V	MUR1615CT		MUR1615CT		MUR1615CT		MUR3015PT
100 V	MUR440, MUR840A		MUR840A		MUR840A		MUR840A
Recommended Control Circuits	SG1525A, SG1526, TL494; Inverter Control Circuit MC3423; Overvoltage Detector Error Amplifier: SINGLE TL431; DUAL-LM358; QUAD — MC3403, LM324, LM2902						

Flyback and Forward Converters

To take advantage of the regulating techniques discussed earlier and also provide isolation, a total of seven popular configurations have evolved and are listed below. Each circuit has a practical power range or capability associated with it as follows:

Circuit	Power Range	Motorola Reference	Parts Cost
DC Converter	5 watts	AN920	$ 4.00
Converter with 30 V Transformer	10 watts	AN920	7.00
Blocking OSC	20 watts	—	10.00
Flyback	50 watts	EB-87	15.00
Forward	100 watts	—	20.00
Half Bridge	200 watts	EB's 86 & 100, AN-767	30.00
Full Bridge	500 watts	EB-85	75.00

First to be discussed will be the low power (20–200 W) converters which are dominated by the single transistor circuits shown in Figure 12-1. All of these circuits operate the magnetic element in the unipolar rather than bipolar mode. This means that transformer size is sacrificed for circuit simplicity.

The flyback (alternately known as the "ringing choke") regulator stores energy in the primary winding and dumps it into the secondary windings (see

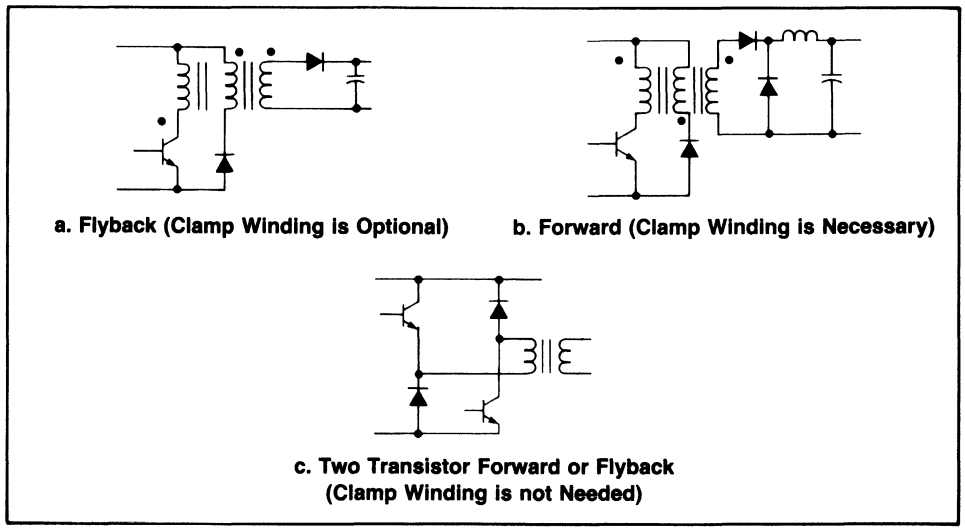


Figure 12-1. Low Power Popular (20–200 W) Converter Configurations

Figure 12-1a). A clamp winding is usually present to allow energy stored in the leakage reactance to return safely to the line instead of avalanching the switching transistor. The operating model for this circuit is the buck-boost discussed earlier. The flyback is the lowest cost regulator because output filter chokes are not required since the output capacitors feed from a current source rather than a voltage source. It does have higher output ripple than the forward converters because of this. However, it is an excellent choice when multiple output voltages are required and does tend to provide better cross regulation than the other types. In other words changing the load on one winding will have little effect on the output voltage of the others.

A 120/220 Vac flyback design requires transistors that block twice the peak line plus transients or about 1 kV. Motorola's MJE13000 and 16000A series with ratings of 750 to 1000 V are normally used here. These bipolar devices are relatively fast (100 ns) and are typically used in the 20 to 50 kHz operating frequency range. The recent availability of 900 and 1000 V TMOS FETs allows designers to operate in the next higher range (50 to 80 kHz) and some have even gone as high as 300 kHz with square wave designs and FETs. Faster 1 kV bipolar transistors are also planned in the future and will provide another design alternative. The two transistor variations of this circuit (Figure 12-1c) eliminate the clamp winding and add a transistor and diode to effectively clamp peak transistor voltages to the line. With this circuit a designer can use the faster 400 V to 500 V FET transistors and push operating frequencies considerably higher. There is a cost penalty here over the single transistor circuit due to the extra transistor, diodes and gate drive circuitry.

A subtle variation in the method of operation can be applied to the flyback regulator. The difference is referred to as operation in the discontinuous or continuous mode and the waveform diagrams are shown in Figure 12-2. The analysis given in the earlier section on boost regulators dealt strictly with the discontinuous mode where all the energy is dumped from the choke before the transistor turns on again. If the transistor is turned on while energy is still being dumped into

the load, the circuit is operating in the continuous mode. This is generally an advantage for the transistor in that it needs to switch only half as much peak current in order to deliver the same power to the load. In many instances, the same transformer may be used with only the gap reduced to provide more inductance. Sometimes the core size will need to be increased to support the higher LI product (2 to 4 times) now required because the inductance must increase by almost 10 times to effectively reduce the peak current by two. In dealing with the continuous mode, it should also be noted that the transistor must now turn on from 500 to 600 V rather than 400 V level because there no longer is any dead time to allow the flyback voltage to settle back down in the input voltage level. Generally it is advisable to have $V_{CEO(sus)}$ ratings comparable to the turn-on requirements except for SMIII where turn on up to V_{CEV} is permitted.

The flyback converter stands out from the others in its need for a low inductance, high current primary. Conventional E and pot core ferrites are difficult to work with because their permeability is too high even with relatively large gaps (50 to 100 milli-inches). The industry needs something better that will provide permeabilities of 60 to 120 instead of 2000 to 3000 for this application.

The single transistor forward converter is shown in Figure 12-1b. Although it initially appears very similar to the flyback, it is not. The operating model for this circuit is actually the buck regulator discussed earlier. Instead of storing energy in the transformer and then delivering it to the load, this circuit uses the transformer in the active or forward mode and delivers power to the load while the transistor is on. The additional output rectifier is used as a freewheeling diode for the LC filter and the third winding is actually a reset winding. It generally has the same turns as the primary, (is usually bifilar wound) and does clamp the

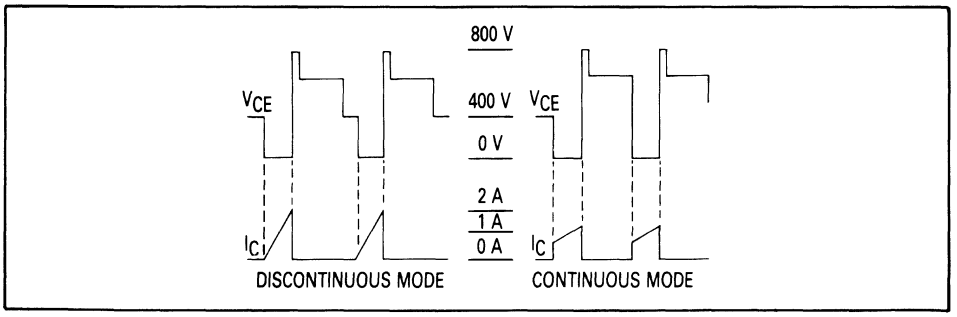


Figure 12-2. Flyback Transistor Waveforms

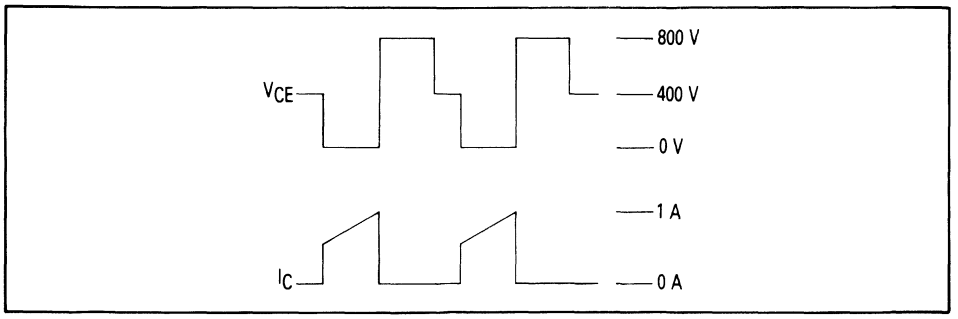


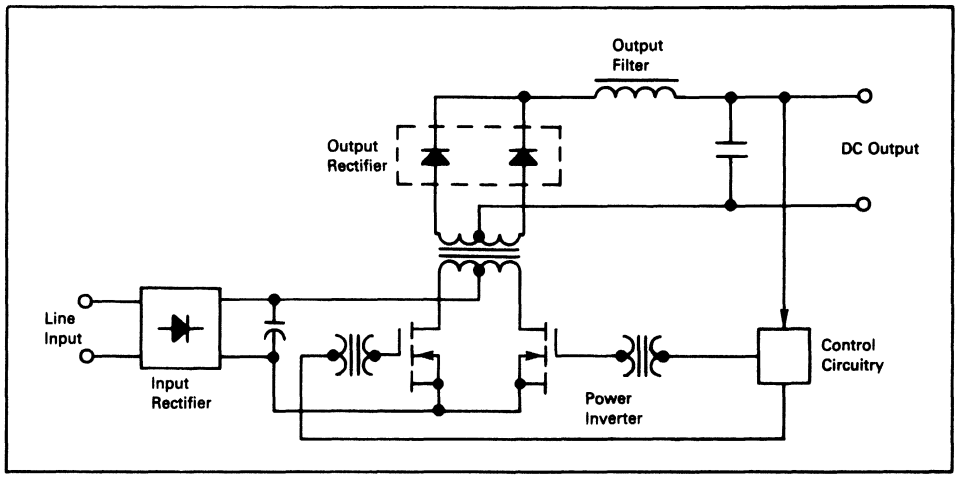
Figure 12-3. Forward Converter Transistor Waveforms

Push-Pull Switching Power Supplies: 100–500 W

- Input line variation: V_{in} + 10%, − 20%
- Converter efficiency: η = 80%
- Output regulation by duty cycle (δ) variation: δ_{max} = 0.8
- Maximum transistor working current:

$$I_w = \frac{P_{out}}{\eta \cdot \delta_{max} \cdot V_{in(min)} \cdot \sqrt{2}} = \frac{1.4\ P_{out}}{V_{in}}$$

- Maximum transistor working voltage: $V_w = 2 \cdot V_{in(max)} \cdot \sqrt{2}$ + guardband
- Working frequency: f = 20 to 200 kHz



Basic Push-Pull Configuration

Table 12-2. Push-Pull Semiconductor Selection Chart

Output Power	100 W		250 W		500 W	
Input Line Voltage, V_{in}	120 V	220 V 240 V	120 V	220 V 240 V	120 V	220 V 240 V
MOSFET Requirements						
Max Working Current, I_w	1.2 A	0.6 A	2.9 A	1.6 A	5.7 A	3.1 A
Max Working Voltage, V_{DSW}	380 V	750 V	380 V	750 V	380 V	750 V
Power MOSFETs Recommended						
Metal (TO-204AA) (TO-3)	MTM2N50	MTM2N90	MTM4N45	MTM2N90	MTM7N45	MTM4N90
Plastic (TO-220AB)	MTP2N45	MTP2N90	MTP4N45	MTP2N94	—	—
Plastic (TO-218AC)	—	—	—	—	MTH7N45	—
Input Rectifiers						
Max Working Current, I_{DC}	0.9 A	0.5 A	2.35 A	1.25 A	4.6 A	2.5 A
Recommended Types	MDA206	MDA210	MDA970-5	MDA210	MDA3506	MDA3510
Output Rectifiers:						
Recommended types						
for output voltages of: 5.0 V	MBR3035PT		MBR12035CT		MBR20035CT	
10 V	MBR3045PT MUR3010PT		MUR10010CT		MUR10010CT	
20 V	MUR1615CT		MUR3015PT		MUR10015CT	
50 V	MUR1615CT		MUR1615CT		MUR3015PT	
100 V	MUR840A, MUR440		MUR840A		MUR840A	
Recommended Control Circuits	See Table 12-1					

reset voltage to twice the line. However, its main function is to return energy stored in the magnetizing inductance to the line and thereby reset the core after each cycle of operation. Because it takes the same time to set and reset the core, the duty cycle of this circuit cannot exceed 50%. This also is a very popular low power converter and like the flyback is practically immune from transformer saturation problems. Transistor waveforms shown in Figure 12-3 illustrate that the voltage requirements are identical to the flyback. For the single transistor versions, 400 V turn-on and 1 kV blocking devices like the MJE13000 and MJE16000 transistors are required. The two transistor circuit variations shown in Figure 12-1b again adds a cost penalty but allows a designer to use the faster 400 to 500 V devices. With this circuit, operation in the discontinuous mode refers to the time when the load is reduced to a point where the filter choke runs "dry." This means that choke current starts at and returns to zero during each cycle of operation. Most designers prefer to avoid this type of mode because of higher ripple and noise even though there are no adverse effects on the components themselves. Standard ferrite cores work fine here and in the high power converters as well. In these applications, no gap is used as the high permeability (3000) results in the desirable effect of very low magnetizing current levels. And, Zeners or RC clamps may be used to reset the core in lieu of the clamp winding to lower the voltage stress on the switching transistors.

Push-Pull and Bridge Converters

The high power circuits shown in Figures 12-4–12-7 all operate the magnetic element in the bipolar or push-pull mode and require 2 to 4 inverter transistors. Because the transformers operate in this mode they tend to be almost half the size of the equivalent single transistor converters and thereby provide a cost advantage over their counterparts at power levels of 200 to 1 kW.

The push-pull converter shown in Figure 12-4 is one of the oldest converter circuits around. Its early use was in low voltage inverters such as the 12 Vdc to 120 Vdc power source for recreational vehicles and in dc to dc converters. Because these converters are free running rather than driven and operate from low voltages, transformer saturation problems are minimal. In the high voltage off-line switchers, saturation problems are common and were difficult to solve. The transistors are also subjected to twice the peak line voltage which requires the use of high voltage (1 kV) transistors. Both of these drawbacks have tended to discourage designers of off-line switchers from using this configuration until current mode control IC's were introduced. Now these circuits are being looked at with renewed interest.

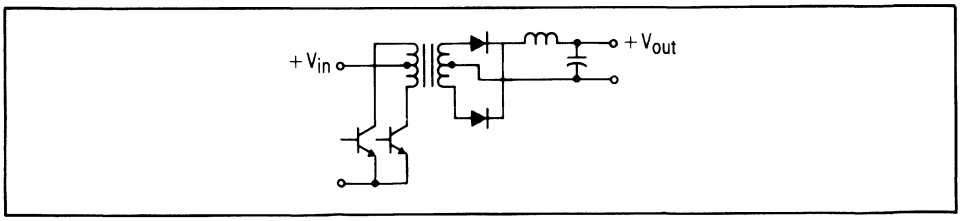


Figure 12-4. Push-Pull Converter (200 W–1 kW)

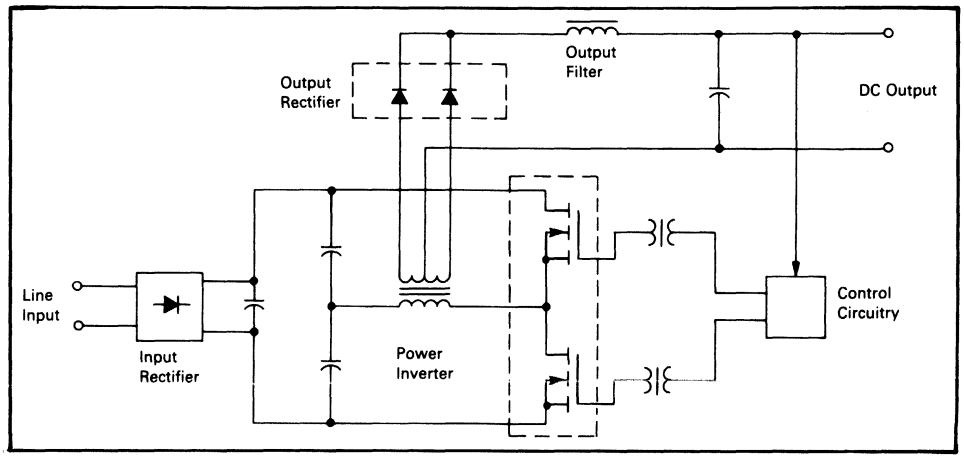
Half-Bridge/Full-Bridge Switching Power Supplies: 100–500 W/500–1000 W

- Input line variation: V_{in} + 10%, − 20%
- Converter efficiency: η = 80%
- Output regulation by duty cycle (δ) variation: δ_{max} = 0.8
- Maximum working current:

$$I_w = \frac{2\ P_{out}}{\eta \cdot \delta_{max} \cdot V_{in(min)} \cdot \sqrt{2}} = \frac{2.8\ P_{out}}{V_{in}} \text{ (Half-Bridge)}$$

$$= \frac{P_{out}}{\eta \cdot \delta_{max} \cdot V_{in(min)} \cdot \sqrt{2}} = \frac{1.4\ P_{out}}{V_{in}} \text{ (Full-Bridge)}$$

- Maximum transistor working voltage:
  $V_w = V_{in(max)} \cdot \sqrt{2}$ + guardband
- Working frequency: f = 20 to 200 kHz



Basic Half-Bridge Configuration

Table 12-3. Half-Bridge Semiconductor Selection Chart

Output Power	100 W		350 W		500 W	
Input Voltage, V_{in}	120 V	220 V 240 V	120 V	220 V 240 V	120 V	220 V 240 V
MOSFET Requirements Max Working Current, I_w Max Working Voltage, V_{DSW}	 2.3 A 190 V	 1.25 A 380 V	 5.7 A 190 V	 3.1 A 380 V	 11.5 A 190 V	 6.25 A 380 V
Power MOSFETs Recommended Metal (TO-204AA) (TO-3) Plastic (TO-220AB) Plastic (TO-218AC)	 MTM5N35 MTP3N40 —	 MTM2N45 MTP2N45 —	 MTM8N40 — MTH8N40	 MTM4N45 MTP4N45 —	 MTM10N25 MTP10N25 —	 MTM7N45 — MTH7N45
Input Rectifiers Max Working Current, I_{DC} Recommended Types	 0.9 A MDA206	 0.5 A MDA210	 2.3 A MDA970-5	 1.25 A MDA210	 4.6 A MDA3506	 2.5 A MDA3510
Output Rectifiers: Recommended types for output voltage of: 5.0 V 10 V 20 V 50 V 100 V	 MBR3035PT MBR3045PT MUR3010PT MUR1615CT MUR1615CT MUR840A, MUR440		 MBR12035CT MUR10010CT MUR3015PT MUR1615CT MUR840A		 MBR20035CT MUR10010CT MUR10015CT MUR3015PT MUR840A	
Recommended Control Circuits	See Table 12-1					

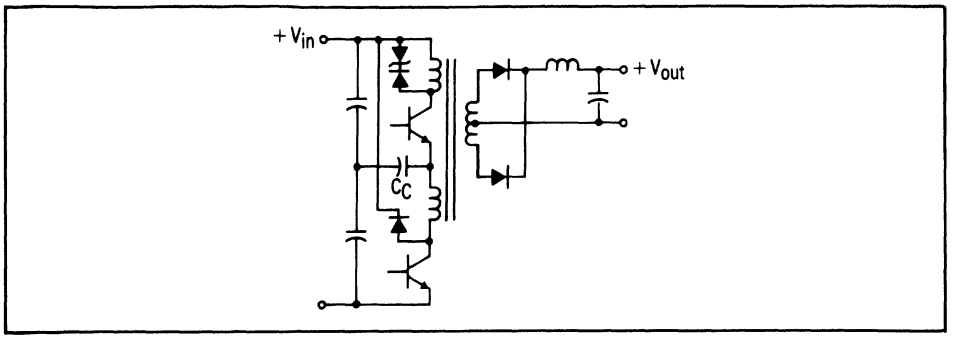


Figure 12-5. Half-Bridge Converter with Split Windings

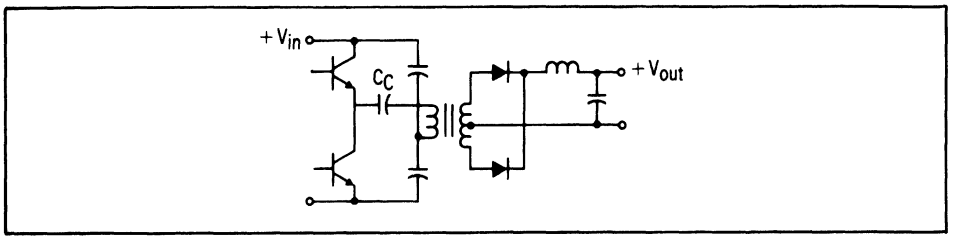
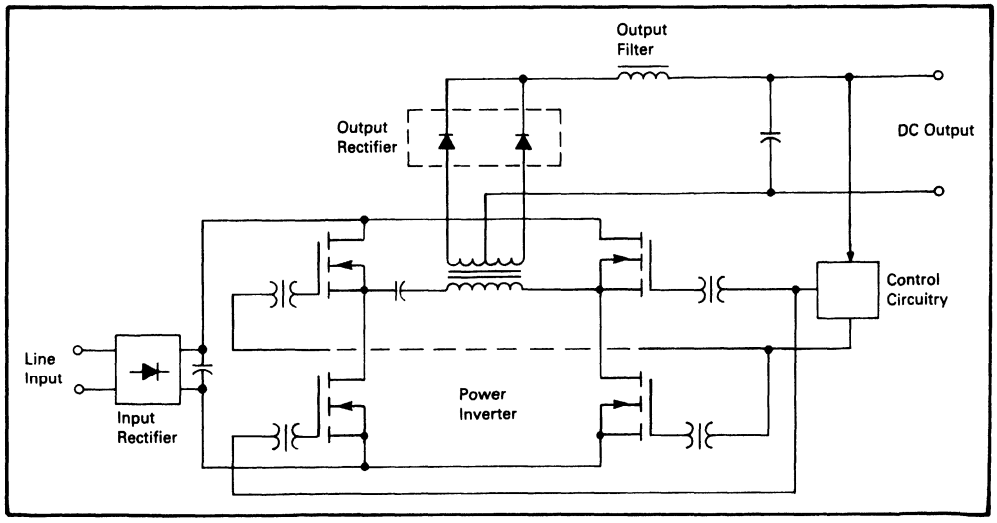


Figure 12-6. Half-Bridge Converter (200 W–1 kW)

Half and Full Bridge

The most popular high power converter is the half bridge (Figure 12-6). It has two clear advantages over the push-pull and became the favorite rather quickly. First, the transistors never see more than the peak line voltage and the standard 400 V fast Switchmode transistors that are readily available may be used. And second, and probably even more important, transformer saturation problems are easily minimized by use of a small coupling capacitor (about 2–5 μF) as shown. Because the primary winding is driven in both directions, a full wave output



Basic Full-Bridge Configuration

Table 12-4. Full-Bridge Semiconductor Selection Chart

Output Power	500 W		750 W		1000 W	
Input Voltage, V_{in}	120 V	220 V 240 V	120 V	220 V 240 V	120 V	220 V 240 V
MOSFET Requirements Max Working Current, I_W Max Working Voltage, V_{DSW}	5.7 A 190 V	3.1 A 380 V	8.6 A 190 V	4.7 A 380 V	11.5 A 190 V	6.25 A 380 V
Power MOSFETs Recommended Metal (TO-204AA) (TO-3) Plastic (TO-220AB) Plastic (TO-218AC)	MTM8N20 MTP8N20 —	MTM4N45 MTP4N45 —	MTM10N25 MTP10N25 —	MTM7N45 MTP4N45 MTH7N45	MTM15N20 MTP12N20 MTH15N20	MTM7N45 — MTH7N45
Input Rectifiers Max Working Current, I_{DC} Recommended Types	4.6 A MDA3506	2.5 A MDA3510	7.0 A	3.8 A	9.25 A	5.0 A
Output Rectifiers: Recommended types for output voltages of: 5.0 V 10 V 20 V 50 V 100 V	MBR20035CT MUR10010CT MUR10015CT MUR3015PT MUR804PT		MBR30035CT MUR10010CT* MUR10015CT MUR3015PT* MUR3040PT*		MBR30035CT* MUR10010CT* MUR10015CT* MUR10015CT MUR3040PT	
Recommended Control Circuits	See Table 12-1					

*More than one device per leg, matched.

filter, rather than half, is now used and the core is actually utilized more effectively. Another more subtle advantage of this circuit is that the input filter capacitors are placed in series across the rectified 220 V line which allows them to be used as the voltage doubler elements on a 120 V line. This still allows the inverter transformer to operate from a nominal 320 V bus when the circuit is connected to either 120 V or 220 V. Finally, this topology allows diode clamps across each transistor to contain destructive switching transients. The designer's dream, of course, is for fast transistors that can handle a clamped inductive load line at rated current. And a few (like the MJE16000 series from Motorola) are beginning to appear on the market. With the improved RBSOA that these transistors feature, less snubbing is required and this improves both the cost and efficiency of these designs.

The effective current limit of today's low cost TO-218 discrete transistors (250 mil die) is somewhere in the 10 to 20 A area. Once this limit is reached, the designer generally changes to the full bridge configurations shown in Figure 12-7. Because full line rather than half is applied to the primary winding, the

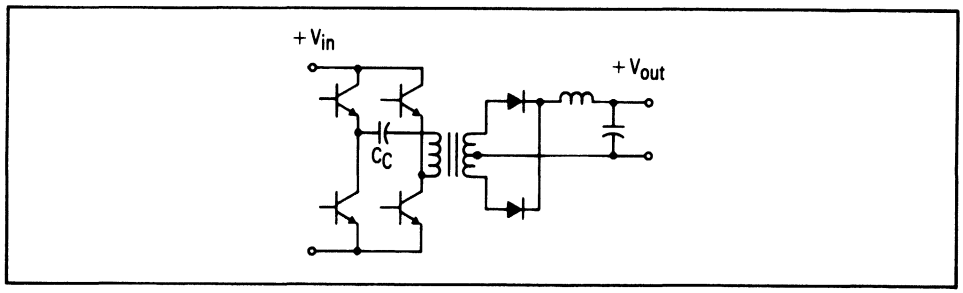


Figure 12-7. Full-Bridge Converter (200 W–1 kW)

power out can be almost double that of the half bridge with the same switching transistors. Power Darlington transistors are a logical choice for higher power control with current, voltage and speed capabilities allowing very high performance and cost effective designs. Another variation of the half bridge is the split winding circuit shown in Figure 12-5. A diode clamp can protect the lower transistor but a snubber or zener clamp must still be used to protect the top transistor from switching transients. Because both emitters are at an ac ground point, expensive drive transformers can now be replaced by lower cost capacitively coupled drive circuits.

SECTION 13
SWITCHING REGULATOR DESIGN EXAMPLES

A broad range of switching regulator power supply designs are covered in this section. Part A describes in detail the principle of operation of the MC34063 and μA78S40 switching regulator subsystems. Several converter design examples and numerous applications circuits with test data are included. Part B details the operation of the MC34129 current mode switching regulator controller, and presents an example application of this device used with Motorola SENSEFET™ products. In Part C, a 60 W flyback regulator is described which uses the MC34060 Control I.C. Part D focuses on a 400 W half bridge and a 100 W full bridge configuration in which the TL494 control I.C. is utilized.

A. THEORY AND APPLICATIONS OF THE MC34063 AND μA78S40 SWITCHING REGULATOR CONTROL CIRCUITS

The MC34063 and μA78S40 are monolithic switching regulator subsystems intended for use as dc to dc converters. These devices represent a significant advancement in the ease of implementing highly efficient and yet simple switching power supplies. The use of switching regulators is becoming more pronounced over that of linear regulators because the size reductions in new equipment designs require greater conversion efficiency. Another major advantage of the switching regulator is that it has increased application flexibility of output voltage. The output can be less than, greater than, or of opposite polarity to that of the input voltage.

Principal of Operation

In order to understand the difference in operation between linear and switching regulators we must compare the block diagrams of the two step-down regulators shown in Figure 13-1. The linear regulator consists of a stable reference, a high gain error amplifier, and a variable resistance series-pass element. The error amplifier monitors the output voltage level, compares it to the reference and generates a linear control signal that varies between two extremes, saturation and cutoff. This signal is used to vary the resistance of the series-pass element in a corrective fashion in order to maintain a constant output voltage under varying input voltage and output load conditions.

The switching regulator consists of a stable reference and a high gain error amplifier identical to that of the linear regulator. This system differs in that a free running oscillator and a gated latch have been added. The error amplifier again monitors the output voltage, compares it to the reference level and generates a control signal. If the output voltage is below nominal, the control signal will go to a high state and turn on the gate, thus allowing the oscillator clock pulses to drive the series-pass element alternately from cutoff to saturation. This will continue until the output voltage is pumped up slightly above its nominal value. At this time, the control signal will go low and turn off the gate, terminating any further switching of the series-pass element. The output voltage will eventually decrease to below nominal due to the presence of an external load, and will initiate the switching process again. The increase in conversion efficiency is

primarily due to the operation of the series-pass element only in the saturated or cutoff state. The voltage drop across the element, when saturated, is small as is the dissipation. When in cutoff, the current through the element and likewise the power dissipation are also small. There are other variations of switching control. The most common are the fixed frequency pulse width modulator and the fixed on-time variable off-time types, where the on-off switching is uninterrupted and regulation is achieved by duty cycle control. Generally speaking, the example given in Figure 13-1b does apply to MC34063 and μA78S40.

General Description

The MC34063 series is a monolithic control circuit containing all the active functions required for dc to dc converters. This device contains an internal temperature compensated reference, comparator, controlled duty cycle oscillator with an active peak current limit circuit, driver, and a high current output switch. This series was specifically designed to be incorporated in step-up, step-down and voltage-inverting converter applications. These functions are contained in an 8 pin dual in-line package shown in Figure 13-2a.

The μA78S40 is identical to the MC34063 with the addition of an on-board power catch diode, and an uncommitted operational amplifier. This device is in a 16 pin dual in-line package which allows the reference and the non-inverting input of the comparator to be pinned out. These additional features greatly enhance the flexibility of this part and allow the implementation of more sophisticated applications. These may include series-pass regulation of the main output or of a derived second output voltage, a tracking regulator configuration or even a second switching regulator.

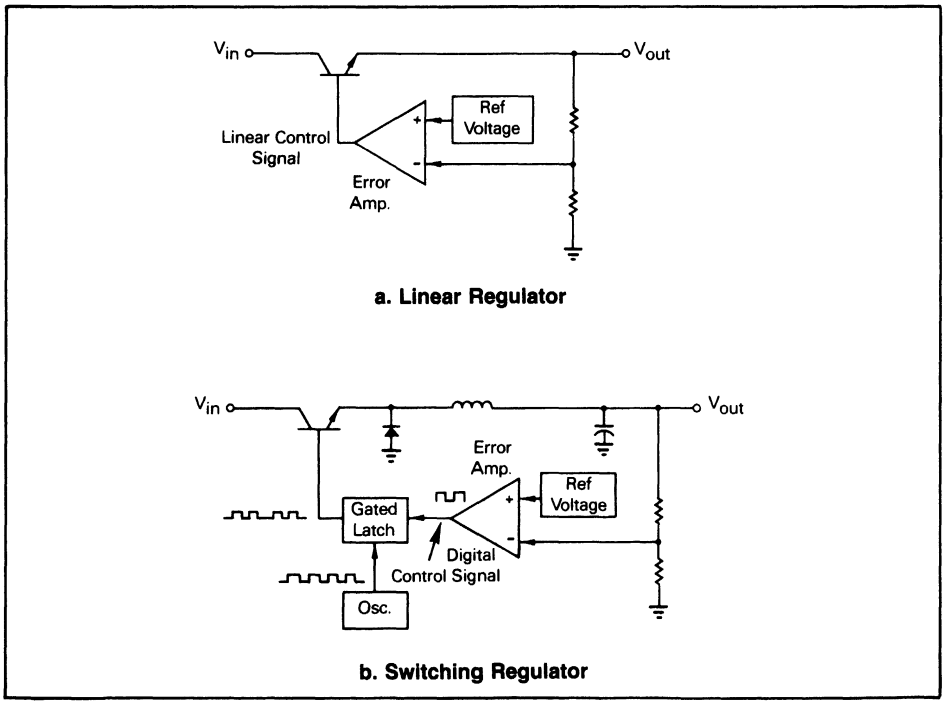


Figure 13-1. Step-Down Regulators

Functional Description

The oscillator is composed of a current source and sink which charges and discharges the external timing capacitor C_T between an upper and lower preset threshold. The typical charge and discharge currents are 35 μA and 200 μA respectively, yielding about a 1 to 6 ratio. Thus the ramp-up period is 6 times longer than that of the ramp-down as shown in Figure 13-3. The upper threshold is equal to the internal reference voltage of 1.25 volts and the lower is approximately equal to 0.75 V. The oscillator runs continuously at a rate controlled by the selected value of C_T.

During the ramp-up portion of the cycle, a Logic '1' is present at the 'A' input of the AND gate. If the output voltage of the switching regulator is below nominal, a Logic '1' will also be present at the 'B' input. This condition will set the latch and cause the 'Q' output to go to a Logic '1', enabling the driver and output switch to conduct. When the oscillator reaches its upper threshold, C_T will start to discharge and Logic '0' will be present at the 'A' input of the AND

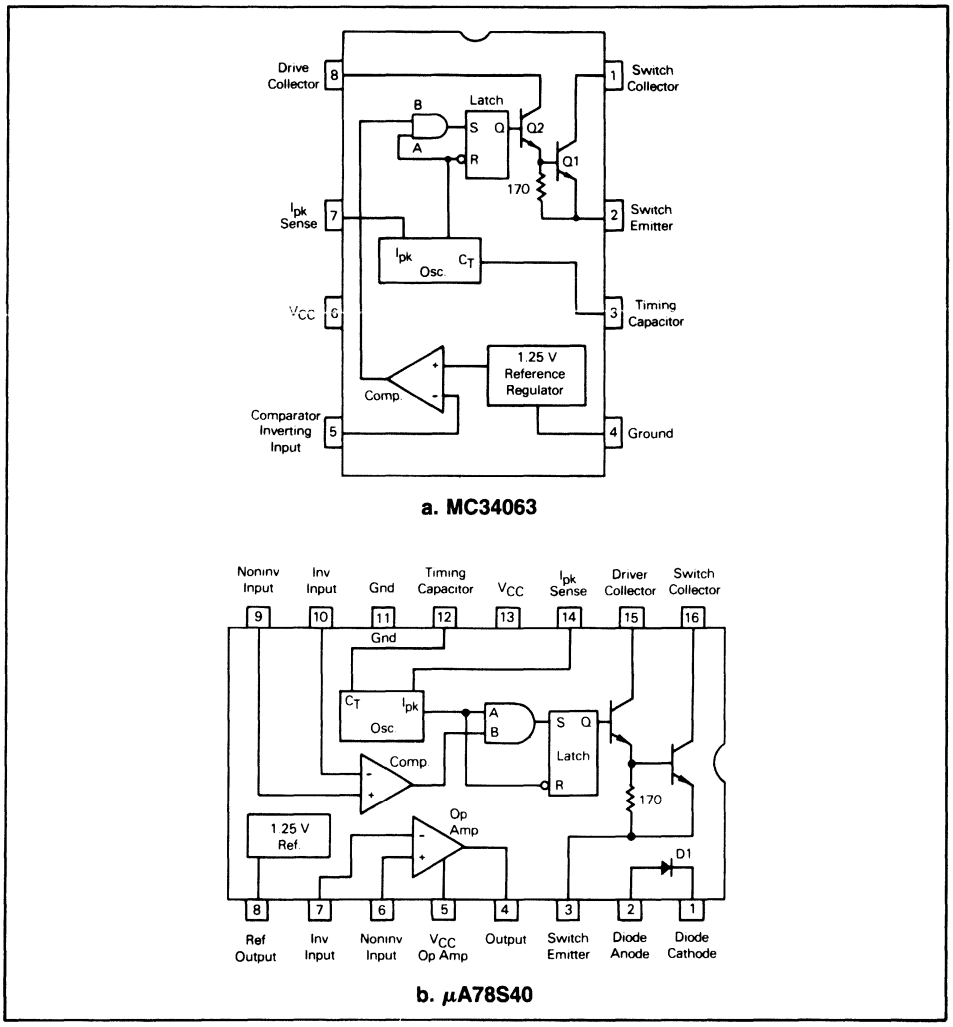


Figure 13-2. Functional Block Diagrams

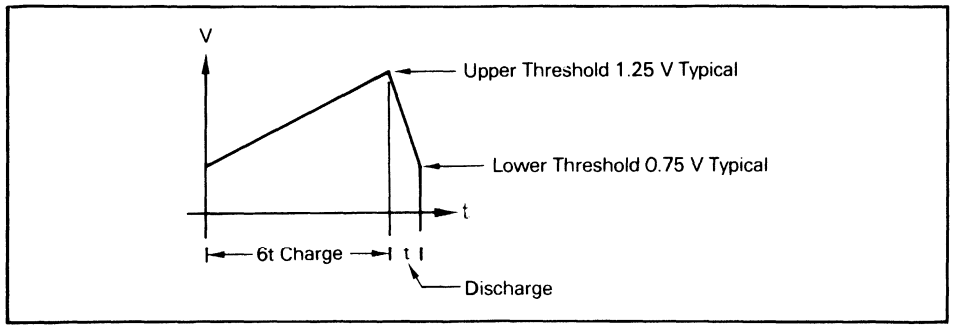


Figure 13-3. C_T Voltage Waveform

gate. This logic level is also connected to an inverter whose output presents a Logic '1' to the reset input of the latch. This condition will cause 'Q' to go low, disabling the driver and output switch. A logic truth table of these functional blocks is shown in Figure 13-4.

The output of the comparator can set the latch only during the ramp-up of C_T and can initiate a partial or full on-cycle of output switch conduction. Once the comparator has set the latch, it cannot reset it. The latch will remain set until C_T begins ramping down. Thus the comparator can initiate output switch conduction, but **cannot terminate it** and the latch is always reset when C_T **begins** ramping down. The comparator's output will be at a Logic '0' when the output voltage of the switching regulator is above nominal. Under these conditions, the comparator's output can inhibit a portion of the output switch on-cycle, a complete cycle, a complete cycle plus a portion of one cycle, multiple cycles, or multiple cycles plus a portion of one cycle.

Current limiting is accomplished by monitoring the voltage drop across an external sense resistor placed in series with V_{CC} and the output switch. The

Active Condition of Timing Capacitor C_T	AND Gate Inputs		Latch Inputs		Output Switch	Comments on State of Output Switch
	A	B	S	R		
Begins Ramp-Up	⎍	0	0	⎍	0	Switching Regulator's Output is ≥ nominal ('B' = 0).
Begins Ramp-Down	⎍	0	0	⎍	0	No change since 'B' was 0 before C_T Ramp-Down.
Ramping Down	0	⎍	0	1	0	No change even though switching regulators output < nominal. Output switch cannot be initiated during C_T Ramp-Down.
Ramping Down	0	⎍	0	1	0	No change since output switch conduction was terminated when 'A' went to 0.
Ramping Up	1	⎍	⎍	0	⎍	Swiching regulator's output went < nominal during C_T Ramp-Up ('B' → 1). Partial on-cycle for output switch.
Ramping Up	1	⎍	⎍	0	1	Switching regulators output went ≥ nominal ('B' → 0) during C_T Ramp-Up. No change since 'B' cannot reset latch.
Begins Ramp-Up	⎍	1	⎍	⎍	⎍	Complete on-cycle since 'B' was 1 before C_T started Ramp-Up.
Begins Ramp-Down	⎍	1	⎍	⎍	⎍	Output switch conduction is always terminated whenever C_T is Ramping Down.

Figure 13-4. Logic Truth Table of Functional Blocks

voltage drop developed across this resistor is monitored by the I_{pk} Sense pin. When this voltage becomes greater than 330 mV, the current limit circuitry provides an additional current path to charge the timing capacitor C_T. This causes it to rapidly reach the upper oscillator threshold, thereby shortening the time of output switch conduction and thus reducing the amount of energy stored in the inductor. This can be observed as an increase in the slope of the charging portion of the C_T voltage waveform as shown in Figure 13-5. Operation of the switching regulator in an overload or shorted condition will cause a very short but finite time of output conduction followed by either a normal or extended off-time interval provided by the oscillator ramp-down time of C_T. The extended interval is the result of charging C_T beyond the upper oscillator threshold by overdriving the current limit sense input. This can be caused by operating the switching regulator with a severely overloaded or shorted output or having the input voltage grossly above the nominal design value. Under extreme conditions, the voltage across C_T will approach V_{CC} and can cause a relatively long off-time. This action may be considered a feature since it will reduce the power dissipation of the output switch considerably. This feature may be disabled on the μA78S40 only, by connecting a small signal PNP transistor as a clamp. The emitter is connected to C_T, the base to the reference output, and the collector to ground. This will limit the maximum charge voltage across C_T to less than 2 volts. With the use of current limiting, saturation of the storage inductor may be prevented as well as achieving a soft start-up.

In practice the current limit circuit will somewhat modify the charging slope and peak amplitude of C_T each time the output switch is required to conduct. This is because the threshold voltage of the current limit sense circuit exhibits a "soft" voltage turn-on characteristic and has a turn-off time delay that causes some overshoot. The 330 mV threshold is defined where the charge and discharge

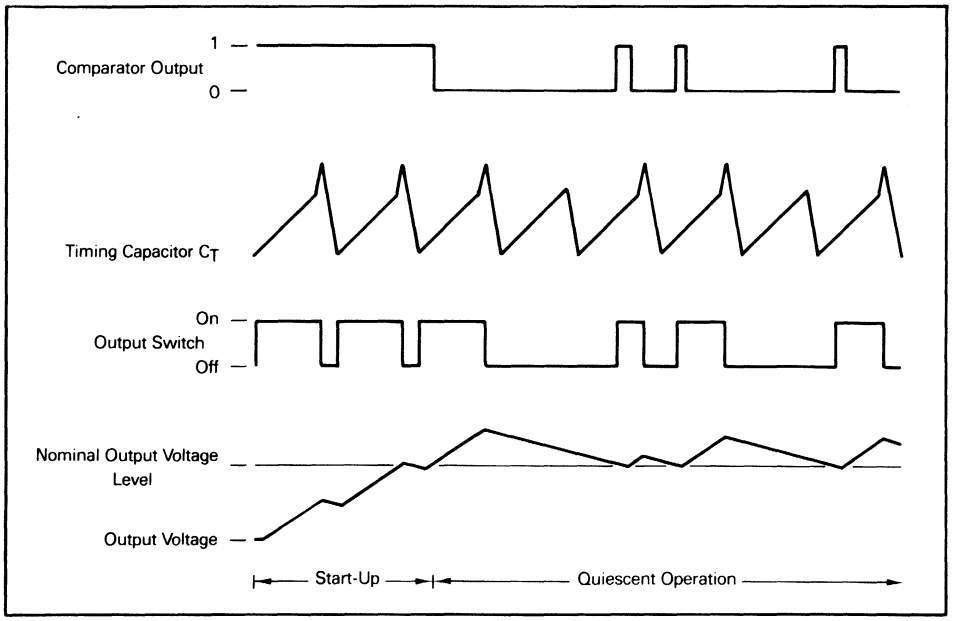


Figure 13-5. Typical Operating Waveforms

currents are of equal value with V_{CC} = 5.0 V, as shown in Figure 13-6. The current limit sense circuit can be disabled by connecting the I_{pk} Sense pin to V_{CC}.

To aid in system design flexibility, the driver collector, output switch collector and emitter are pinned out separately. This allows the designer the option of driving the output switch transistor into saturation with a selected forced gain or driving it near saturation when connected as a Darlington. The output switch has a typical current gain of 70 at 1 amp and is designed to switch a maximum of 40 volts collector-to-emitter, with up to 1.5 amps peak collector current.

The μA78S40 has the additional features of an on-chip uncommitted operational amplifier and catch diode. The op amp is a high gain single supply type with an input common-mode voltage range that includes ground. The output is capable of sourcing up to 150 mA and sinking 35 mA. A separate V_{CC} pin is provided in order to reduce the integrated circuit standby current and is useful in low power applications if the operational amplifier is not incorporated into the main switching system. The catch diode is constructed from a lateral PNP transistor and is capable of blocking up to 40 volts and will conduct currents up to 1.5 amps. There is, however, a "catch" when using it.

Because the integrated circuit substrate is common with the internal and external circuitry ground, the cathode of the diode cannot be operated much below ground or forward biasing of the substrate will result. This totally eliminates the diode from being used in the basic voltage inverting configuration as in Figure 13-15, since the substrate, pin 11, is common to ground. The diode can be considered for use only in **low power** converter applications where the total system component count must be held to a minimum. The substrate current will be about 10 percent of the catch diode current in the step-up configuration and about 20 percent in the step-down and voltage-inverting in which pin 11 is common to the negative output. System efficiency will suffer when using this diode and the package dissipation limits must be observed.

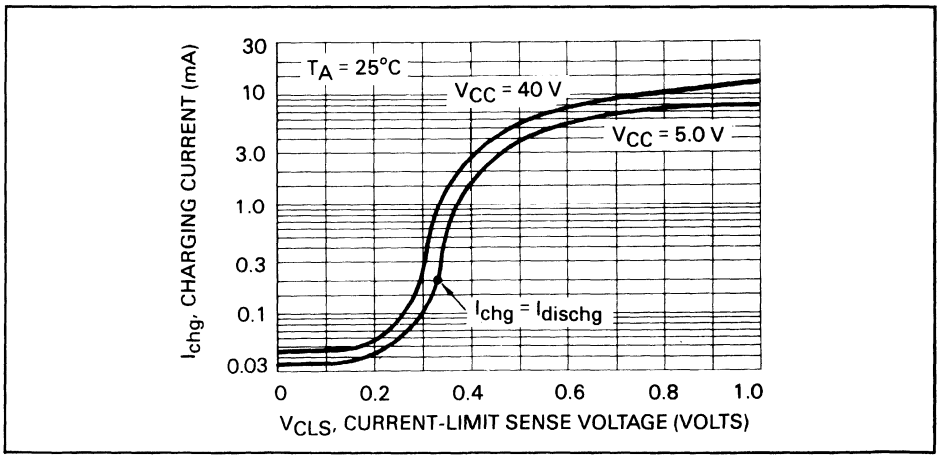


Figure 13-6. Timing Capacitor Charge Current versus Current-Limit Sense Voltage

Step-Down Switching Regulator Operation

Shown in Figure 13-7a is the basic step-down switching regulator. Transistor Q1 interrupts the input voltage and provides a variable duty cycle squarewave to a simple LC filter. The filter averages the squarewaves producing a dc output

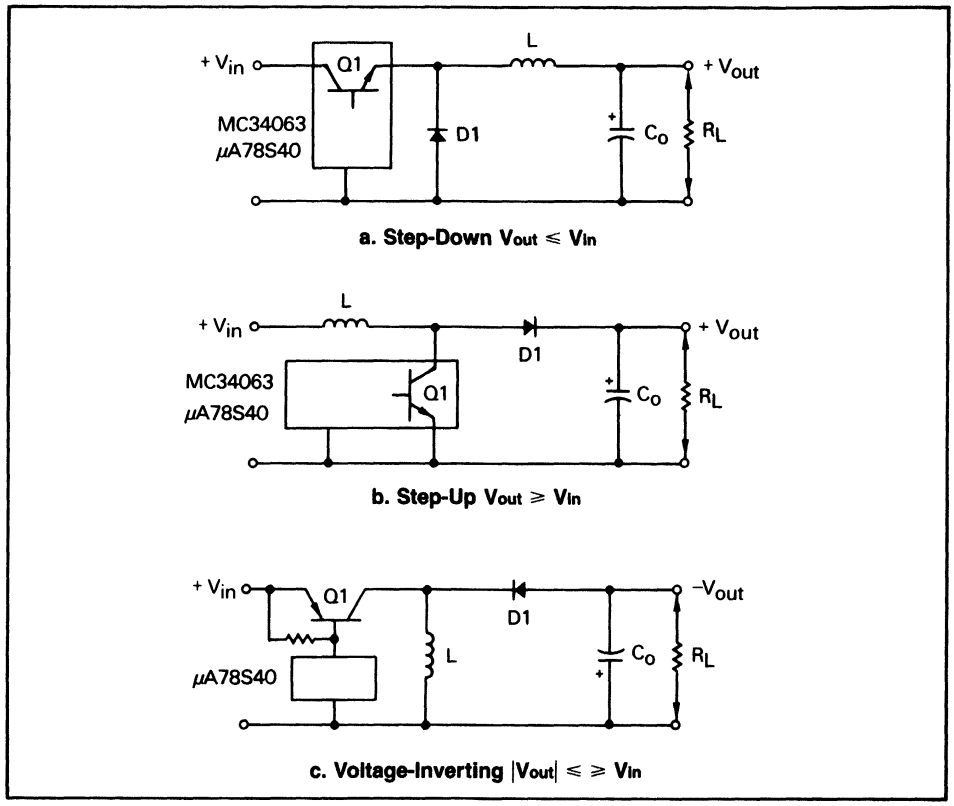


Figure 13-7. Basic Switching Regulator Configurations

voltage that can be set to any level less than the input by controlling the percent conduction time of Q1 to that of the total switching cycle time. Thus,

$$V_{out} = V_{in}\left(\% \text{ ton}\right) \text{ or } V_{out} = V_{in}\left(\frac{\text{ton}}{\text{ton} + \text{toff}}\right)$$

The MC34063/μA78S40 achieves regulation by varying the on-time and the total switching cycle time. An explanation of the step-down converter operation is as follows: Assume that the transistor Q1 is off, the inductor current I_L is zero, and the output voltage V_{out} is at its nominal value. The output voltage across capacitor C_o will eventually decay below nominal because it is the only component supply current into the external load R_L. This voltage deficiency is monitored by the switching control circuit and causes it to drive Q1 into saturation. The inductor current will start to flow from V_{in} through Q1 and, C_o in parallel with R_L, and rise at a rate of $\Delta I/\Delta T = V/L$. The voltage across the inductor is equal to $V_{in} - V_{sat} - V_{out}$ and the peak current at any instant is:

$$I_L = \left(\frac{V_{in} - V_{sat} - V_{out}}{L}\right) t$$

At the end of the on-time, Q1 is turned off. As the magnetic field in the inductor starts to collapse, it generates a reverse voltage that forward biases D1 and, the peak current will decay at a rate of $\Delta I/\Delta T = V/L$ as energy is supplied to C_o

and R_L. The voltage across the inductor during this period is equal to $V_{out} + V_F$ of D1 and, the current at any instant is:

$$I_L = I_{L(pk)} - \left(\frac{V_{out} + V_F}{L}\right) t$$

Assume that during quiescent operation the average output voltage is constant and that the system is operating in the discontinuous mode. Then $I_{L(peak)}$ attained during t_{on} must decay to zero during t_{off} and a ratio of t_{on} to t_{off} can be determined.

$$\left(\frac{V_{in} - V_{sat} - V_{out}}{L}\right) t_{on} = \left(\frac{V_{out} + V_F}{L}\right) t_{off}$$

$$\therefore \frac{t_{on}}{t_{off}} = \frac{V_{out} + V_F}{V_{in} - V_{sat} - V_{out}}$$

Note that the volt-time product of t_{on} must be equal that of t_{off} and the inductance value is not of concern when determining their ratio. If the output voltage is to remain constant, the average current into the inductor must be equal to the output current for a complete cycle. The peak inductor current with respect to output current is:

$$\left(\frac{I_{L(pk)}}{2}\right) t_{on} + \left(\frac{I_{L(pk)}}{2}\right) t_{off} = \left(I_{out}\, t_{on}\right) + \left(I_{out}\, t_{off}\right)$$

$$\frac{I_{L(pk)}(t_{on} + t_{off})}{2} = I_{out}\,(t_{on} + t_{off})$$

$$\therefore I_{L(pk)} = 2\, I_{out}$$

The peak inductor current is also equal to the peak switch current $I_{pk(switch)}$ since the two are in series. The on-time t_{on} is the maximum possible switch conduction time. It is equal to the time required for C_T to ramp up from its lower to upper threshold. The required value for C_T can be determined by using the minimum oscillator charging current and the typical value for the oscillator voltage swing both taken from the data sheet electrical characteristics table.

$$C_T = I_{chg(min)} \left(\frac{\Delta t}{\Delta V}\right)$$

$$= 20 \times 10^{-6} \left(\frac{t_{on}}{0.5}\right)$$

$$= 4.0 \times 10^{-5}\, t_{on}$$

The off-time t_{off}, is the time that diode D1 is in conduction and it is determined by the time required for the inductor current to return to zero. The off-time is **not** related to the ramp-down time of C_T. The cycle time of the LC network is equal to $t_{on(max)} + t_{off}$ and the minimum operating frequency is:

$$f_{min} = \frac{1}{t_{on(max)} + t_{off}}$$

A minimum value of inductance can now be calculated for L. The known quantities are the voltage across the inductor and the required peak current for the

selected switch conduction time.

$$L_{(min)} = \frac{V_{in} - V_{sat} - V_{out}}{I_{pk(switch)}} t_{on}$$

This minimum value of inductance was calculated by assuming the onset of continuous conduction operation with a fixed input voltage, maximum output current, and a minimum charge-current oscillator.

The net charge per cycle delivered to the output filter capacitor C_o, must be zero, $Q+ = Q-$, if the output voltage is to remain constant. The ripple voltage can be calculated from the known values of on-time, off-time, peak inductor current, and output capacitor value.

$$V_{ripple(p-p)} = \left(\frac{1}{C_o}\right) \int_0^{t_1} i\ t\ dt + \left(\frac{1}{C_o}\right) \int_{t_1}^{t_2} i'\ t\ dt$$

$$\text{Where } i\ t = \frac{\frac{1}{2} I_{pkt}}{t_{on}/2} \text{ and } i'\ t = \frac{\frac{1}{2} I_{pkt}}{t_{off}/2}$$

$$= \frac{1}{C_o} \left| \frac{I_{pk}}{t_{on}} \frac{t^2}{2} \right|_0^{t_1} + \frac{1}{C_o} \left| \frac{I_{pk}}{t_{off}} \frac{t^2}{2} \right|_{t_1}^{t_2}$$

$$\text{And } t_1 = \frac{t_{on}}{2} \text{ and } t_2 - t_1 = \frac{t_{off}}{2}$$

Substituting for t_1 and $t_2 - t_1$ yields:

$$= \frac{1}{C_o} \frac{I_{pk}}{t_{on}} \frac{(t_{on}/2)^2}{2} + \frac{1}{C_o} \frac{I_{pk}}{t_{off}} \frac{(t_{off}/2)^2}{2}$$

$$= \frac{I_{pk}\ (t_{on} + t_{off})}{8\ C_o}$$

A graphical derivation of the peak-to-peak ripple voltage can be obtained from the capacitor current and voltage waveforms in Figure 13-8.

The calculations shown account for the ripple voltage contributed by the ripple current into an ideal capacitor. In practice, the calculated value will need to be increased due to the internal equivalent series resistance ESR of the capacitor. The additional ripple voltage will be equal to $I_{pk}(ESR)$. Increasing the value of the filter capacitor will reduce the output ripple voltage. However, a point of diminishing return will be reached because the comparator requires a finite voltage difference across its inputs to control the latch. This voltage difference to completely change the latch states is about 1.5 mV and the minimum achievable ripple at the output will be the feedback divider ratio multiplied by 1.5 mV or:

$$V_{ripple(p-p)min} = \frac{V_{out}}{V_{ref}} (1.5 \times 10^{-3})$$

This problem becomes more apparent in a step-up converter with a high output voltage. Figures 13-12 and 13-13 show two different ripple reduction techniques. The first uses the μA78S40 operational amplifier to drive the comparator in the feedback loop. The second technique uses a zener diode to level shift the output down to the reference voltage.

Step-Down Switching Regulator Design Example

A schematic of the basic step-down regulator is shown in Figure 13-9. The μA78S40 was chosen in order to implement a minimum component system, however, the MC34063 with an external catch diode can also be used. The frequency chosen is a compromise between switching losses and inductor size. There will be a further discussion of this and other design considerations later. Given are the following conditions:

V_{out} = 5.0 V
I_{out} = 50 mA
f_{min} = 50 kHz
$V_{in(min)}$ = 24 V −10% or 21.6V
$V_{ripple(p-p)}$ = 0.5% V_{out} or 25 mVp-p

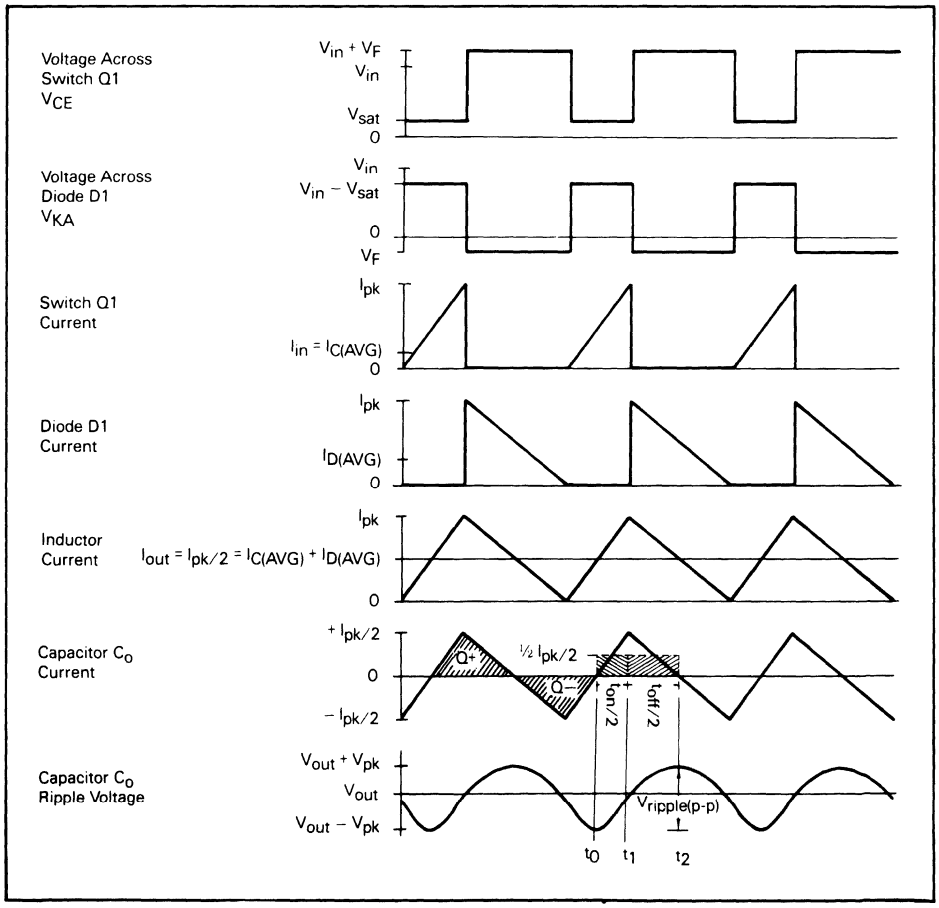


Figure 13-8. Step-Down Switching Regulator Waveforms

1. Determine the ratio of switch conduction t_{on} versus diode conduction t_{off} time.

$$\frac{t_{on}}{t_{off}} = \frac{V_{out} + V_F}{V_{in(min)} - V_{sat} - V_{out}}$$

$$= \frac{5.0 + 0.8}{21.6 - 0.8 - 5.0}$$

$$= 0.37$$

2. The cycle time of the LC network is equal to $t_{on(max)} + t_{off}$.

$$t_{on(max)} + t_{off} = \frac{1}{f_{min}}$$

$$= \frac{1}{50 \times 10^3}$$

$$= 20\ \mu s \text{ per cycle}$$

3. Next calculate t_{on} and t_{off} from the ratio of t_{on}/t_{off} in #1 and the sum of $t_{on} + t_{off}$ in #2. By using substitution and some algebraic gymnastics, an equation can be written for t_{off} in terms of t_{on}/t_{off} and $t_{on} + t_{off}$. The equation is:

$$t_{off} = \frac{t_{on(max)} + t_{off}}{\frac{t_{on}}{t_{off}} + 1}$$

$$= \frac{20 \times 10^{-6}}{0.37 + 1}$$

$$= 14.6\ \mu s$$

$$\text{Since } t_{on(max)} + t_{off} = 20\ \mu s$$

$$t_{on(max)} = 20\ \mu s - 14.6\ \mu s$$

$$= 5.4\ \mu s$$

Note that the ratio of $t_{on}/(t_{on} + t_{off})$ does not exceed the maximum of 6/7 or 0.857. This maximum is defined by the 6:1 ratio of charge-to-discharge current of timing capacitor C_T (refer to Figure 13-3).

4. The maximum on-time, $t_{on(max)}$, is set by selecting a value for C_T.

$$C_T = 4.0 \times 10^{-5}\ t_{on}$$

$$= 4.0 \times 10^{-5}\ (5.4 \times 10^{-6})$$

$$= 216\ pF$$

Use a standard 220 pF capacitor.

5. The peak switch current is:

$$I_{pk(switch)} = 2\ I_{out}$$

$$= 2\ (50 \times 10^{-3})$$

$$= 100\ mA$$

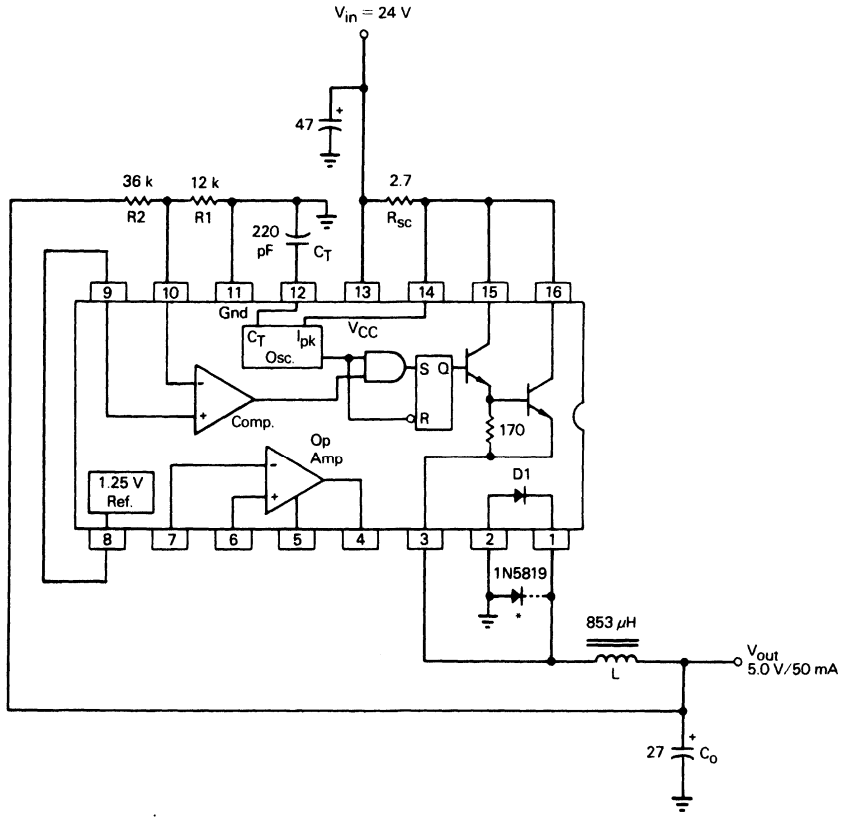
6. With knowledge of the peak switch current and maximum on time, a minimum value of inductance can be calculated.

$$L_{(min)} = \left(\frac{V_{in(min)} - V_{sat} - V_{out}}{I_{pk(switch)}}\right) t_{on(max)}$$

$$= \left(\frac{21.6 - 0.8 - 5.0}{100 \times 10^{-3}}\right) 5.4 \times 10^{-6}$$

$$= 853\ \mu H$$

7. A value for the current limit resistor R_{sc} can be determined by using the current level of $I_{pk(switch)}$ when V_{in} = 24 V.



Test	Conditions	Results
Line Regulation	V_{in} = 18 to 30 V, I_{out} = 50 mA	Δ = 16 mV or ± 0.16%
Load Regulation	V_{in} = 24 V, I_{out} = 25 to 50 mA	Δ = 28 mV or ± 0.28%
Output Ripple	V_{in} = 21.6 V, I_{out} = 50 mA	24 mV_{p-p}
Short Circuit Current	V_{in} = 24 V, R_L = 0.1 Ω	105 mA
Efficiency, Internal Diode	V_{in} = 24 V, I_{out} = 50 mA	45.3%
Efficiency, External Diode*	V_{in} = 24 V, I_{out} = 50 mA	72.6%

Figure 13-9. Step-Down Design Example

$$I'_{pk(switch)} = \left(\frac{V_{in} - V_{sat} - V_{out}}{L_{(min)}}\right) t_{on(max)}$$

$$= \left(\frac{24 - 0.8 - 5.0}{853 \times 10^{-6}}\right) 5.4 \times 10^{-6}$$

$$= 115 \text{ mA}$$

$$R_{sc} = \frac{0.33}{I'_{pk(switch)}}$$

$$= \frac{0.33}{115 \times 10^{-3}}$$

$$= 2.86\ \Omega \qquad \text{use } 2.7\ \Omega$$

This value may have to be adjusted downward to compensate for conversion losses and any increase in $I_{pk(switch)}$ current if V_{in} varies upward. Do not set R_{sc} to exceed the maximum $I_{pk(switch)}$ limit of 1.5 A when using the internal switch transistor.

8. A minimum value for an ideal output filter capacitor can now be obtained.

$$C_o = \frac{I_{pk(switch)} (t_{on} + t_{off})}{8\ V_{ripple\ (p-p)}}$$

$$= \frac{0.1\ (20 \times 10^{-6})}{8\ (25 \times 10^{-3})}$$

$$= 10\ \mu F$$

Ideally this would satisfy the design goal, however, even a solid tantalum capacitor of this value will have a typical ESR (equivalent series resistance) of 0.3 Ω which will contribute 30 mV of ripple. The ripple components are not in phase, but can be assumed to be for a conservative design. In satisfying the example shown, a 27 μF tantalum with an ESR of 0.1 Ω was selected. The ripple voltage should be kept to a low value since it will directly affect the system line and load regulation.

9. The nominal output voltage is programmed by the R1, R2 resistor divider. The output voltage is:

$$V_{out} = 1.25 \left(\frac{R2}{R1} + 1\right)$$

The divider current can go as low as 100 μA without affecting system performance. In selecting a minimum current divider R1 is equal to:

$$R1 = \frac{1.25}{100 \times 10^{-6}}$$

$$= 12{,}500\ \Omega$$

Rearranging the above equation so that R2 can be solved yields:

$$R2 = R1 \left(\frac{V_{out}}{1.25} - 1\right)$$

If a standard 5% tolerance 12 k resistor is chosen for R1, R2 will also be a standard value.

$$R2 = 12 \times 10^3 \left(\frac{5.0}{1.25} - 1\right)$$
$$= 36\ k$$

Using the above derivation, the design is optimized to meet the assumed conditions. At $V_{in(min)}$, operation is at the onset of continuous mode and the output current capability will be greater than 50 mA. At $V_{in(nom)}$ i.e.: 24 V, the current limit will activate slightly above the rated I_{out} of 50 mA.

Step-Up Switching Regulator Operation

The basic step-up switching regulator is shown in Figure 13-7B and the waveform is in Figure 13-10. Energy is stored in the inductor during the time that transistor Q1 is in the 'on' state. Upon turn-off, the energy is transferred in series with V_{in} to the output filter capacitor and load. This configuration allows the output voltage to be set to any value greater than that of the input by the following relationship:

$$V_{out} = V_{in}\left(\frac{t_{on}}{t_{off}}\right) + V_{in} \qquad \text{or} \qquad V_{out} = V_{in}\left(\frac{t_{on}}{t_{off}} + 1\right)$$

An explanation of the step-up converter's operation is as follows: Initially, assume that transistor Q1 is off, the inductor current is zero, and the output voltage is at its nominal value. At this time, load current is being supplied only by C_o and it will eventually fall below nominal. This deficiency will be sensed by the control circuit and it will initiate an on-cycle, driving Q1 into saturation. Current will start to flow from V_{in} through the inductor and Q1 and rise at a rate of $\Delta I/\Delta T = V/L$. The voltage across the inductor is equal to $V_{in} - V_{sat}$ and the peak current is:

$$I_L = \left(\frac{V_{in} - V_{sat}}{L}\right) t$$

When the on-time is completed, Q1 will turn off and the magnetic field in the inductor will start to collapse generating a reverse voltage that forward biases D1, supplying energy to C_o and R_L. The inductor current will decay at a rate of $\Delta I/\Delta T = V/L$ and the voltage across it is equal to $V_{out} + V_F - V_{in}$. The current at any instant is:

$$I_L = I_{L(pk)} - \left(\frac{V_{out} + V_F - V_{in}}{L}\right) t$$

Assuming that the system is operating in the discontinuous mode, the current through the inductor will reach zero after the t_{off} period is completed. Then $I_{L(pk)}$ attained during t_{on} must decay to zero during t_{off} and a ratio of t_{on} to t_{off} can be written.

$$\left(\frac{V_{in} - V_{sat}}{L}\right) t_{on} = \left(\frac{V_{out} + V_F - V_{in}}{L}\right) t_{off}$$
$$\therefore \frac{t_{on}}{t_{off}} = \frac{V_{out} + V_F - V_{in}}{V_{in} - V_{sat}}$$

Note again, that the volt-time product of t_{on} must be equal to that of t_{off} and the inductance value does not affect this relationship.

The inductor current charges the output filter capacitor through diode D1 only during t_{off}. If the output voltage is to remain constant, the net charge per cycle delivered to the output filter capacitor must be zero, $Q+ = Q-$.

$$I_{chg}\ t_{off} = I_{dischg}\ t_{on}$$

Figure 13-10 shows the step-up switching regulator waveforms. By observing the capacitor current and making some substitutions in the above statement, a formula for peak inductor current can be obtained.

$$\left(\frac{I_{L\,(pk)}}{2}\right) t_{off} = I_{out}\,(t_{on} + t_{off})$$

$$I_{L(pk)} = 2\ I_{out}\left(\frac{t_{on}}{t_{off}} + 1\right)$$

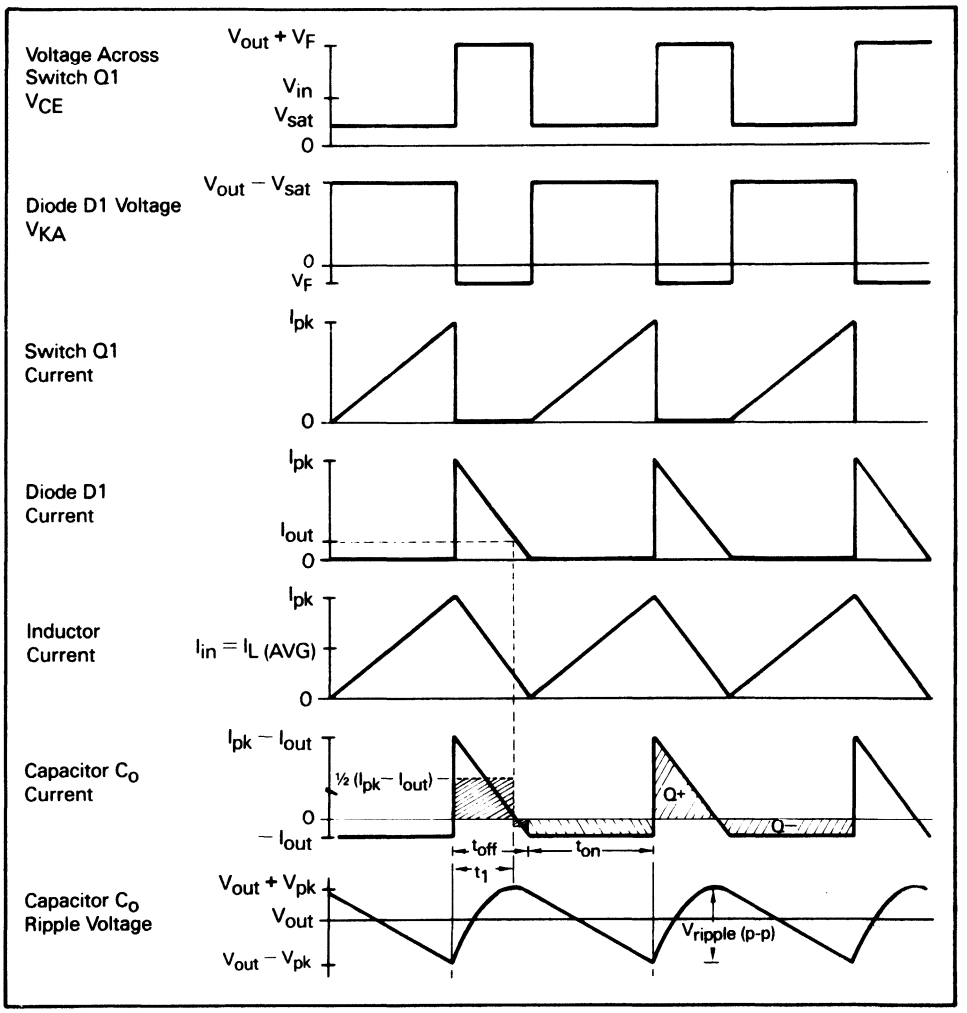


Figure 13-10. Step-Up Switching Regulator Waveforms

The peak inductor current is also equal to the peak switch current, since the two are in series.

With knowledge of the voltage across the inductor during t_{on} and the required peak current for the selected switch conduction time, a minimum inductance value can be determined.

$$L_{(min)} = \left(\frac{V_{in} - V_{sat}}{I_{pk(switch)}}\right) t_{on(max)}$$

The ripple voltage can be calculated from the known values of on-time, off-time, peak inductor current, output current and output capacitor value. Referring to the capacitor current waveforms in Figure 13-10, t_1 is defined as the capacitor charging interval. Solving for t_1 in known terms yields:

$$\frac{I_{pk} - I_{out}}{t_1} = \frac{I_{pk}}{t_{off}}$$

$$\therefore t_1 = \left(\frac{I_{pk} - I_{out}}{I_{pk}}\right) t_{off}$$

And the current during t_1 can be written:

$$I = \left(\frac{I_{pk} - I_{out}}{t_1}\right) t$$

The ripple voltage is:

$$V_{ripple(p-p)} = \left(\frac{1}{C_o}\right) \int_0^{t_1} \frac{I_{pk} - I_{out}}{t_1} t \, dt$$

$$= \frac{1}{C_o} \left| \frac{I_{pk} - I_{out}}{t_1} \frac{t^2}{2} \right|_0^{t_1}$$

$$= \frac{1}{C_o} \frac{(I_{pk} - I_{out})}{2} t_1$$

Substituting for t_1 yields:

$$= \frac{1}{C_o} \frac{(I_{pk} - I_{out})}{2} \frac{(I_{pk} - I_{out})}{I_{pk}} t_{off}$$

$$= \frac{(I_{pk} - I_{out})^2 t_{off}}{2 I_{pk} C_o}$$

A simplified formula that will give an error of less than 5% for a voltage step-up greater than 3 with an ideal capacitor is shown:

$$V_{ripple(p-p)} \approx \left(\frac{I_{out}}{C_o}\right) t_{on}$$

This neglects a small portion of the total Q− area. The area neglected is equal to:

$$A = (t_{off} - t_1) \frac{I_{out}}{2}$$

Step-Up Switching Regulator Design Example

The basic step-up regulator schematic is shown in Figure 13-11. The μA78S40 again was chosen in order to implement a minimum component system. The following conditions are given:

V_{out} = 28 V
I_{out} = 50 mA
f_{min} = 50 kHz
$V_{in(min)}$ = 9.0 V − 25% or 6.75 V
$V_{ripple(p\text{-}p)}$ = 0.5% V_{out} or 140 mVp-p

1. Determine the ratio of switch conduction t_{on} versus diode conduction t_{off} time.

$$\frac{t_{on}}{t_{off}} = \frac{V_{out} + V_F = V_{in(min)}}{V_{in(min)} - V_{sat}}$$

$$= \frac{28 + 0.8 - 6.75}{6.75 - 0.3}$$

$$= 3.42$$

2. The cycle time of the LC network is equal to $t_{on(max)} + t_{off}$.

$$t_{on(max)} + t_{off} = \frac{1}{f_{min}}$$

$$= \frac{1}{50 \times 10^3}$$

$$= 20\ \mu s \text{ per cycle}$$

3. Next calculate t_{on} and t_{off} from the ratio of t_{on}/t_{off} in #1 and the sum of $t_{on} + t_{off}$ in #2.

$$t_{off} = \frac{20 \times 10^{-6}}{3.42 + 1}$$

$$= 4.5\ \mu s$$

$$t_{on} = 20\ \mu s - 4.5\ \mu s$$

$$= 15.5\ \mu s$$

Note that the ratio of $t_{on}/(t_{on} + t_{off})$ does not exceed the maximum of 0.857.

4. The maximum on-time, $t_{on(max)}$, is set by selecting a value for C_T.

$$C_T = 4.0 \times 10^{-5}\ t_{on}$$
$$= 4.0 \times 10^{-5}\ (15.5 \times 10^{-6})$$
$$= 620\ pF$$

5. The peak switch current is:

$$I_{pk(switch)} = 2\ I_{out} \left(\frac{t_{on}}{t_{off}} + 1 \right)$$

$$= 2\ (50 \times 10^{-3})\ (3.42 + 1)$$

$$= 442\ mA$$

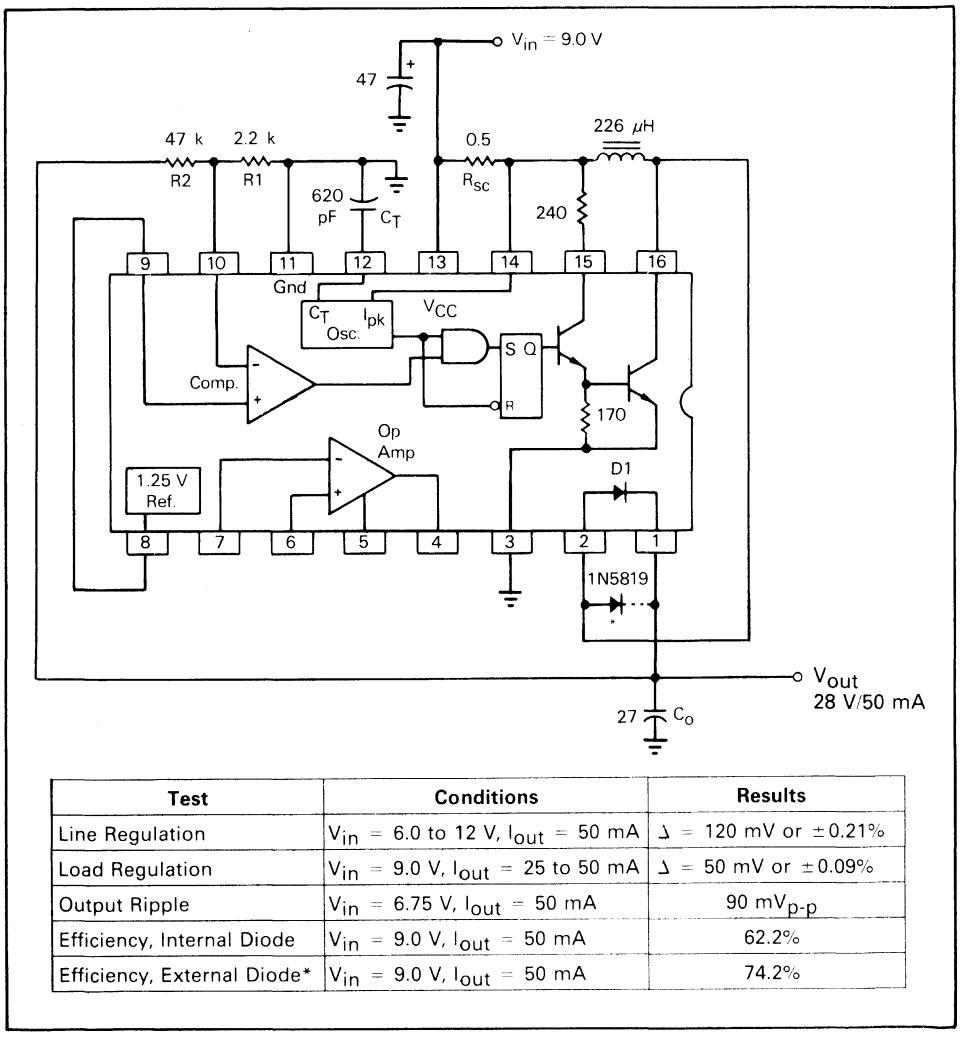
6. A minimum value of inductance can be calculated since the maximum on-time and peak switch current are known.

$$L_{(min)} = \left(\frac{V_{in(min)} - V_{sat}}{I_{pk(switch)}}\right) t_{on}$$

$$= \left(\frac{6.75 - 0.3}{442 \times 10^{-3}}\right) 15.5 \times 10^{-6}$$

$$= 226\ \mu H$$

7. A value for the current limit resistor, R_{sc}, can now be determined by using the current level of $I_{pk(switch)}$ when $V_{in} = 9.0$ V.



Test	Conditions	Results
Line Regulation	V_{in} = 6.0 to 12 V, I_{out} = 50 mA	Δ = 120 mV or ±0.21%
Load Regulation	V_{in} = 9.0 V, I_{out} = 25 to 50 mA	Δ = 50 mV or ±0.09%
Output Ripple	V_{in} = 6.75 V, I_{out} = 50 mA	90 mV_{p-p}
Efficiency, Internal Diode	V_{in} = 9.0 V, I_{out} = 50 mA	62.2%
Efficiency, External Diode*	V_{in} = 9.0 V, I_{out} = 50 mA	74.2%

Figure 13-11. Step-Up Design Example

$$I'_{pk(switch)} = \left(\frac{V_{in} - V_{sat}}{L_{(min)}}\right) t_{on(max)}$$

$$= \left(\frac{9.0 - 0.3}{226 \times 10^{-6}}\right) 15.5 \times 10^{-6}$$

$$= 597 \text{ mA}$$

$$R_{sc} = \frac{0.33}{I'_{pk(switch)}}$$

$$= \frac{0.33}{597 \times 10^{-3}}$$

$$= 0.55\ \Omega \qquad \text{use } 0.5\ \Omega$$

Note that current limiting in this basic step-up configuration will **only** protect the switch transistor from overcurrent due to inductor saturation. If the output is severely overloaded or shorted D1, L, or R_{sc} may be destroyed since they form a direct path from V_{in} to V_{out}. Protection may be achieved by current limiting V_{in} or replacing the inductor with 1:1 turns ratio transformer.

8. An approximate value for an ideal output filter capacitor is:

$$C_o \approx \frac{I_{out}}{V_{ripple(p-p)}} t_{on}$$

$$\approx \frac{50 \times 10^{-3}}{140 \times 10^{-3}} 15.5 \times 10^{-6}$$

$$\approx 5.5\ \mu F$$

The ripple contribution due to the gain of the comparator:

$$V_{ripple(p-p)} = \frac{V_{out}}{V_{ref}} 1.5 \times 10^{-3}$$

$$= \frac{28}{1.25} 1.5 \times 10^{-3}$$

$$= 33.6 \text{ mV}$$

A 27 μF tantalum capacitor with an ESR of 0.10 Ω was again chosen. The ripple voltage due to the capacitance value is 28.7 mV and 44.2 mV due to ESR. This yields a total ripple voltage of:

$$E_{ripple(p-p)} = \frac{V_{out}}{V_{ref}} 1.5 \times 10^{-3} + \frac{I_{out}}{C_o} t_{on} + I_{pk}\ ESR$$

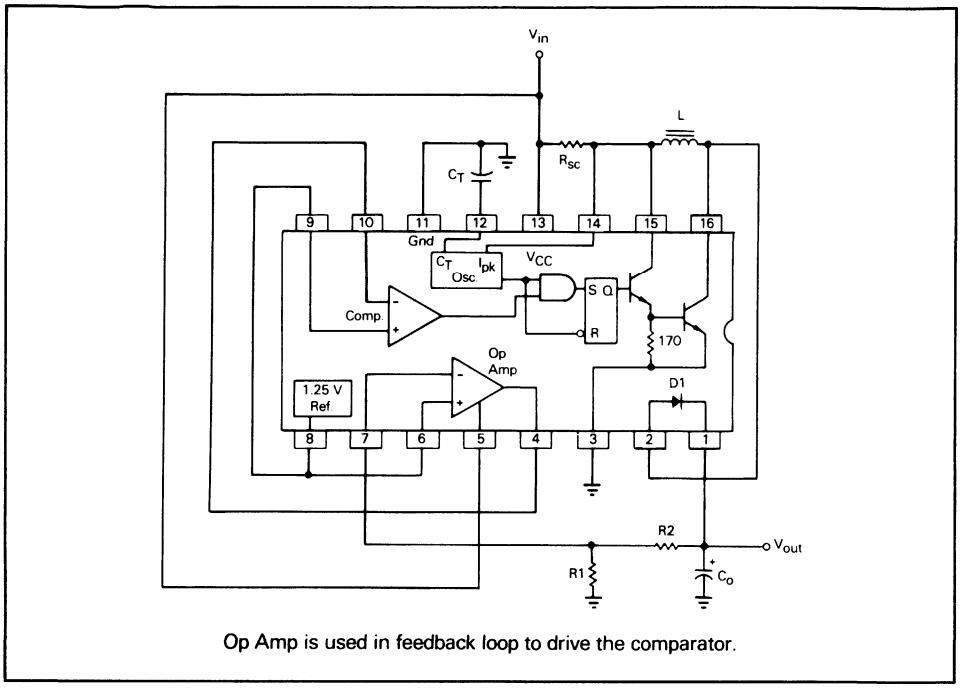
$$= 33.6 \text{ mV} + 28.7 \text{ mV} + 44.2 \text{ mV}$$

$$= 107 \text{ mV}$$

9. The nominal output voltage is programmed by the R1, R2 divider.

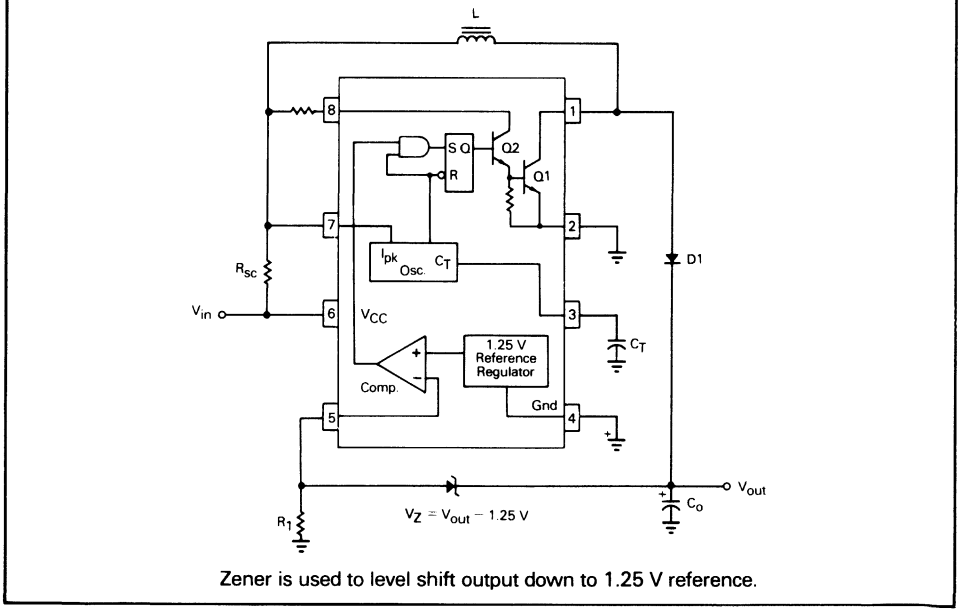
$$V_{out} = 1.25\left(1 + \frac{R2}{R1}\right)$$

A standard 5% tolerance, 2.2 k resistor was selected for R1 so that the divider current is about 500 μA.



Op Amp is used in feedback loop to drive the comparator.

Figure 13-12. μA78S40 Ripple Reduction Technique



Zener is used to level shift output down to 1.25 V reference.

Figure 13-13. MC34063 Ripple Reduction Technique

$$R1 = \frac{1.25}{500 \times 10^{-6}}$$

$$= 2500\ \Omega \qquad \text{use } 2.2\text{ k}$$

$$\text{Then } R2 = R1\left(\frac{V_{out}}{1.25} - 1\right)$$

$$= 2200\left(\frac{28}{1.25} - 1\right)$$

$$= 47{,}080\ \Omega \qquad \text{use } 47\text{ k}$$

10. In this design example, the output switch transistor is driven into saturation with a forced gain of 20 at an input voltage of 7.0 V. The required base drive is:

$$I_B = \frac{I_{pk(switch)}}{B_f}$$

$$= \frac{442 \times 10^{-3}}{20}$$

$$= 22.1\text{ mA}$$

The current required to drive the internal 170 Ω base-emitter resistor is:

$$I_{170\,\Omega} = \frac{V_{BE(switch)}}{170}$$

$$= \frac{0.7}{170}$$

$$= 4.1\text{ mA}$$

The driver collector current is equal to sum of 22.1 mA + 4.1 mA = 26.2 mA. Allow 0.3 V for driver saturation and 0.2 V for the drop across R_{sc} (0.5 x 442 mA I_{pk}).

Then the driver collector resistor is equal to:

$$R_{driver} = \frac{V_{in} - V_{sat(driver)} - V_{RSC}}{I_B + I_{170\,\Omega}}$$

$$= \frac{7.0 - 0.3 - 0.2}{(22.1 + 4.1) \times 10^{-3}}$$

$$= 248\ \Omega \qquad \text{use } 240\ \Omega$$

Voltage-Inverting Switching Regulator Operation

The basic voltage-inverting switching regulator is shown in Figure 13-7c and the operating waveforms are in Figure 13-14. Energy is stored in the inductor during the conduction time of Q1. Upon turn-off, the energy is transferred to the output filter capacitor and load. Notice that in this configuration the output voltage is derived only from the inductor. This allows the magnitude of the output to be set to any value. It may be less than, equal to, or greater than that of the input and is set by the following relationship:

$$V_{out} = V_{in}\left(\frac{t_{on}}{t_{off}}\right)$$

The voltage-inverting converter operates almost identically to that of the step-up previously discussed. The voltage across the inductor during t_{on} is $V_{in} - V_{sat}$ but during t_{off}, the voltage is equal to the negative magnitude of $V_{out} + V_F$. Remembering that the volt-time product of t_{on} must be equal to that of t_{off}, a ratio of t_{on} to t_{off} can be determined.

$$(V_{in} - V_{sat})\, t_{on} = (|V_{out}| + V_F)\, t_{off}$$

$$\therefore \frac{t_{on}}{t_{off}} = \frac{|V_{out}| + V_F}{V_{in} - V_{sat}}$$

The derivations and the formulas for $I_{pk(switch)}$, $L_{(min)}$, and C_o are the same as that of the step-up converter.

Voltage-Inverting Switching Regulator Design Example

A circuit diagram of the basic voltage-inverting regulator is shown in Figure 13-15.

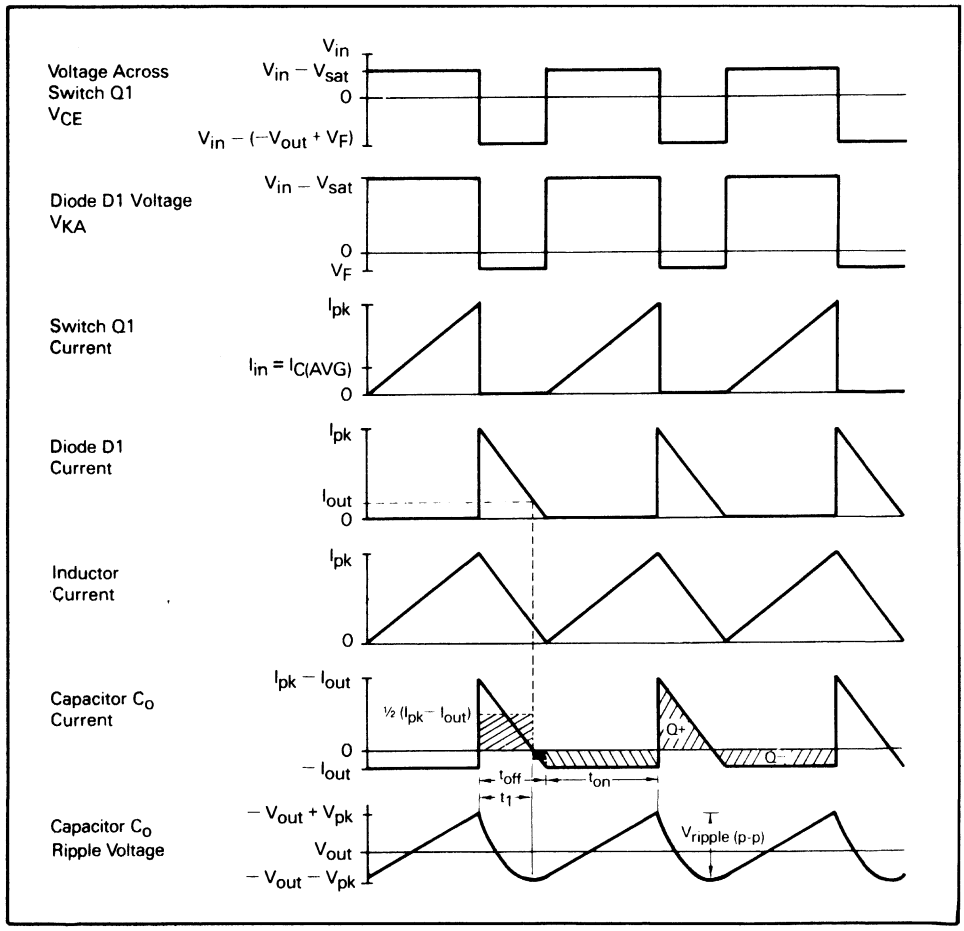


Figure 13-14. Voltage-Inverting Switching Regulator Waveforms

The μA78S40 was selected for this design since it has the reference and both comparator inputs pinned out. The following operating conditions are given:

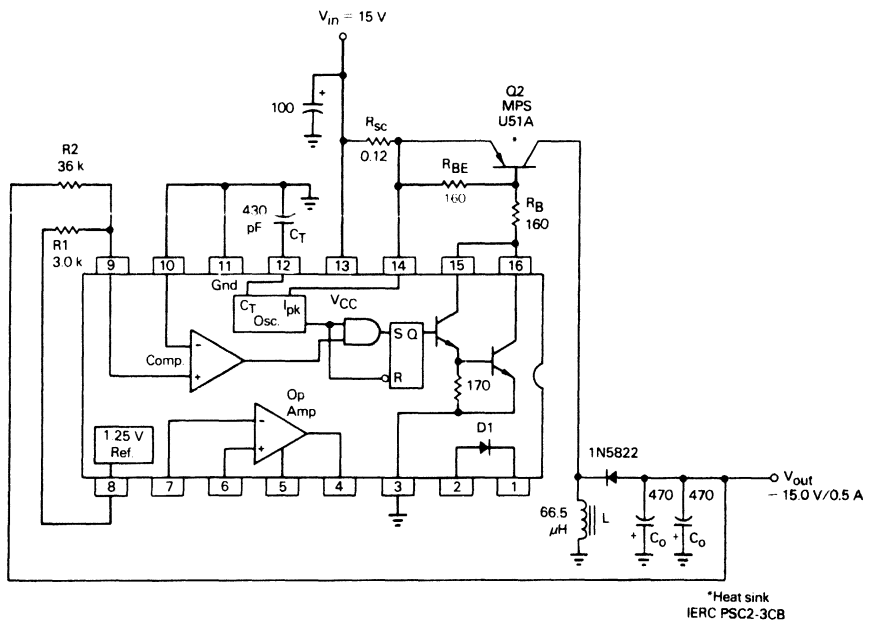
$V_{out} = -15$ V
$I_{out} = 500$ mA
$f_{min} = 50$ kHz
$V_{in(min)} = 15$ V $- 10\%$ or 13.5 V
$V_{ripple(p\text{-}p)} = 0.4\%$ V_{out} or 60 mVp-p

1. Determine the ratio of switch conduction ton versus diode conductions toff time.

$$\frac{ton}{toff} = \frac{|V_{out}| + V_F}{V_{in} - V_{sat}}$$

$$= \frac{15 + 0.8}{13.5 - 0.8}$$

$$= 1.24$$



Test	Conditions	Results
Line Regulation	V_{in} = 12 to 16 V, I_{out} = 0.5 A	Δ = 3.0 mV or ± 0.01%
Load Regulation	V_{in} = 15 V, I_{out} = 0.1 to 0.5 A	Δ = 27 mV or ± 0.09%
Output Ripple	V_{in} = 13.5 V, I_{out} = 0.5 A	35 $mV_{p\text{-}p}$
Short Circuit Current	V_{in} = 15 V, R_L = 0.1 Ω	2.5 A
Efficiency	V_{in} = 15 V, I_{out} = 0.5 A	80.6%

Figure 13-15. Voltage-Inverting Design Example

2. The cycle time of the LC network is equal to $t_{on(max)} + t_{off}$.

$$t_{on(max)} + t_{off} = \frac{1}{f_{min}}$$

$$= \frac{1}{50 \times 10^3}$$

$$= 20\ \mu s$$

3. Calculate t_{on} and t_{off} from the ratio of t_{on}/t_{off} in #1 and the sum of $t_{on} + t_{off}$ in #2.

$$t_{off} = \frac{20 \times 10^{-6}}{1.24 + 1}$$

$$= 8.9\ \mu s$$

$$t_{on} = 20\ \mu s - 8.9\ \mu s$$

$$= 11.1\ \mu s$$

Note again that the ratio of $t_{on}/(t_{on} + t_{off})$ does not exceed the maximum of 0.857

4. A value of C_T must be selected in order to set $t_{on(max)}$.

$$C_T = 4.0 \times 10^{-5}\ t_{on}$$
$$= 4.0 \times 10^{-5}\ (11.1 \times 10^{-6})$$
$$= 444\ pF \qquad \text{use } 430\ pF$$

5. The peak switch current is:

$$I_{pk(switch)} = 2\ I_{out}\left(\frac{t_{on}}{t_{off}} + 1\right)$$

$$= 2\ (500 \times 10^{-3})\ (1.24 + 1)$$

$$= 2.24\ A$$

6. The minimum required inductance value is:

$$L_{(min)} = \left(\frac{V_{in(min)} - V_{sat}}{I_{pk(switch)}}\right) t_{on}$$

$$= \left(\frac{13.5 - 0.8}{2.24}\right) 11.1 \times 10^{-6}$$

$$= 66.5\ \mu H$$

7. The current-limit resistor value was selected by determining the level of $I_{pk(switch)}$ for $V_{in} = 16.5$ V.

$$I'_{pk(switch)} = \left(\frac{V_{in} - V_{sat}}{L_{(min)}}\right) t_{on}$$

$$= \left(\frac{16.5 - 0.8}{66.5 \times 10^{-6}}\right) 11.1 \times 10^{-6}$$

$$= 2.62\ A$$

$$R_{sc} = \frac{0.33}{I'_{pk(switch)}}$$

$$= \frac{0.33}{2.62}$$

$$= 0.13\ \Omega \qquad \text{use } 0.12\ \Omega$$

8. An approximate value for an ideal output filter capacitor is:

$$C_o \approx \left(\frac{I_{out}}{V_{ripple(p\text{-}p)}}\right) t_{on}$$

$$\approx \frac{0.5}{60 \times 10^{-3}} 11.1 \times 10^{-6}$$

$$\approx 92.5\ \mu F$$

The ripple contribution due to the gain of the comparator is:

$$V_{ripple(p\text{-}p)} = \frac{|V_{out}|}{V_{ref}} 1.5 \times 10^{-3}$$

$$= \frac{15}{1.25} 1.5 \times 10^{-3}$$

$$= 18\ mV$$

For a given level of ripple, the ESR of the output filter capacitor becomes the dominant factor in choosing a value for capacitance. Therefore two 470 μF capacitors with an ESR of 0.020 Ω each was chosen. The ripple voltage due to the capacitance value is 5.9 mV and 22.4 mV due to ESR. This yields a total ripple voltage of:

$$E_{ripple(p\text{-}p)} = \frac{|V_{out}|}{V_{ref}} 1.5 \times 10^{-3} + \frac{I_{out}}{C_o} t_{on} + I_{pk}\ ESR$$

$$= 18\ mV + 5.9\ mV + 22.4\ mV$$

$$= 46.3\ mV$$

9. The nominal output voltage is programmed by the R1, R2 divider. Note that with a negative output voltage, the inverting input of the comparator is referenced to ground. Therefore, the voltage at the junction of R1, R2 and the noninverting input must also be at ground potential when V_{out} is in regulation. The magnitude of V_{out} is:

$$|V_{out}| = 1.25 \frac{R2}{R1}$$

A divider current of about 400 μA was desired for this example.

$$R1 = \frac{1.25}{400 \times 10^{-6}}$$

$$= 3{,}125\ \Omega \qquad \text{use } 3.0\ k$$

$$\text{Then } R2 = \frac{|V_{out}|}{1.25} R1$$

$$= \frac{15}{1.25} 3.0 \times 10^{3}$$

$$= 36\ k$$

10. Output switch transistor Q2 is driven into a soft saturation with a forced gain of 35 at an input voltage of 13.5 V in order to enhance the turn-off switching time. The required base drive is:

$$I_B = \frac{I_{pk(switch)}}{B_f}$$

$$= \frac{2.24}{35}$$

$$= 64 \text{ mA}$$

The value for the base-emitter turn-off resistor R_{BE} is determined by:

$$R_{BE} = \frac{10\ B_f}{I_{pk(switch)}}$$

$$= \frac{10\ (35)}{2.24}$$

$$= 156.3\ \Omega \qquad \text{use } 160\ \Omega$$

The additional base current required due to R_{BE} is:

$$I_{R_{BE}} = \frac{V_{BE}\ (Q2)}{R_{BE}}$$

$$= \frac{0.8}{160}$$

$$= 5.0 \text{ mA}$$

Then I_B (Q2) is equal to the sum of 64 mA + 5.0 mA = 69 mA. Allow 0.8 V for the IC driver saturation and 0.3 V for the drop across R_{sc} (0.12 x 2.24 A I_{pk}).

Then the base driver resistor is equal to:

$$R_B = \frac{V_{in(min)} - V_{sat\ (IC)} - V_{RSC} - V_{BE\ (Q2)}}{I_B + I_{160\ \Omega}}$$

$$= \frac{13.5 - 0.8 - 0.3 - 1.0}{(64 + 5) \times 10^{-3}}$$

$$= 165.2\ \Omega \qquad \text{use } 160\ \Omega$$

Step Up/Down Switching Regulator Operation

When designing at the board level it sometimes becomes necessary to generate a constant output voltage that is less than that of the battery. The step-down circuit shown in Figure 13-16a will perform this function efficiently. However, as the battery discharges, its terminal voltage will eventually fall below the desired output, and in order to utilize the remaining battery energy the step-up circuit shown in Figure 13-16b will be required.

General Applications

By combining circuits a and b a unique step-up/down configuration can be created (Figure 13-17) which still employs a *simple inductor* for the voltage

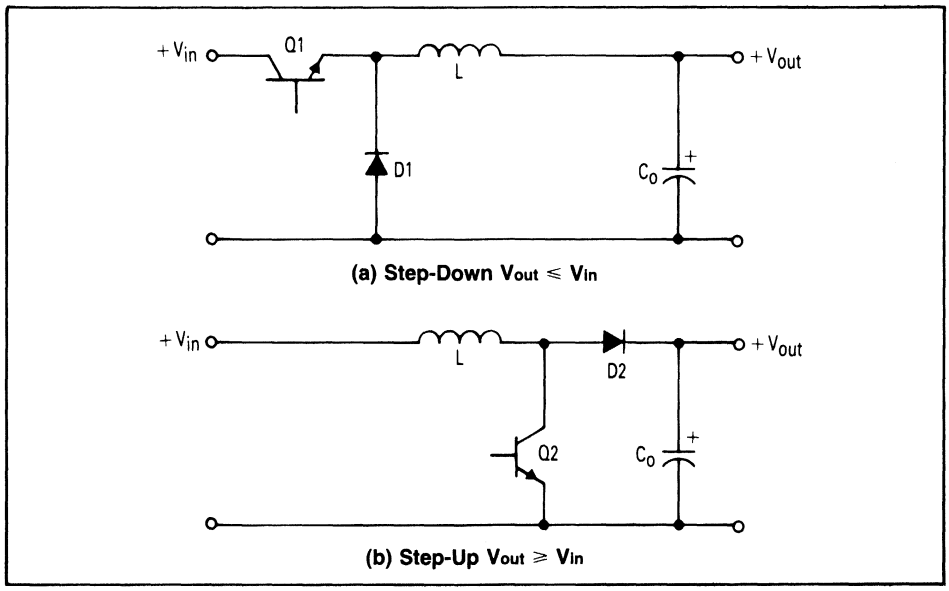


Figure 13-16. Basic Switching Regulator Configurations

transformation. Energy is stored in the inductor during the time that transistors Q1 and Q2 are in the 'on' state. Upon turn-off, the energy is transferred to the output filter capacitor and load forward biasing diodes D1 and D2. Note that during t_{on} this circuit is identical to the basic step-up, but during t_{off} the output voltage is derived only from the inductor and is with respect to ground instead of V_{in}. This allows the output voltage to be set to any value, thus it may be less than, equal to, or greater than that of the input. Current limit protection cannot be employed in the basic step-up circuit. If the output is severely overloaded or shorted L or D2 may be destroyed since they form a direct path from V_{in} to V_{out}. The step-up/down configuration allows the control circuit to implement current limiting because Q1 is now in series with V_{out}, as is in the step-down circuit.

Step Up/Down Switching Regulator Design Example

A complete step-up/down switching regulator design example is shown in Figure 13-18. An external switch transistor was used to perform the function of

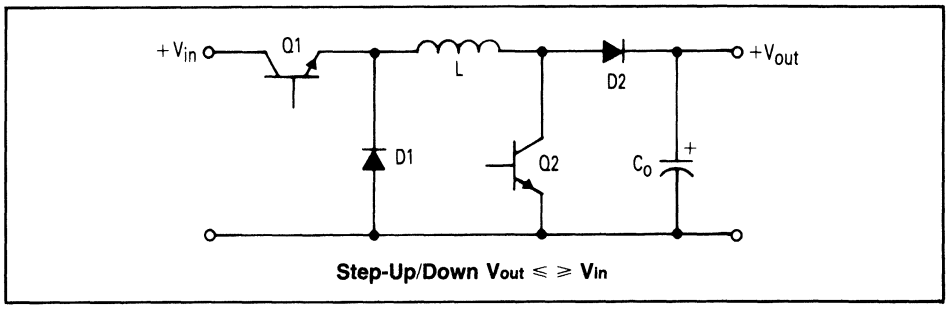


Figure 13-17. Combined Configuration

Q2. This regulator was designed to operate from a standard 12 V battery pack with the following conditions:

V_{in} = 7.5 to 14.5 V V_{out} = 10 V
f_{min} = 50 kHz I_{out} = 120 mA
$V_{ripple(p\text{-}p)}$ = 1% V_{out} or 100 $mV_{p\text{-}p}$

The following design procedure is provided so that the user can select proper component values for his specific converter application.

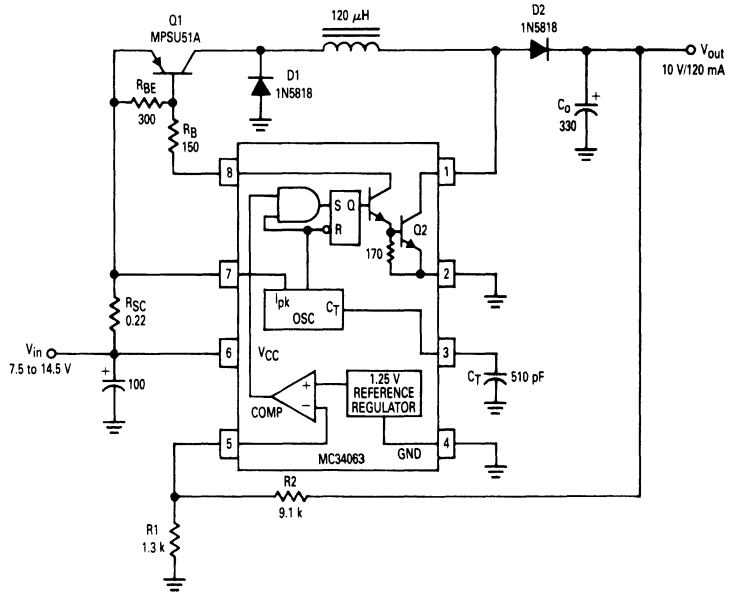
1) Determine the ratio of switch conduction t_{on} versus diode conduction t_{off} time.

$$\frac{t_{on}}{t_{off}} = \frac{V_{out} + V_{FD1} + V_{FD2}}{V_{in(min)} - V_{satQ1} - V_{satQ2}}$$

$$= \frac{10 + 0.6 + 0.6}{7.5 - 0.8 - 0.8}$$

$$= 1.9$$

2) The cycle time of the LC network is equal to $t_{on(max)} + t_{off}$.



Test	Conditions	Results
Line Regulation	V_{in} = 7.5 to 14.5 V, I_{out} = 120 mA	Δ = 22 mV or ± 0.11%
Load Regulation	V_{in} = 12.6 V, I_{out} = 10 to 120 mA	Δ = 3 mV or ± 0.015%
Output Ripple	V_{in} = 12.6 V, I_{out} = 120 mA	95 $mV_{p\text{-}p}$
Short Circuit Current	V_{in} = 12.6 V, R_L = 0.1 Ω	1.54 A
Efficiency	V_{in} = 7.5 to 14.5 V, I_{out} = 120 mA	74%

Figure 13-18. Step-Up/Down Switching Regulator Design Example

$$t_{on(max)} + t_{off} = \frac{1}{f_{min}}$$
$$= \frac{1}{50 \times 10^3}$$
$$= 20\ \mu s \text{ per cycle}$$

3) Next calculate t_{on} and t_{off} from the ratio of t_{on}/t_{off} in #1 and the sum of $t_{on(max)} + t_{off}$ in #2.

$$t_{off} = \frac{t_{on(max)} + t_{off}}{\frac{t_{on}}{t_{off}} + 1}$$
$$= \frac{20 \times 10^{-6}}{1.9 + 1}$$
$$= 6.9\ \mu s$$
$$t_{on} = 20\ \mu s - 6.9\ \mu s$$
$$= 13.1\ \mu s$$

4) The maximum on-time is set by selecting a value for C_T.

$$C_T = 4 \times 10^{-5}\ t_{on(max)}$$
$$= 4 \times 10^{-5}\ (13.1 \times 10^{-6})$$
$$= 524 \text{ pF}$$

Use a standard 510 pF capacitor.

5) The peak switch current is:

$$I_{pk(switch)} = 2I_{out}\left(\frac{t_{on}}{t_{off}} + 1\right)$$
$$= 2\ (120 \times 10^{-3})\ (1.9 + 1)$$
$$= 696 \text{ mA}$$

6) A minimum value of inductance can now be calculated since the maximum on-time and peak switch current are known.

$$L_{min} = \left(\frac{V_{in(min)} - V_{satQ1} - V_{satQ2}}{I_{pk(switch)}}\right) t_{on}$$
$$= \left(\frac{7.5 - 0.8 - 0.8}{696 \times 10^{-3}}\right) 13.1 \times 10^{-6}$$
$$= 111\ \mu H$$

A 120 μH inductor was selected for $L_{(min)}$.

7) A value for the current limit resistor, R_{SC}, can be determined by using the current limit level of $I_{pk(switch)}$ when $V_{in} = 14.5$ V.

$$I'_{pk(switch)} = \left(\frac{V_{in} - V_{satQ1} - V_{satQ2}}{L_{(min)}}\right) t_{on(max)}$$
$$= \left(\frac{14.5 - 0.8 - 0.8}{120 \times 10^{-6}}\right) 13.1 \times 10^{-6}$$

$$= 1.41 \text{ A}$$

$$R_{SC} = \frac{0.33}{I'_{pk(switch)}}$$

$$= \frac{0.33}{1.41}$$

$$= 0.23\ \Omega$$

Use a standard 0.22 Ω resistor.

8) A minimum value for an *ideal* output filter capacitor is:

$$C_o \approx \left(\frac{I_{out}}{V_{ripple(p\text{-}p)}}\right) t_{on}$$

$$\approx \left(\frac{120 \times 10^{-3}}{100 \times 10^{-3}}\right) 13.1 \times 10^{-6}$$

$$\approx 15.7\ \mu F$$

Ideally this would satisfy the design goal, however, even a solid tantalum capacitor of this value will have a typical ESR (equivalent series resistance) of 0.3 Ω which will contribute an additional 209 mV of ripple. Also there is a ripple component due to the gain of the comparator equal to:

$$V_{ripple(p\text{-}p)} = \left(\frac{V_{out}}{V_{Ref}}\right) 1.5 \times 10^{-3}$$

$$= \left(\frac{10}{1.25}\right) 1.5 \times 10^{-3}$$

$$= 12 \text{ mV}$$

The ripple components are not in phase, but can be assumed to be for a conservative design. From the above it becomes apparent that ESR is the dominant factor in the selection of an output filter capacitor. a 330 μF with an ESR of 0.12 Ω was selected to satisfy this design example by the following:

$$ESR \approx \frac{V_{ripple(p\text{-}p)} - \left(\frac{I_{out}}{C_o}\right) t_{on} - \left(\frac{V_{out}}{V_{Ref}}\right) 1.5 \times 10^{-3}}{I_{pk(switch)}}$$

9) The nominal output voltage is programmed by the R1, R2 resistor divider.

$$R2 = R1 \left(\frac{V_{out}}{V_{Ref}} - 1\right)$$

$$= R1 \left(\frac{10}{1.25} - 1\right)$$

$$= 7\ R1$$

If 1.3 k is chosen for R1, then R2 would be 9.1 k, both being standard resistor values.

10) Transistor Q1 is driven into saturation with a forced gain of approximately 20 at an input voltage of 7.5 V. The required base drive is:

$$I_B = \frac{I_{pk(switch)}}{B_F}$$
$$= \frac{696 \times 10^{-3}}{20}$$
$$= 35 \text{ mA}$$

The value for the base-emitter turn-off resistor R_{BE} is determined by:

$$R_{BE} = \frac{10 B_F}{I_{pk(switch)}}$$
$$= \frac{10 (20)}{696 \times 10^{-3}}$$
$$= 287 \ \Omega$$

A standard 300 Ω resistor was selected.

The additional base current required due to R_{BE} is:

$$I_{R_{BE}} = \frac{V_{BEQ1}}{R_{BE}}$$
$$= \frac{0.8}{300}$$
$$= 3 \text{ mA}$$

The base drive resistor for Q1 is equal to:

$$R_B = \frac{V_{in(min)} - V_{sat(driver)} - V_{RSC} - V_{BEQ1}}{I_B + I_{R_{BE}}}$$
$$= \frac{7.5 - 0.8 - 0.15 - 0.8}{(35 + 3) \times 10^{-3}}$$
$$= 151 \ \Omega$$

A standard 150 Ω resistor was used.

The circuit performance data shows excellent line and load regulation. There is some loss in conversion efficiency over the basic step-up or step-down circuits due to the added switch transistor and diode 'on' losses. However this unique converter demonstrates that with a simple inductor, a step-up/down converter with current limiting can be constructed.

Design Considerations

As previously stated, the design equations for L_{min} were based upon the assumption that the switching regulator is operating on the onset of continuous conduction with a fixed input voltage, maximum output load current, and a minimum charge-current oscillator. Typically the oscillator charge-current will be greater than the specific minimum of 20 microamps, thus t_{on} will be somewhat shorter and the actual LC operating frequency will be greater than predicted.

Also note that the voltage drop developed across the current-limit resistor R_{sc} was not accounted for in the t_{on}/t_{off} and $L_{(min)}$ design formulas. This voltage drop must be considered when designing high current converters that operate with an input voltage of less than 5.0 volts.

When checking the initial switcher operation with an oscilloscope, there will

be some concern of circuit instability due to the apparent random switching of the output. The oscilloscope will be difficult to synchronize. This is **not** a problem. It is a normal operating characteristic of this type of switching regulator and is caused by the asynchronous operation of the comparator to that of the oscillator. The oscilloscope may be synchronized by varying the input voltage or load current slightly from the design nominals.

High frequency circuit layout techniques are imperative with switching regulators. To minimize EMI, all high current loops should be kept as short as possible using heavy copper runs. The low current signal and high current switch and output grounds should return on separate paths back to the input filter capacitor. The R1, R2 output voltage divider should be located as close to the IC as possible to eliminate any noise pick-up into the feedback loop. The circuit diagrams were purposely drawn in a manner to depict this.

All circuits used molypermalloy power toroid cores for the magnetics where only the inductance value is given. The number of turns, wire and core size information is not given since no attempt was made to optimize their design. Inductor and transformer design information may be obtained from the magnetic core and assembly companies listed on the switching regulator component source table.

In some circuit designs, mainly step-up and voltage-inverting, a ratio of $t_{on}/(t_{on} + t_{off})$ greater than 0.857 may be required. This can be obtained by the addition of the ratio extender circuit shown in Figure 13-19. This circuit uses germanium components and is temperature sensitive. A negative temperature coefficient timing capacitor will help reduce this sensitivity. Figure 13-20 shows the output switch on and off time versus C_T with and without the ratio extender

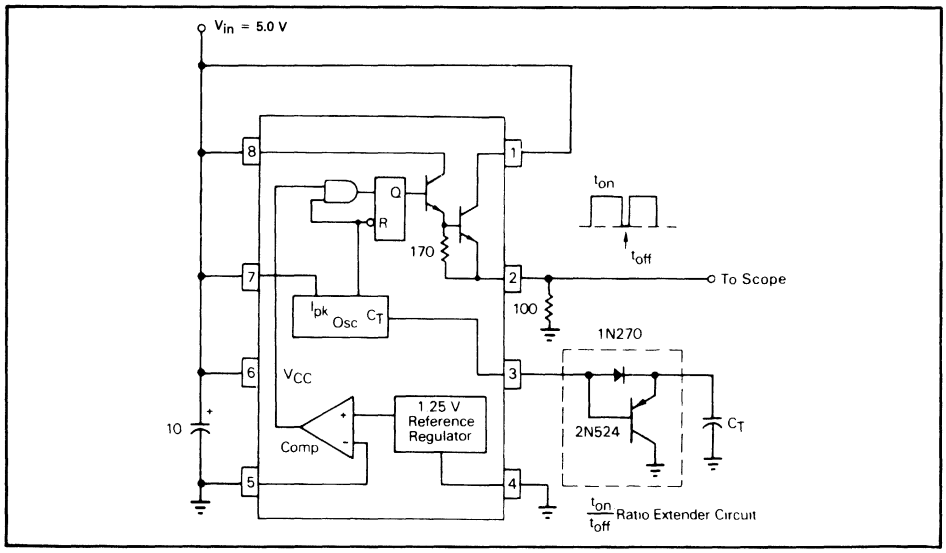


Figure 13-19. Output Switch On-Off Time Test Circuit

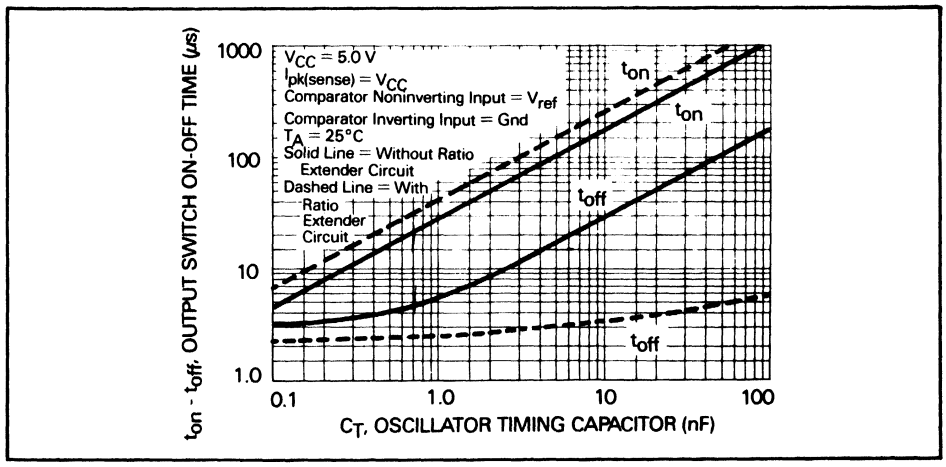


Figure 13-20. Output Switch On-Off Time versus Oscillator Timing Capacitor

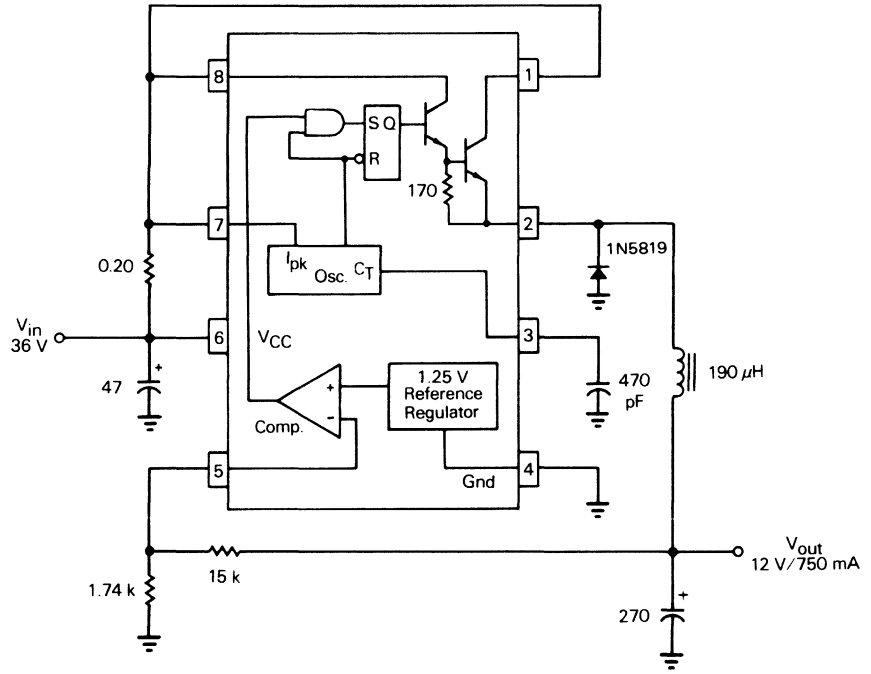
circuit. Notice that without the circuit, the ratio of $t_{on}/(t_{on} + t_{off})$ is limited to 0.857 only for values of C_T greater than 2.0 nF. With the circuit, the ratio is variable depending upon the value chosen for C_T since t_{off} is now nearly a constant. Current limiting must be used on all step-up and voltage-inverting designs using the ratio extender circuit. This will allow the inductor time to reset between cycles of overcurrent during initial power-up of the switcher. When the output filter capacitor reaches its nominal voltage, the voltage feedback loop will control regulation.

Applications Section

Listed below is an index of all the converter circuits shown in this application note. They are categorized into three major groups based upon the main output configuration. Each of these circuits was constructed and tested, and a performance table is included.

Index of Converter Circuits

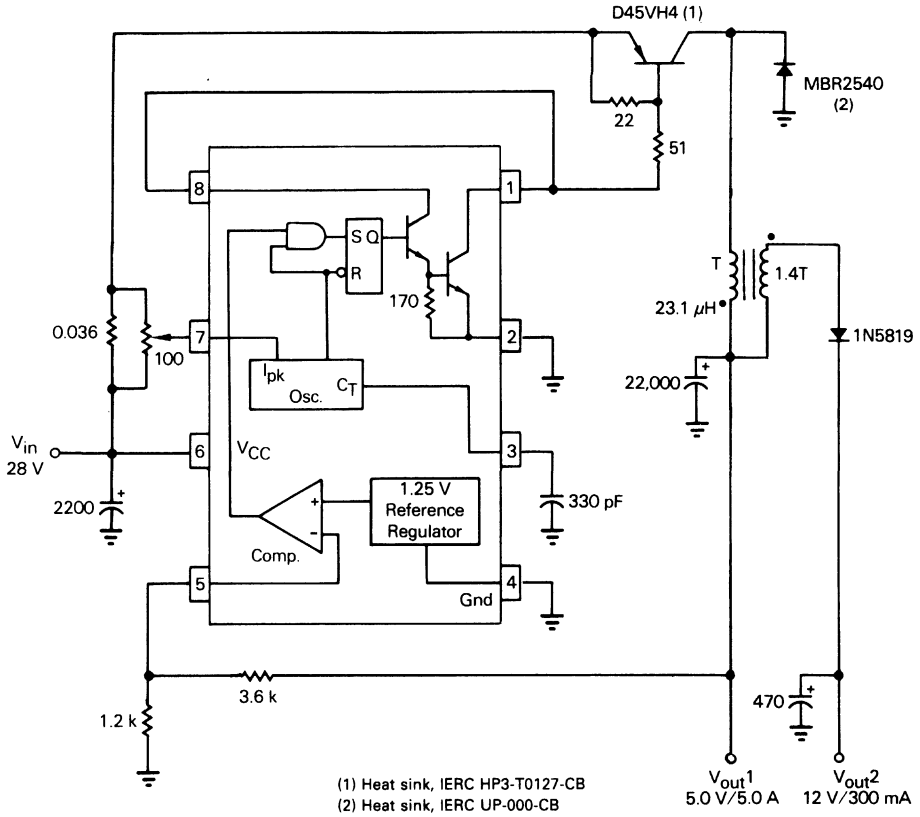
MAIN OUTPUT CONFIGURATION		INPUT V	OUTPUT 1 V/mA	OUTPUT 2 V/mA	OUTPUT 3 V/mA	FIGURE NO.
Step-Down						
μA78S40	Low Power with Minimum Components	24	5/50	—	—	13-9
MC34063	Medium Power	36	12/750	—	—	13-21
MC34063	Buffered Switch and Second Output	28	5/5000	12/300	—	13-22
μA78S40	Linear Pass from Main Output	33	24/500	15/50	—	13-23
μA78S40	Buffered Switch and Buffered Linear Pass from Main Output	28	15/3000	12/1000	—	13-24
μA78S40	Negative Input and Negative Output	−28	−12/500	—	—	13-25
Step-Up						
μA78S40	Low Power with Minimum Components	9.0	28/50	—	—	13-11
MC34063	Medium Power	12	36/225	—	—	13-26
MC34063	High Voltage, Low Power	4.5	190/5.0	—	—	13-27
μA78S40	High Voltage, Medium Power Photoflash	4.5	334/45	—	—	13-28
μA78S40	Linear Pass from Main Output	2.5	9/100	6/30	—	13-29
μA78S40	Buffered Linear Pass from Main Output EE PROM Programmer	4.5	See Circuit	—	—	13-30
μA78S40	Buffered Switch and Buffered Linear Pass from Main Output	4.5	15/1000	12/500	−12/50	13-31
μA78S40	Dual Switcher, Step-Up and Step Down with Buffered Switch	12	28/250	5/250	—	13-32
Step-Up/Down						
MC34063	Medium Power Step-Up/Down	7.5 to 14.5	10/120	—	—	13-18
Voltage-Inverting						
MC34063	Low Power	5	−12/100	—	—	13-33
μA78S40	Medium Power with Buffered Switch	15	−15/500	—	—	13-15
μA78S40	High Voltage, High Power with Buffered Switch	28	−120/850	—	—	13-34
μA78S40	42 Watt Off-Line Flyback Switcher	115 Vac	5/4000	12/700	−12/700	13-35
μA78S40	Tracking Regulator with Buffered Switch and Buffered Linear Pass from Input	15	−12/500	12/500	—	13-37



Test	Conditions	Results
Line Regulation	V_{in} = 20 to 40 V, I_{out} = 750 mA	Δ = 15 mV or ± 0.063%
Load Regulation	V_{in} = 36 V, I_{out} = 100 to 750 mA	Δ = 40 mV or ± 0.17%
Output Ripple	V_{in} = 36 V, I_{out} = 750 mA	60 mV_{p-p}
Short Circuit Current	V_{in} = 36 V, R_L = 0.1 Ω	1.6 A
Efficiency	V_{in} = 36 V, I_{out} = 750 mA	89.5%

A maximum power transfer of 9.0 watts is possible from an 8 pin dual in-line package with V_{in} = 36 V and V_{out} = 12 V.

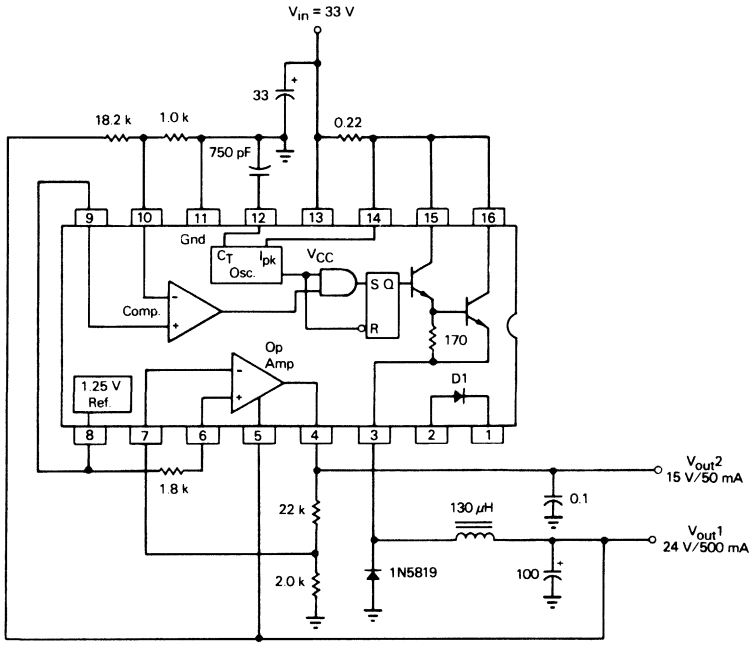
Figure 13-21. Step-Down



Test		Conditions	Results
Line Regulation	$V_{out}1$	V_{in} = 20 to 30 V, $I_{out}1$ = 5.0 A, $I_{out}2$ = 300 mA	Δ = 9.0 mV or ± 0.09%
Load Regulation	$V_{out}1$	V_{in} = 28 V, $I_{out}1$ = 1 to 5.0 A, $I_{out}2$ = 300 mA	Δ = 20 mV or ± 0.2%
Output Ripple	$V_{out}1$	V_{in} = 28 V, $I_{out}1$ = 5.0 A, $I_{out}2$ = 300 mA	60 mV_{p-p}
Short Circuit Current	$V_{out}1$	V_{in} = 28 V, R_L = 0.1 Ω	11.4 A
Line Regulation	$V_{out}2$	V_{in} = 20 to 30 V, $I_{out}1$ = 5.0 A, $I_{out}2$ = 300 mA	Δ = 72 mV or ± 0.3%
Load Regulation	$V_{out}2$	V_{in} = 20 V, $I_{out}2$ = 100 to 300 mA, $I_{out}1$ = 5.0 A	Δ = 12 mV or ± 0.05%
Output Ripple	$V_{out}2$	V_{in} = 28 V, $I_{out}1$ = 5.0 A, $I_{out}2$ = 300 mA	25 mV p-p
Short Circuit Current	$V_{out}2$	V_{in} = 28 V, R_L = 0.1 Ω	11.25A
Efficiency		V_{in} = 28 V, $I_{out}1$ = 5.0 A, $I_{out}2$ = 300 mA	80%

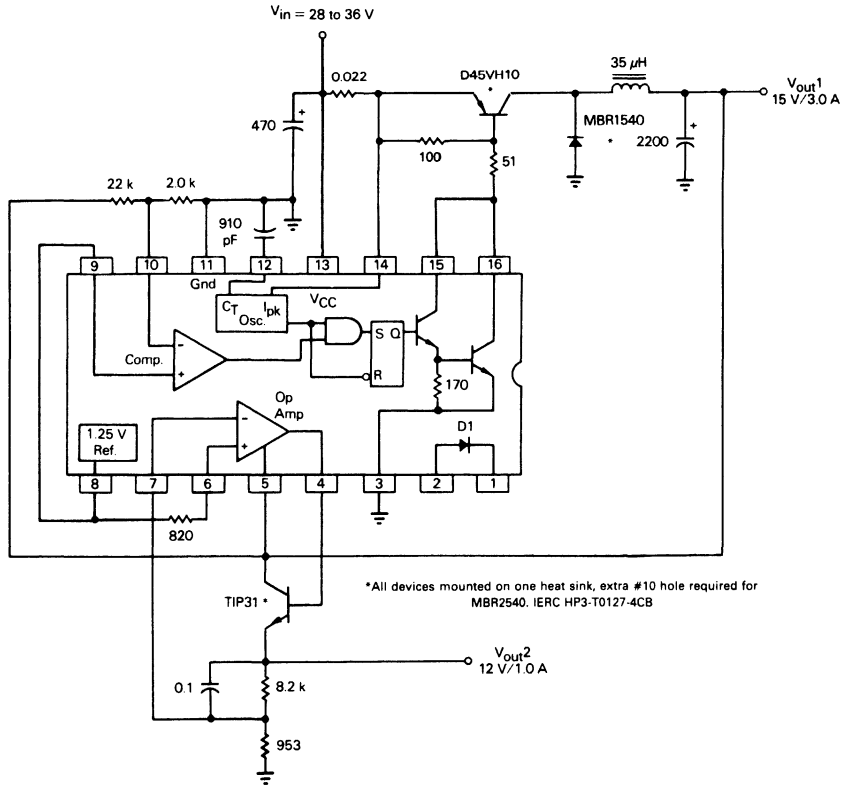
A second output can be easily derived by winding a secondary on the main output inductor and phasing it so that energy is delivered to $V_{out}2$ during t_{off}. The second output power should not exceed 25% of the main output. The 100 Ω potentiometer is used to divide down the voltage across the 0.036 Ω resistor and thus fine tune the current limit.

Figure 13-22. Step-Down with Buffered Switch and Second Output



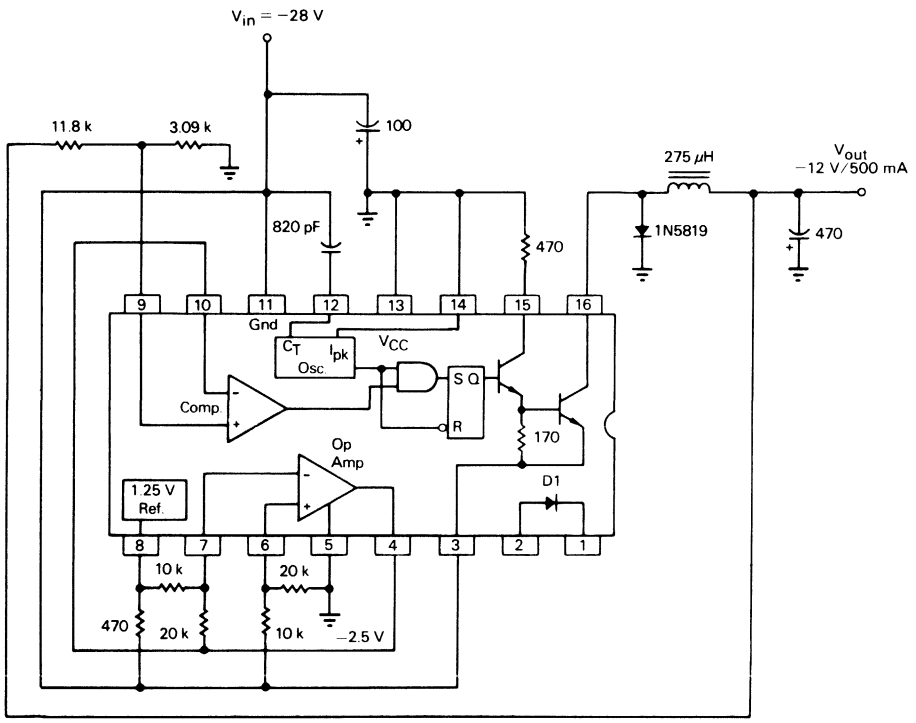
Test		Conditions	Results
Line Regulation	$V_{out}1$	V_{in} = 30 to 36 V, $I_{out}1$ = 500 mA, $I_{out}2$ = 50 mA	Δ = 30 mV or ± 0.63%
Load Regulation	$V_{out}1$	V_{in} = 33 V, $I_{out}1$ = 100 to 500 mA, $I_{out}2$ = 50 mA	Δ = 70 mV or ± 0.15%
Output Ripple	$V_{out}1$	V_{in} = 33 V, $I_{out}1$ = 500 mA, $I_{out}2$ = 50 mA	80 mV_{p-p}
Short Circuit Current	$V_{out}1$	V_{in} = 33 V, R_L = 0.1 Ω	2.5 A
Line Regulation	$V_{out}2$	V_{in} = 30 to 36 V, $I_{out}1$ = 500 mA, $I_{out}2$ = 50 mA	Δ = 20 mV or = 0.067%
Load Regulation	$V_{out}2$	V_{in} = 33 V, $I_{out}2$ = 0 to 50 mA, $I_{out}1$ = 500 A	Δ = 60 mV or ± 0.2%
Output Ripple	$V_{out}2$	V_{in} = 33 V, $I_{out}1$ = 500 mA, $I_{out}2$ = 50 mA	70 mV p-p
Short Circuit Current	$V_{out}2$	V_{in} = 33 V, R_L = 0.1 Ω	90 mA
Efficiency		V_{in} = 33 V, $I_{out}1$ = 500 mA, $I_{out}2$ = 50 mA	88.2%

Figure 13-23. Step-Down with Linear Pass from Main Output



Test		Conditions	Results
Line Regulation	$V_{out}1$	V_{in} = 28 to 36 V, $I_{out}1$ = 3.0 A, $I_{out}2$ = 1.0 A	Δ = 13 mV or ± 0.043%
Load Regulation	$V_{out}1$	V_{in} = 36 V, $I_{out}1$ = 1 to 4.0 A, $I_{out}2$ = 1.0 A	Δ = 21 mV or ± 0.07%
Output Ripple	$V_{out}1$	V_{in} = 36 V, $I_{out}1$ = 3.0 A, $I_{out}2$ = 1.0 A	120 mV_{p-p}
Short Circuit Current	$V_{out}1$	V_{in} = 36 V, R_L = 0.1 Ω	12.6 A
Line Regulation	$V_{out}2$	V_{in} = 28 to 36 V, $I_{out}1$ = 3.0 A, $I_{out}2$ = 1.0 A	Δ = 2.0 mV or ± 0.008%
Load Regulation	$V_{out}2$	V_{in} = 36 V, $I_{out}2$ = 0 to 1.5 A	Δ = 2.0 mV or ± 0.008%
Output Ripple	$V_{out}2$	V_{in} = 36 V, $I_{out}1$ = 3.0 A, $I_{out}2$ = 1.0 A	25 mV p-p
Short Circuit Current	$V_{out}2$	V_{in} = 36 V, R_L = 0.1 Ω	3.6 A
Efficiency		V_{in} = 36 V, $I_{out}1$ = 3.0 A, $I_{out}2$ = 1.0 A	78.5%

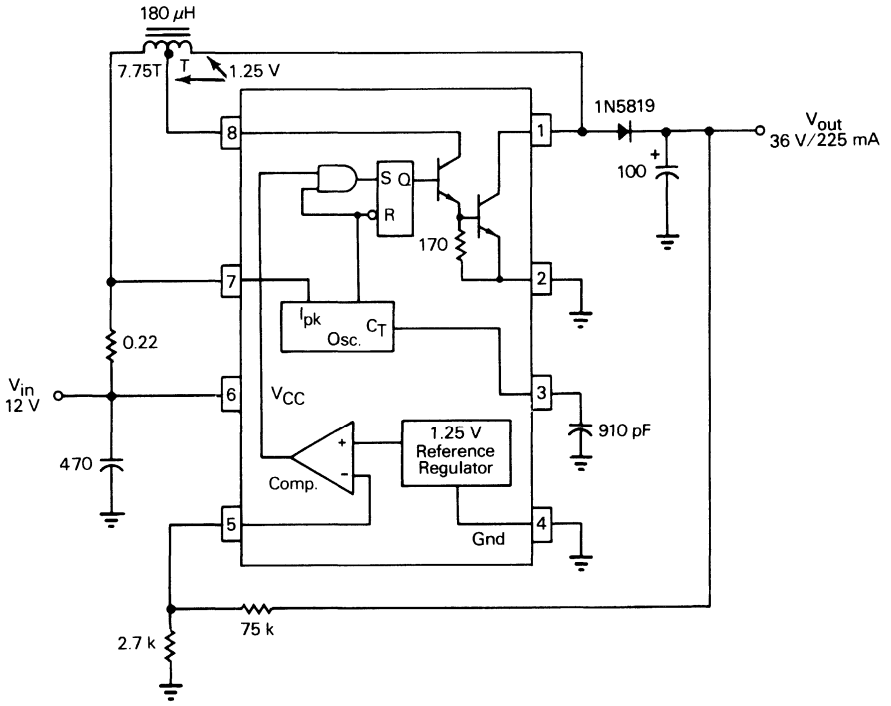
Figure 13-24. Step-Down with Buffered Switch and Buffered Linear Pass from Main Output



Test	Conditions	Results
Line Regulation	V_{in} = −22 to −28 V, I_{out} = 500 mA	Δ 25 mV or ± 0.104%
Load Regulation	V_{in} = −28 V, I_{out} = 100 to 500 mA	Δ = 10 mV or ± 0.042%
Output Ripple	V_{in} = −28 V, I_{out} = 500 mA	130 mV_{p-p}
Efficiency	V_{in} = −28 V, I_{out} = 500 mA	85.5%

In this step-down circuit, the output switch must be connected in series with the negative input, causing the internal 1.25 V reference to be with respect to $-V_{in}$. A second reference of −2.5 V with respect to ground is generated by the Op Amp. Note that the 10 k and 20 k resistors must be matched pairs for good line regulation and that no provision is made for output short-circuit protection.

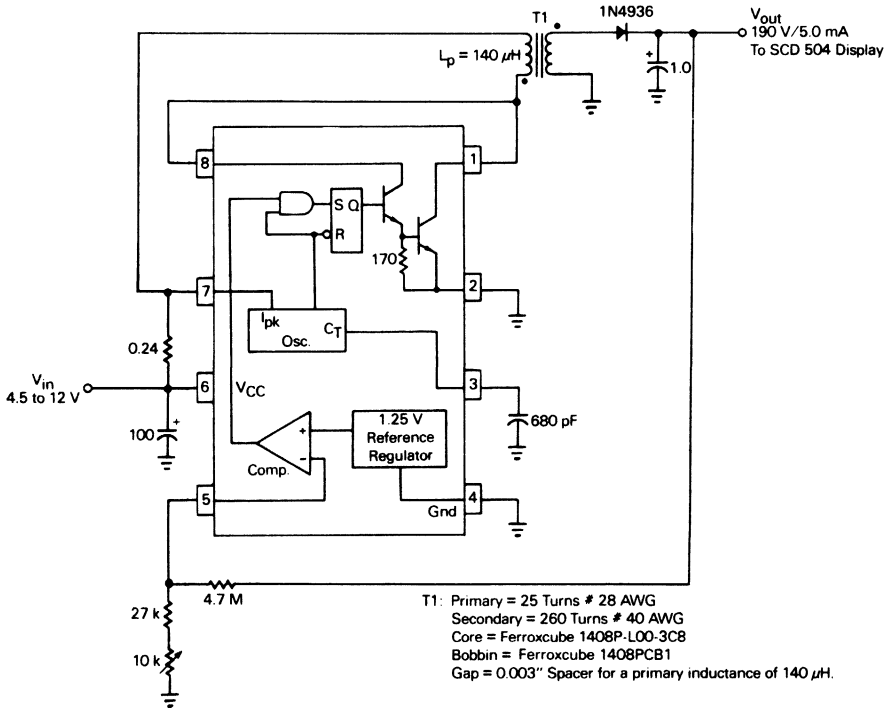
Figure 13-25. Step-Down with Negative Input and Negative Output



Test	Conditions	Results
Line Regulation	V_{in} = 11 to 15 V, I_{out} = 225 mA	Δ = 20 mV or ± 0.028%
Load Regulation	V_{in} = 12 V, I_{out} = 50 to 225 mA	Δ = 30 mV or ± 0.042%
Output Ripple	V_{in} = 12 V, I_{out} = 225 mA	100 mV_{p-p}
Efficiency	V_{in} = 12 V, I_{out} = 225 mA	90.4%

A maximum power transfer of 8.1 watts is possible with V_{in} = 12 V and V_{out} = 36 V. The high efficiency is partially due to the use of the tapped inductor. The tap point is set for a voltage differential of 1.25 V. The range of V_{in} is somewhat limited when using this method.

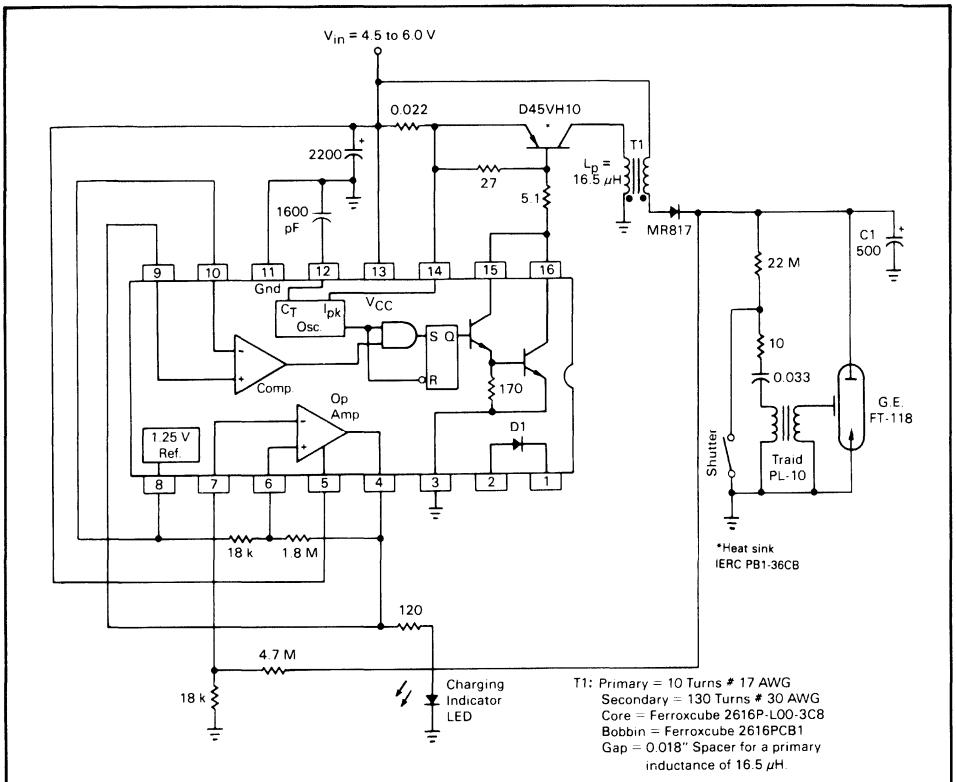
Figure 13-26. Step-Up



Test	Conditions	Results
Line Regulation	V_{in} = 4.5 to 12 V, I_{out} = 5.0 mA	Δ = 2.3 V or ± 0.61%
Load Regulation	V_{in} = 5.0 V, I_{out} = 1.0 to 6.0 mA	Δ = 1.4 V or ± 0.37%
Output Ripple	V_{in} = 5.0 V, I_{out} = 5.0 mA	250 mV_{p-p}
Short Circuit Current	V_{in} = 5.0, V, R_L = 0.1 Ω	113 mA
Efficiency	V_{in} = 5.0 V, I_{out} = 5.0 mA	68%

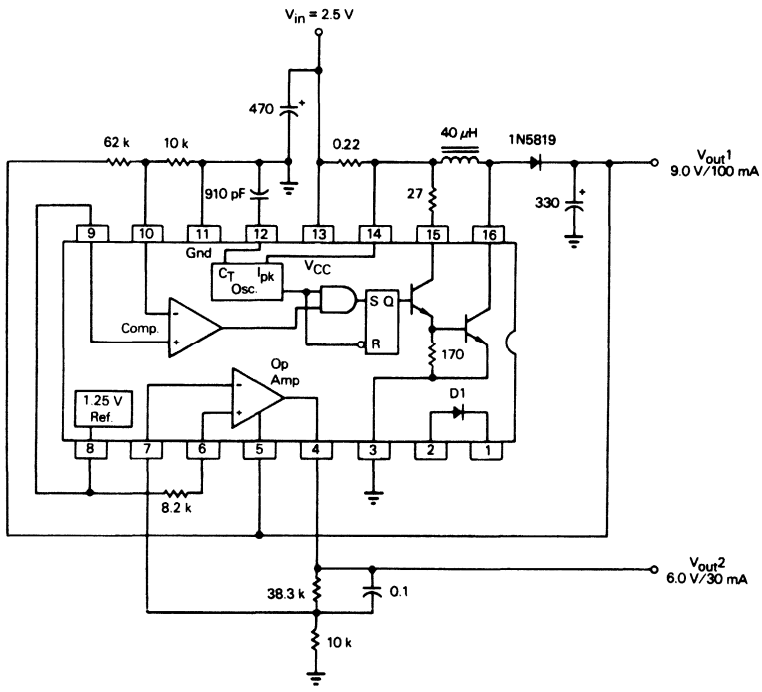
This circuit was designed to power the Motorola Solid Ceramic Displays from a V_{in} of 4.5 to 12 V. The design calculations are based on a step-up converter with an input of 4.5 V and a 24 V output rated at 45 mA. The 24 V level is the maximum step-up allowed by the oscillator ratio of $t_{on}/(t_{on} + t_{off})$. The 45 mA current level was chosen so that the transformer primary power level is about 10% greater than that required by the load. The maximum V_{in} of 12 V is determined by the sum of the flyback and leakage inductance voltages present at the collector of the output switch during turn-off must not exceed 40 V.

Figure 13-27. High-Voltage, Low Power Step-Up for Solid Ceramic Display



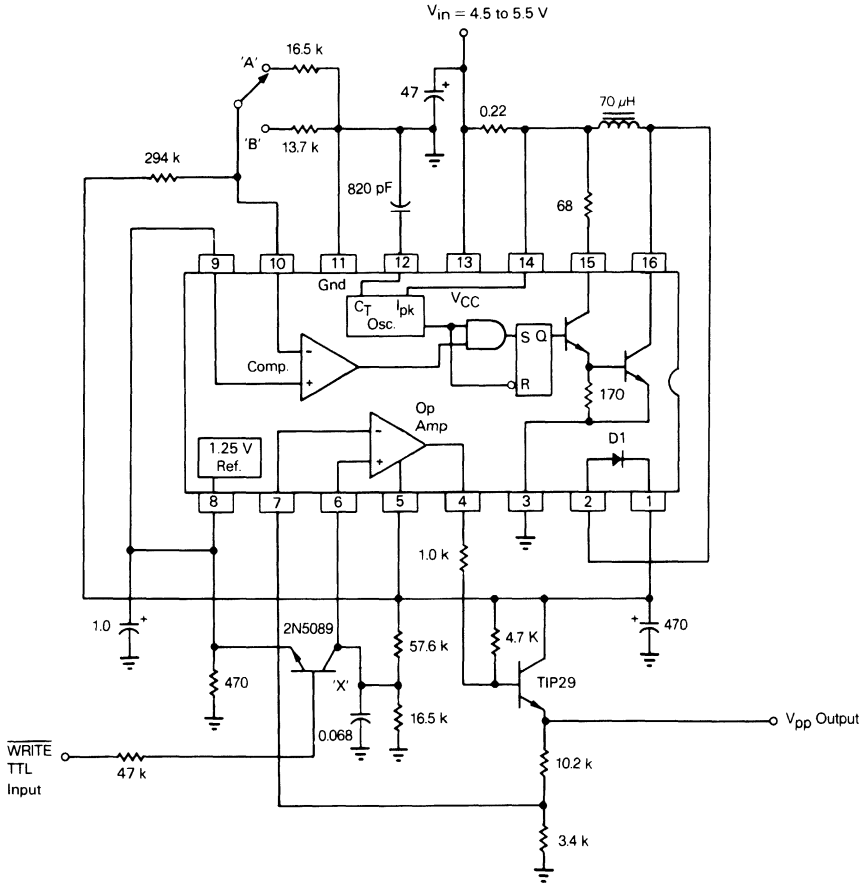
With V_{in} of 6.0 V, this step-up converter will charge capacitor C1 from 0 to 334 V in 4.7 seconds. The switching operation will cease until C1 bleeds down to 323 V. The charging time between flashes is 4.0 seconds. The output current at 334 V is 45 mA.

Figure 13-28. High-Voltage Step-Up with Buffered Switch for Photoflash Applications



Test		Conditions	Results
Line Regulation	$V_{out}1$	V_{in} = 2.5 to 3.5 V, $I_{out}1$ = 100 mA $I_{out}2$ = 30 mA	Δ = 20 mV or ± 0.11%
Load Regulation	$V_{out}1$	V_{in} = 2.5 V, $I_{out}1$ = 25 to 100 mA, $I_{out}2$ = 30 mA	Δ = 20 mV or ± 0.11%
Output Ripple	$V_{out}1$	V_{in} = 2.5 V, $I_{out}1$ = 100 mA, $I_{out}2$ = 30 mA	60 mV_{p-p}
Line Regulation	$V_{out}2$	V_{in} = 2.5 to 3.5 V, $I_{out}1$ = 100 mA, $I_{out}2$ = 30 mA	Δ = 1.0 mV or ± 0.0083%
Load Regulation	$V_{out}2$	V_{in} = 2.5 V, $I_{out}2$ = 0 to 50 mA, $I_{out}1$ = 100 mA	Δ = 1.0 mV or ± 0.0083%
Output Ripple	$V_{out}2$	V_{in} = 2.5 V, $1_{out}1$ = 100 mA, $I_{out}2$ = 30 mA	5.0 mV p-p
Short Circuit Current	$V_{out}2$	V_{in} = 2.5 V, R_L = 0.1 Ω	150 mA
Efficiency		V_{in} = 3.0 V, $I_{out}1$ = 100 mA, $I_{out}2$ = 30 mA	68.3%

Figure 13-29. Step-Up with Linear Pass from Main Output



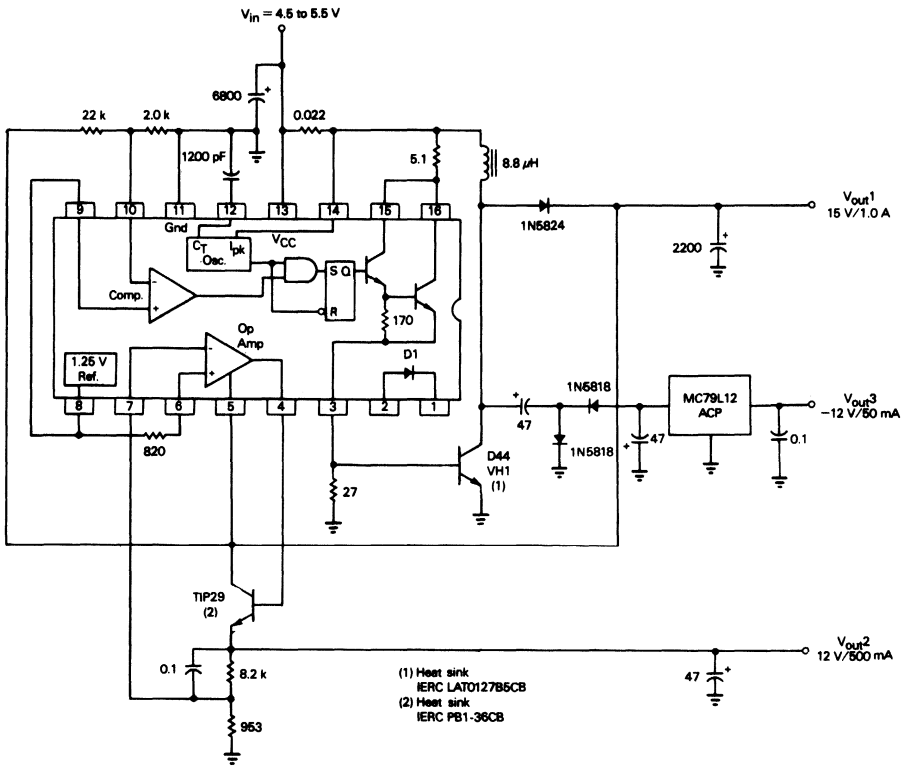
Switch Position	WRITE	Voltage @ Pins 1 & 5	Voltage @ X	Voltage @ V_{pp}
A	< 1.5	23.52	5.24	20.95
A	> 2.25	23.52	1.28	5.12
B	< 1.5	28.07	6.25	25.01
B	> 2.25	28.07	1.28	5.12

All values are in volts. V_{ref} = 1.245 V.

Contributed by Steve Hageman of Calex Mgf. Co. Inc.

Used in conjunction with two transistors, the μA78S40 can generate the required V_{pp} voltage of 21 or 25 volts needed to program and erase EEPROMs from a single 5 volt supply. A step-up converter provides a selectable regulated voltage at Pins 1 and 5. This voltage is used to generate a second reference at point 'X' and to power the linear regulator consisting of the internal op amp and a TIP29 transistor. When the WRITE input is less than 1.5 V, the 2N5089 transistor is OFF, allowing the voltage at 'X' to rise exponentially with an approximate time constant of 600 μs as required by some EEPROMs. The linear regulator amplifies the voltage at 'X' by four, generating the required V_{pp} output voltage for the byte-erase write cycle. When the WRITE input is greater than 2.25 V, the 2N5089 turns ON clamping point 'X' to the internal reference level of 1.245 volts. The V_{pp} output will not be at approximately 5.1 volts or 4 (1.245 + V_{sat} 2N5089). The μA78S40 reference can only source current, therefore a reference pre bias of 470 Ω is used. The V_{pp} output is short-circuit protected and can supply a current of 100 mA at 21 V or 75 mA at 25 V over an input range of 4.5 to 5.5 V.

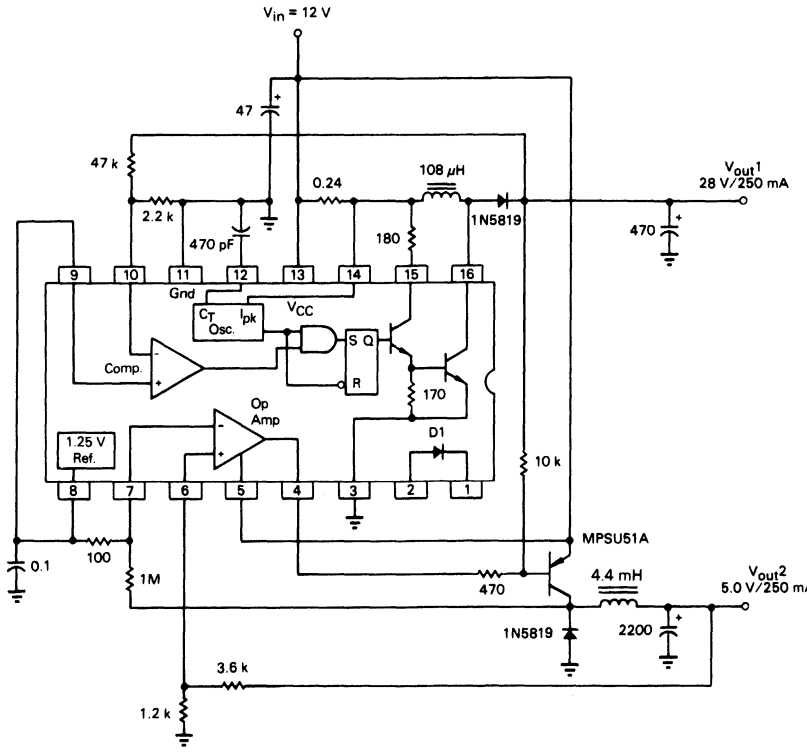
Figure 13-30. Step-Up with Buffered Linear Pass from Main Output for Programming EEPROMs



Test		Conditions	Results
Line Regulation	$V_{out}1$	V_{in} = 4.5 to 5.5 V	Δ = 18 mV or ± 0.06%
Load Regulation	$V_{out}1$	V_{in} = 5.0 V, $I_{out}1$ = 0.25 to 1.0 A	Δ = 25 mV or ±0.083%
Output Ripple	$V_{out}1$	V_{in} = 5.0 V	75 mV_{p-p}
Line Regulation	$V_{out}2$	V_{in} = 4.5 to 5.5 V	Δ = 3.0 mV or ± 0.013%
Load Regulation	$V_{out}2$	V_{in} = 5.0 V, $I_{out}2$ = 100 to 500 mA	Δ = 5.0 mV or ± 0.021%
Output Ripple	$V_{out}2$	V_{in} = 5.0 V	20 mV_{p-p}
Short Circuit Current	$V_{out}2$	V_{in} = 5.0 V, R_L = 0.1 Ω	2.7 A
Line Regulation	$V_{out}3$	V_{in} = 4.5 to 5.5 V	Δ = 2.0 mV or ± 0.008%
Load Regulation	$V_{out}3$	V_{in} = 5.0 V, $I_{out}3$ = 0.0 to 50 mA	Δ = 29 mV or ± 0.12%
Output Ripple	$V_{out}3$	V_{in} = 5.0 V	15 mV_{p-p}
Short Circuit Current	$V_{out}3$	V_{in} = 5.0 V, R_L = 0.1 Ω	130 mA
Efficiency		V_{in} = 5.0 V	71.8%

All outputs are at nominal load current unless otherwise noted.

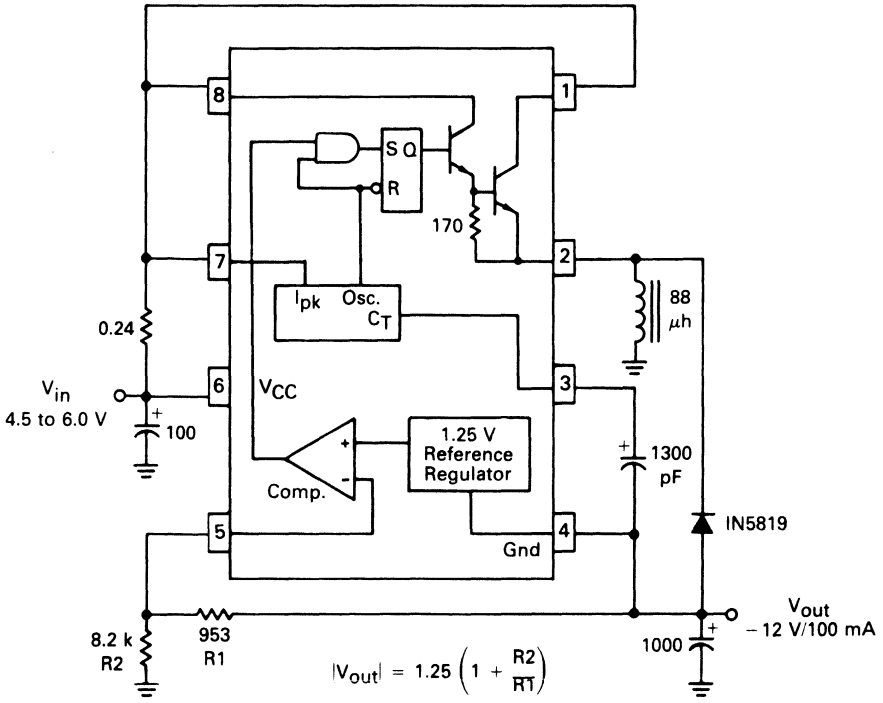
Figure 13-31. Step-Up with Buffered Switch and Buffered Linear Pass from Main Output



Test		Conditions	Results
Line Regulation	$V_{out}1$	V_{in} = 9.0 to 15 V, $I_{out}1$ = 250 mA, $I_{out}2$ = 250 mA	Δ = 30 mV or ± 0.054%
Load Regulation	$V_{out}1$	V_{in} = 12 V, $I_{out}1$ = 100 to 300 mA, $I_{out}2$ = 250 mA	Δ = 20 mV or ± 0.036%
Output Ripple	$V_{out}1$	V_{in} = 12 V, $I_{out}1$ = 250 mA, $I_{out}2$ = 250 mA	35 mV_{p-p}
Short Circuit Current	$V_{out}1$	V_{in} = 12 V, R_L = 0.1 Ω	1.7 A
Line Regulation	$V_{out}2$	V_{in} = 9.0 to 15 V, $I_{out}1$ = 250 mA, $I_{out}2$ = 250mA	Δ = 4.0 mV or ± 0.04%
Load Regulation	$V_{out}2$	V_{in} = 12 V, $I_{out}2$ = 100 to 300 mA, $I_{out}1$ = 250 mA	Δ = 18 mV or ± 0.18%
Output Ripple	$V_{out}2$	V_{in} = 12 V, $I_{out}1$ = 250 mA, $I_{out}2$ = 250 mA	70 mV p-p
Efficiency		V_{in} = 12 V, $I_{out}1$ = 250 mA, $I_{out}2$ = 250 mA	81.8%

This circuit shows a method of using the μA78S40 to construct two independent converters. Output 1 uses the typical step-up circuit configuration while Output 2 makes the use of the op amp connected with positive feedback to create a free running step-down converter. The op amp slew rate limits the maximum switching frequency at rated load to less than 2.0 kHz.

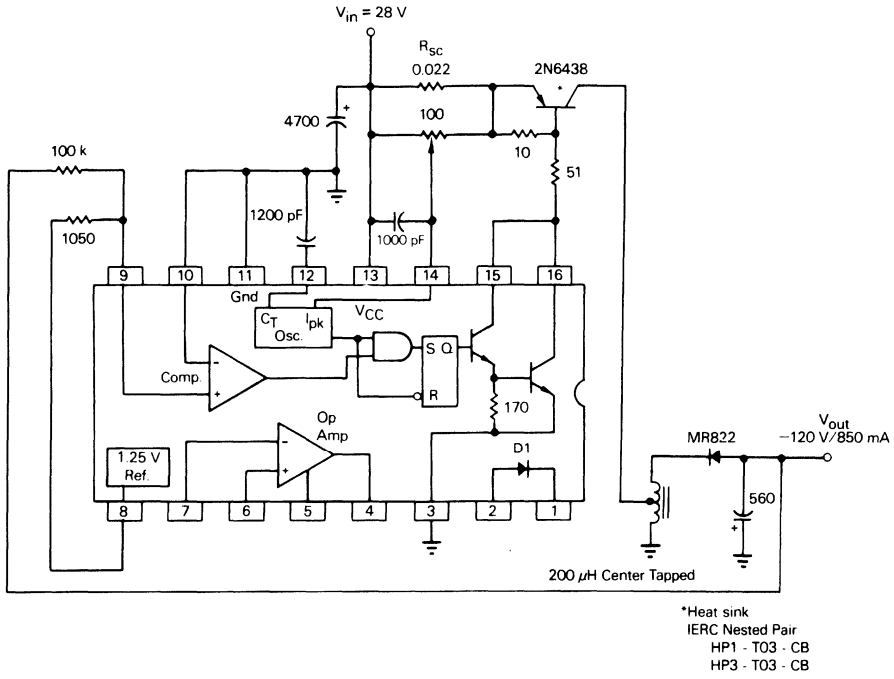
Figure 13-32. Dual Switcher, Step-Up and Step-Down with Buffered Switch



Test	Conditions	Results
Line Regulation	V_{in} = 4.5 to 6.0 V, I_{out} = 100 mA	Δ = 2.0 mV or ±0.008%
Load Regulation	V_{in} = 5.0 V, I_{out} = 10 to 100 mA	Δ = 10 mV or ±0.042%
Output Ripple	V_{in} = 5.0 V, I_{out} = 100 mA	35 mV_{p-p}
Short Circuit Current	V_{in} = 5.0 V, RL = 0.1Ω	1.4 A
Efficiency	V_{in} = 5.0 V, I_{out} = 100 mA	60%

The above circuit shows a method of using the MC34063 to construct a low power voltage-inverting converter. Note that the integrated circuit ground, pin 4, is connected directly to the negative output, thus allowing the internally connected comparator and reference to function properly for output voltage control. With this configuration, the sum of V_{in} + V_{out} + V_F must not exceed 40 V. The conversion efficiency is modest since the output switch is connected as a Darlington and its on-voltage is a large portion of the minimum operating input voltage. A 12% improvement can be realized with the addition of an external PNP saturated switch when connected in a similar manner to that shown in Figure 13-15.

Figure 13-33. Low Power Voltage-Inverting



Test	Conditions	Results
Line Regulation	V_{in} = 24 to 28 V, I_{out} = 850 mA	Δ = 100 mV or ± 0.042%
Load Regulation	V_{in} = 28 V, I_{out} = 100 to 850 mA	Δ = 70 mV or ± 0.029%
Output Ripple	V_{in} = 28 V, I_{out} = 850 mA	450 mV p-p
Short Circuit Current	V_{in} = 28 V, R_L = 0.1 Ω	6.4 A
Efficiency	V_{in} = 28 V, I_{out} = 850 mA	81.8%

This high power voltage-inverting circuit makes use of a center tapped inductor to step-up the magnitude of the output. Without the tap, the output switch transistor would need a V_{CE} breakdown greater than 148 V at the start of t_{off}; the maximum rating of this device is 120 V. All calculations are done for the typical voltage-inverting converter with an input of 28 V and an output of −120 V. The inductor value will be 50 μH or 200 μH center tapped for the value of C_T used. The 1000 pF capacitor is used to filter the spikes generated by the high switching current flowing through the wiring and R_{sc} inductance.

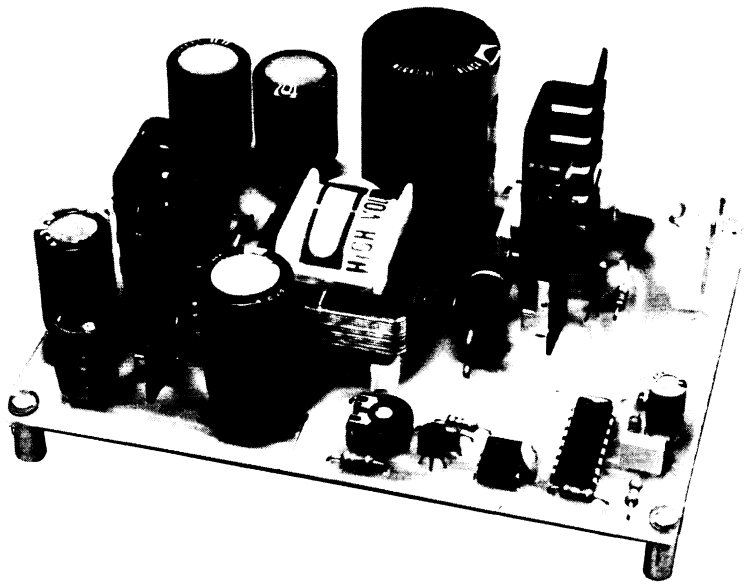
Figure 13-34. High Power Voltage-Inverting with Buffered Switch

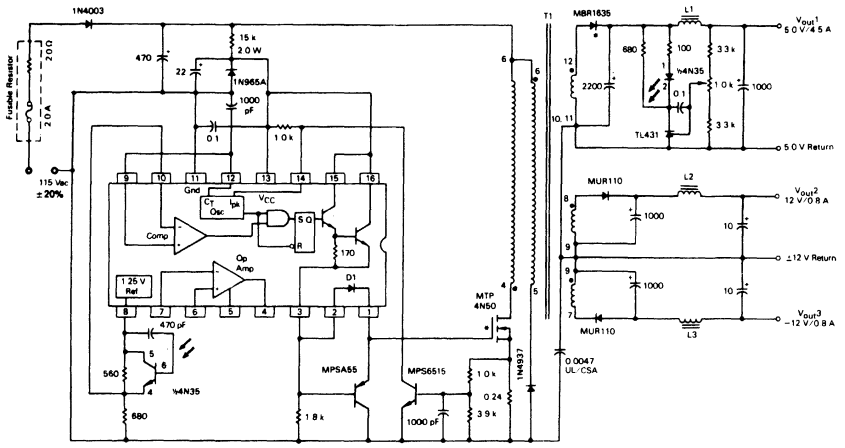
An economical 42 watt off-line flyback switcher is shown in Figure 13-35. In this circuit the μA78S40 is connected to operate as a fixed frequency pulse width modulator. The oscillator sawtooth waveform is connected to the noninverting input of the comparator and a preset voltage of 685 mV, derived from the reference is connected to the inverting input. The preset voltage reduces the maximum percent on-time of the output switch from a nominal of 85.7% to about 45%. The maximum must be less than 50% when an equal turns ratio of primary to clamp winding is used. Output regulation and isolation is achieved by the use of the TL431 as an output reference and comparator, and a 4N35 optocoupler. As the 5.0 V output reaches its nominal level, the TL431 will start to conduct current through the LED in the 4N35. This in turn will cause the optoreceiver transistor to turn-on, raising the voltage at Pin 10 which will cause a reduction in percent on-time of the output switch.

The peak drain current at 42 W output is 2.0 A. As the output loading is increased, the MPS6515 will activate the $I_{pk(sense)}$ pin and shorten t_{on} on a cycle by cycle basis. If an output is shorted the $I_{pk(sense)}$ circuit will cause C_T to charge beyond the upper oscillator trip point and the oscillator frequency will decrease. This action will result in a lower average power dissipation for the output switching transistor.

Each output has a series inductor and a second shunt filter capacitor forming a Pi filter. This is used to reduce the level of high frequency ripple and spikes. Care must be taken with the layout of grounds in the Pi filter network. Each input and output filter capacitor must have separate ground returns to the transformer as shown on the circuit diagram. A complete printed circuit board with component layout is shown in Figure 13-36.

The μA78S40 may be used in any of the previously shown circuit designs as a fixed frequency pulse width modulator, however consideration must be given to the proper selection of the feedback loop elements in order to insure circuit stability.





Test		Conditions	Results
Line Regulation	$V_{out}1$	V_{in} = 92 to 138 Vac	Δ = 1.0 mV or ± 0.01%
Load Regulation	$V_{out}1$	V_{in} = 115 Vac, $I_{out}1$ = 1.0 to 4.5 A	Δ = 3.0 mV or ± 0.03%
Output Ripple	$V_{out}1$	V_{in} = 115 Vac	40 mV_{p-p}
Short Circuit Current	$V_{out}1$	V_{in} = 115 Vac, R_L = 0.1 Ω	19.2 A
Line Regulation	$V_{out}2$ or 3	V_{in} = 92 to 138 Vac	Δ = 10 mV or ± 0.04%
Load Regulation	$V_{out}2$ or 3	V_{in} = 115 Vac, $I_{out}2$ or 3 = 0.25 to 0.8 A	Δ = 384 mV or ± 1.6%
Output Ripple	$V_{out}2$ or 3	V_{in} = 115 Vac	80 mV_{p-p}
Short Circuit Current	$V_{out}2$ or 3	V_{in} = 115 Vac, R_L = 0.1 Ω	10.8 A
Efficiency		V_{in} = 115 Vac	75.7%

All outputs are at nominal load current unless otherwise noted.

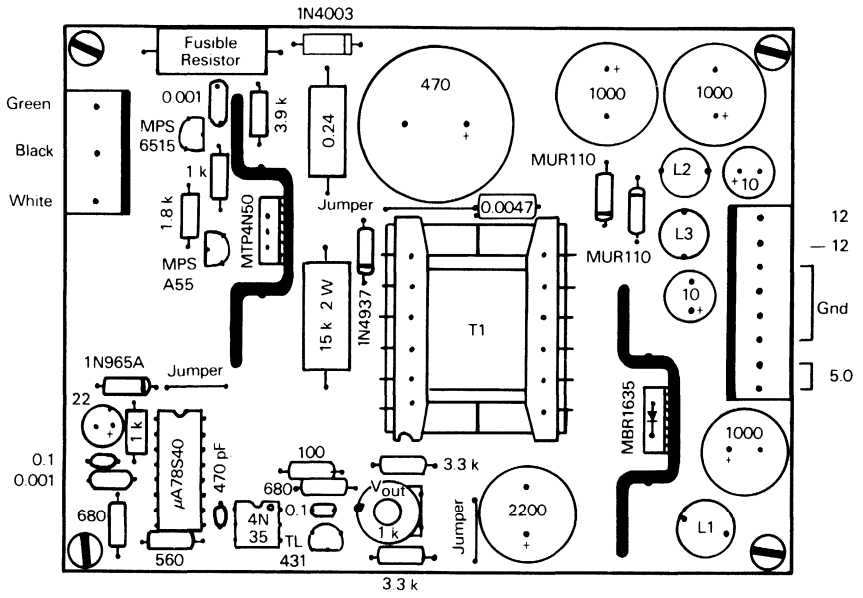
*Heat sink
Thermalloy 6072B-MT

T1 — Primary:
Pins 4 and 6 = 72 Turns #24 AWG } Bifilar Wound
Pins 5 and 6 = 72 Turns #26 AWG }
Secondary 5.0 V:
6 Turns (two strands) #18 AWG Bifilar Wound.
Secondary ± 12 V:
14 Turns #23 AWG Bifilar Wound.
Core and Bobbin:
Coilcraft PT3995.
Gap: 0.030" Spacer in each leg for a primary inductance of 550 μH.
Primary to primary leakage inductance must be less than 30 μH.

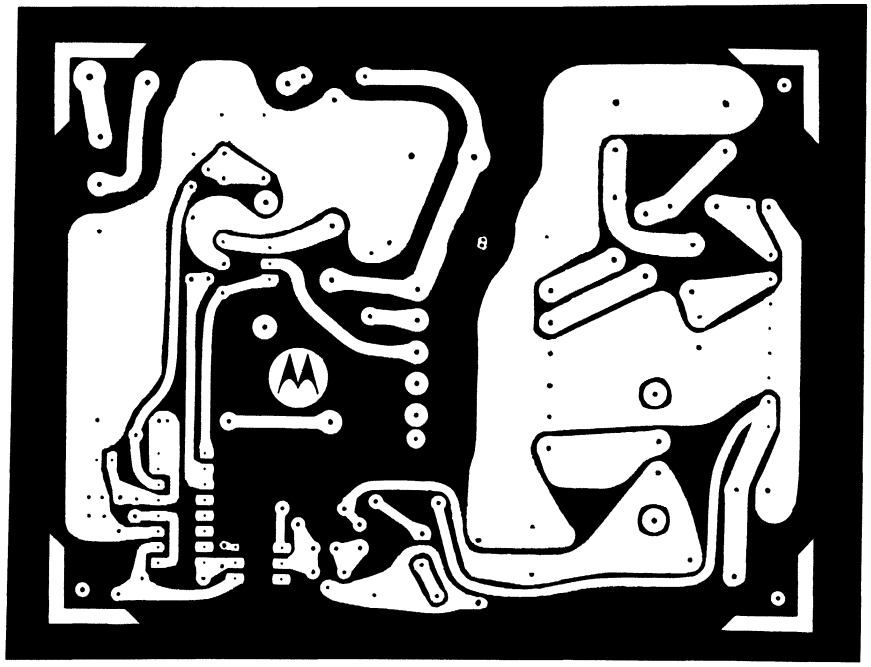
L1 — Coilcraft Z7156:
Remove one layer for final inductance of 4.5 μH

L2, L3 — Coilcraft Z7157:
25 μH at 1.0 A

Figure 13-35. 42 Watt Off-Line Flyback Switcher with Primary Power Limiting

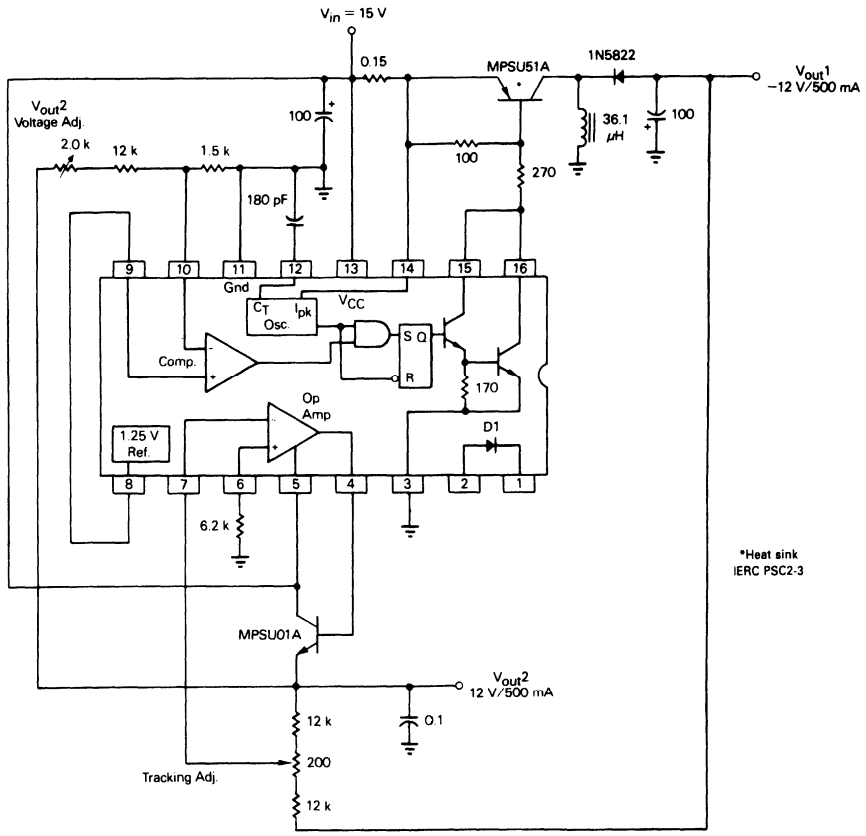


Component Layout — Bottom View



Printed Circuit Board Negative — Bottom View

Figure 13-36. 42 Watt Off-Line



Test		Conditions	Results
Line Regulation	$V_{out}1$	V_{in} = 14.5 to 18 V, $I_{out}1$ = 500 mA, $I_{out}2$ = 500 mA	Δ = 10 mV or ± 0.042%
Load Regulation	$V_{out}1$	V_{in} = 15 V, $I_{out}1$ = 100 to 500 mA, $I_{out}2$ = 500 mA	Δ = 2.0 mV or ± 0.008%
Output Ripple	$V_{out}1$	V_{in} = 15 V, $I_{out}1$ = 500 mA, $I_{out}2$ = 500 mA	125 mV_{p-p}
Line Regulation	$V_{out}2$	V_{in} = 14.5 to 18 V, $I_{out}1$ = 500 mA, $I_{out}2$ = 500 mA	Δ = 10 mV or ± 0.042%
Load Regulation	$V_{out}2$	V_{in} = 15 V, $I_{out}2$ = 100 to 500 mA, $I_{out}1$ = 500 mA	Δ = 5.0 mV or ± 0.021%
Output Ripple	$V_{out}2$	V_{in} = 15 V, $I_{out}1$ = 500 mA, $I_{out}2$ = 500 mA	140 mV p-p
Efficiency		V_{in} = 15 V, $I_{out}1$ = 500 mA, $I_{out}2$ = 500 mA	77.2%

This tracking regulator provides a ± 12 V output from a single 15 V input. The negative output is generated by a voltage-inverting converter while the positive is a linear pass regulator taken from the input. The ± 12 V outputs are monitored by the op amp in a corrective fashion so that the voltage at the center of the divider is zero ± V_{IO}. The op amp is connected as a unity gain inverter when $|V_{out}1| = |V_{out}2|$.

Figure 13-37. Tracking Regulator, Voltage-Inverting with Buffered Switch and Buffered Linear Pass from Input

B. AN INTRODUCTION TO THE MC34129 HIGH PERFORMANCE CURRENT-MODE CONTROLLER

A new current-mode control IC that interfaces directly with current sensing power MOSFETs is described. Its second generation architecture is shown to provide a variety of advantages in current-mode power supplies. The most notable of these advantages is a "lossless" current sensing capability that is provided when used with current sensing MOSFETs.

Included in the discussion are subtle factors to watch out for in practical designs, and an applications example.

Current-mode control is well known for the dynamic performance advantages that it brings to switching power supplies. In response to these advantages, two generations of integrated circuits have been developed. The first generation simplified component counts and made current-mode topologies economically competitive. Second generation products have focused on two additional types of improvements. One approach emphasizes high speeds in critical control loops. The other emphasizes CMOS like bias power requirements and compatibility with current sensing power MOSFETs.

Motorola's MC34129 fits into the second category. Its architecture provides very low bias power consumption, 300 kHz operation, and full compatibility with current sensing power MOSFETs. The latter advantage is particularly important since it allows more efficient current sensing. Instead of running amps through a power sense resistor, primary current is split into power and sense components by new power MOSFETs called SENSEFETs. The sense portion, typically milliamps, is run through a 1/4 watt sense resistor while the power component flows unimpeded to ground. Since power dissipation in the sense resistor is reduced by several orders of magnitude, the circuit technique is called lossless current sensing.

Fully taking advantage of lossless current sensing's benefits requires a control circuit topology which differs somewhat from first generation current-mode control IC's. The MC34129 fills the void with its second generation design.

MC34129 Description

In order to work well with SENSEFETs, current-mode control circuitry has to accept relatively low values of sense voltage. First generation current-mode control IC's will accept these voltages during regulation, but are often found lacking under short circuit conditions. Short circuit current limit thresholds usually exceed sense voltages that are practically attainable with SENSEFETs.

The MC34129 has an architecture which works quite well with SENSEFET output voltages, and provides a number of other features. An illustration of the circuit and a timing diagram are included in Figure 13-38. A block by block description follows from this figure.

Oscillator:

The oscillator is programmed for operating frequency and maximum duty cycle by components R_T and C_T. Capacitor C_T is charged from a 2.5 volt reference through resistor R_T to approximately 1.25 volts and discharged by an internal current sink to ground. During the discharge of C_T, an internal blanking pulse is generated that holds the NOR gate's lower input high. This arrangement causes the Drive Output (Pin 1) to be in a low state, thereby producing a controlled amount of dead time. Note that many values of R_T and C_T will give the same

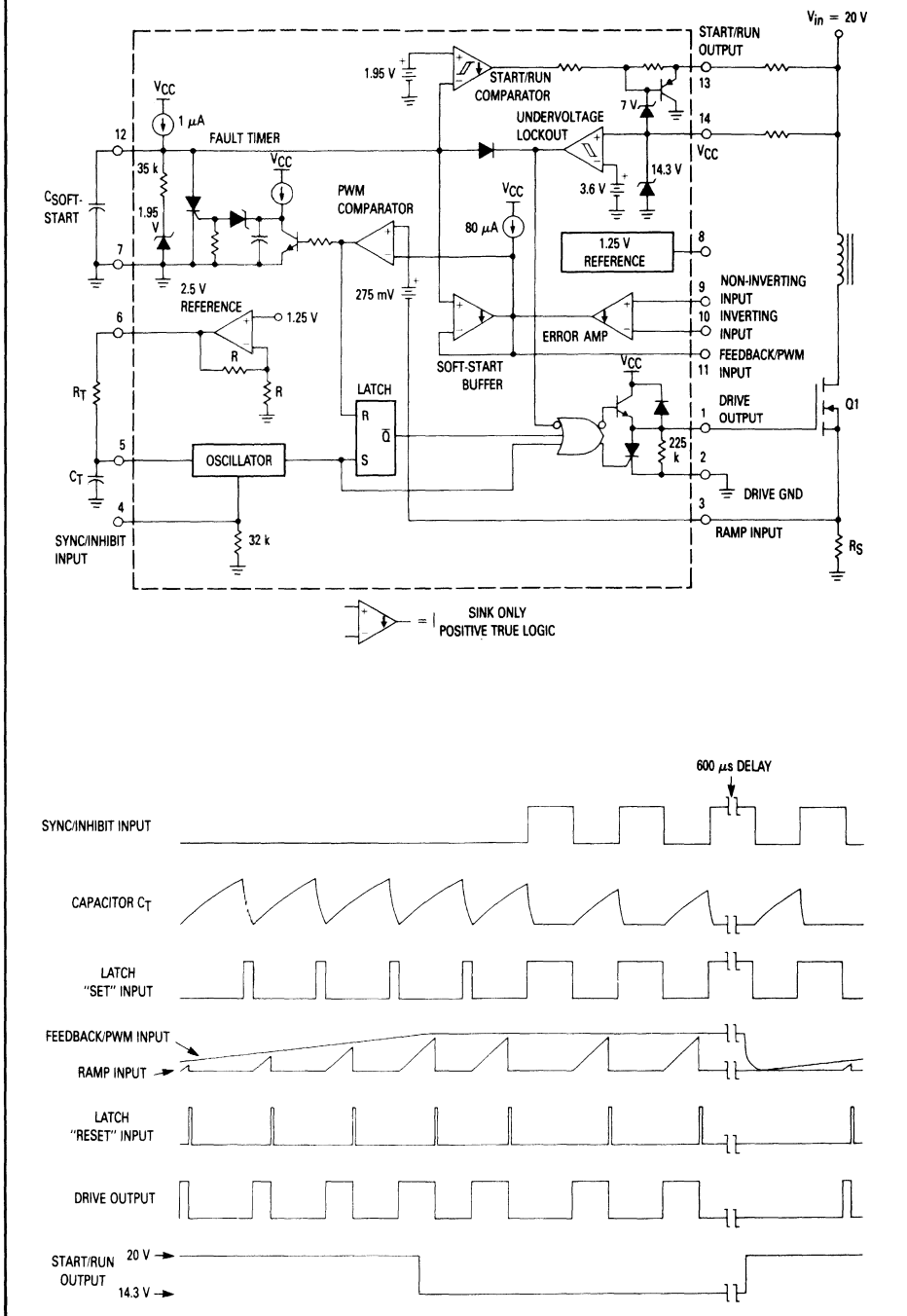


Figure 13-38. Block Diagram

oscillator frequency but only one combination will yield a specific deadtime at a given frequency.

For many noise sensitive applications, it is desirable to frequency lock one or more switching regulators to an external clock. This can be accomplished by applying a clock signal to the Sync/Inhibit Input. For reliable locking, R_T and C_T should be set for approximately 10% less than the external clock frequency. Operation is illustrated by timing waveforms in Figure 13-38. The external clock's rising edge terminates charging of C_T and forces Pin 1 low. As long as the clock is high, Pin 1 remains low. At the clock's falling edge C_T begins charging again, Pin 1 is enabled, and the cycle repeats.

By tailoring the clock waveform, accurate duty cycle clamping of the Drive Output can be achieved. The Sync/Inhibit Input may also be used as a means for system shutdown by applying a dc voltage that is within the range of 2 volts to V_{CC}.

PWM Comparator and Latch:

The MC34129's PWM architecture is designed such that output switch conduction is initiated by the oscillator and terminated when peak inductor current reaches a threshold level. A unique arrangement establishes the threshold level with an Error Amp and Soft Start Buffer whose outputs are tied together at Pin 11. This arrangement controls peak inductor current on a cycle by cycle basis regardless of whether duty cycle is limited by the error signal, soft start, or an output fault. The PWM Comparator-Latch configuration that is used, ensures that only a single pulse appears at the Drive Output during any given oscillator cycle. The inductor current is converted to a voltage by inserting a ground-referenced resistor Rs in series with the Sense terminal of a SENSEFET or Source of a conventional power MOSFET.

The Ramp Input adds 275 millivolts of offset to whatever sense voltage is developed by Rs. This guarantees that no output pulses will appear when Pin 11 is at its lowest state, and provides adequate margin to overcome the error amplifier's minimum output voltage.

Under normal operating conditions, peak inductor current $I_{(pk)}$ is controlled by the voltage at Pin 11 such that:

$$I_{pk} = \frac{V\ (\text{Pin } 11) - 275\ \text{mV}}{(Rs/K)}$$

In this equation K is the ratio of inductor current to sense current. For conventional sense resistors, K is 1, and for SENSEFET applications K is the ratio of Drain current to Sense current.

Abnormal operating conditions occur when the power supply output is overloaded or if output voltage sensing is lost. Under these conditions, the PWM comparator's inverting input (Pin 11) will assume the error amp's maximum output voltage. This voltage determines peak switch current, and is clamped internally to 1.95 volts. Compatibility with SENSEFETs is provided by a configuration that easily allows clamping to much lower levels. One method is shown in Figure 13-39. It uses an external divider and a diode to clamp Pin 11's maximum voltage, and thereby adjust peak fault current. A second diode uses negative input bias current from Pin 3 (typically 120 μA) to provide compensation for the diode drop at Pin 11. Maximum switch current can be calculated as follows:

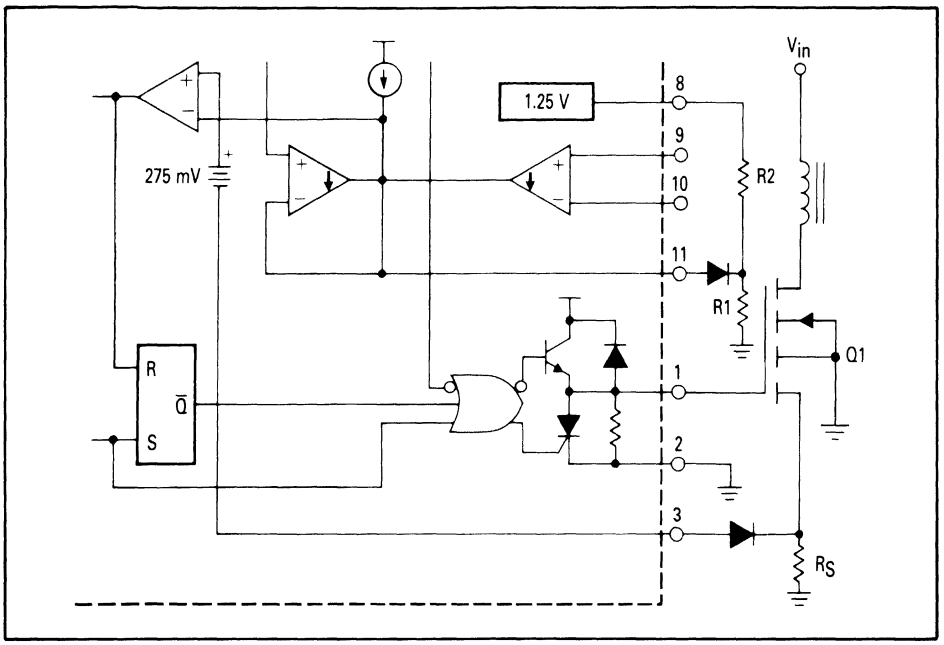


Figure 13-39. Fault Current Adjustment

$$I_{p(max)} = \left(\frac{1.25\ R1}{R1 + R2} - 0.275\right) \cdot K/R_S$$

Although this expression is straightforward, it is important to note that high frequency layout techniques are imperative.

A narrow spike on the leading edge of the current waveform can usually be observed and may cause the power supply to exhibit instability when its output is lightly loaded. This spike is due to power transformer interwinding capacitance, output rectifier recovery charge, and SENSEFET characteristics. The addition of an RC filter on the Ramp Input with a time constant that approximates the spike duration will usually eliminate the instability. A typical connection is shown in Figure 13-40.

Error Amp and Soft Start Buffer:

A fully compensated Error Amplifier with access to its output and both inputs is provided for maximum design flexibility. The Error Amplifier output is tied to the output of the Soft Start Buffer. These outputs are open collector (sink only) and feed the inverting input of the PWM Comparator. With this configuration, the amplifier that demands lower peak inductor current dominates control of the PWM loop.

The Soft Start Buffer is configured as a unity gain follower with its non-inverting input connected to Pin 12. An internal 1 μA current source charges the soft-start capacitor ($C_{soft\text{-}start}$) to Pin 11's clamp voltage. The rate of change of peak inductor current during startup is programmed by the capacitor value selected.

Fault Timer:

This unique circuit prevents sustained operation in a lockout condition. Lockout can occur with conventional switching control IC's when operating from a power source with a high series impedance. If power required by the load is greater than power available from the source, input voltage will collapse and cause a lockout condition. The Fault Timer provides automatic recovery when this condition is detected. Under normal operating conditions the PWM Comparator will reset the Latch and discharge the Fault Timer's internal capacitor on a cycle-by-cycle basis. Under operating conditions where input power is insufficient for the load, Ramp Input Voltage (plus offset) will not reach the threshold established at Pin 11, and the PWM Comparator's output will remain low. If this condition persists for more than 600 μs, the Fault Timer will activate, discharging $C_{soft\text{-}start}$ and initiating a soft-start cycle. The power supply will operate in a skip cycle or hiccup mode until either the load, or source impedance, is reduced. When either occurs, normal operation resumes automatically.

Start/Run Comparator:

A bootstrap startup circuit is included to improve system efficiency when operating from a high input voltage. For this purpose, a Start/Run Comparator controls the state of an external transistor. A typical application is shown in Figure 13-41. While $C_{soft\text{-}start}$ is charging, startup bias is supplied to V_{CC} (Pin 14) from V_{in} through transistor Q2. When $C_{soft\text{-}start}$ reaches 1.95 volts, the Start/Run output switches low and turns off Q2. Operating bias is now derived from an auxiliary bootstrap winding, and drive power is efficiently converted down from V_{in}. A

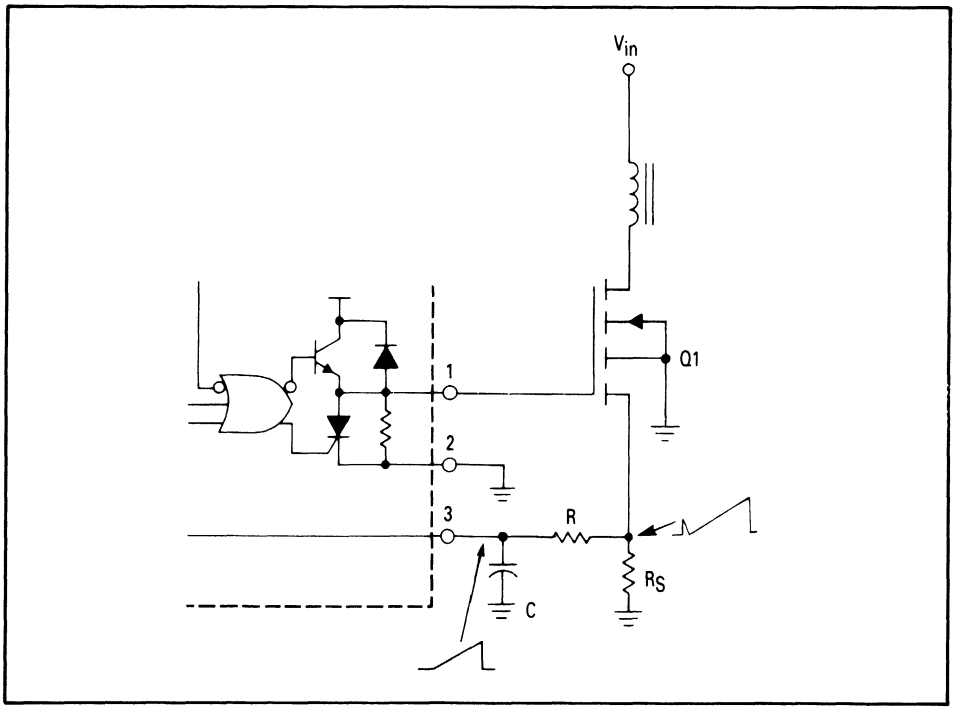


Figure 13-40. Ramp Filter

smooth switchover is facilitated by 350 mV of hysteresis in the Start/Run Comparator.

An important constraint is that start time must be long enough for the power supply to reach regulation. This ensures that there is sufficient bias voltage at the auxiliary winding for sustained operation. An adequate value of $C_{soft\text{-}start}$ can be determined from the following expression:

$$t_{start} = \frac{1.95\ V \bullet C_{soft\text{-}start}}{1\ \mu A} = 1.95\ C_{soft\text{-}start}\ in\ \mu F$$

In addition, use of the Start/Run feature implies that the error amplifier's maximum output voltage has not been clamped externally.

Drive Output and Drive Ground:

The MC34129 contains a single totem-pole output stage that is specifically designed for direct drive of power MOSFET's. It is capable of up to ± 1 amps peak drive current and has a typical fall time of 30 ns with a 500 pF load. The totem-pole stage consists of an NPN transistor for turn-on drive and a high speed SCR for turn-off. The SCR design requires less average supply current (I_{CC}) than conventional switching control IC's that use all NPN totem-poles. The improvement comes during turn-off, where the SCR is able to use the power MOSFET's gate charge as regenerative on-bias. In contrast, a conventional all transistor design requires continuous base current. The improvement is large enough to allow bias from a series dropping resistor in many high input voltage applications.

An internal 225 kΩ pull-down resistor is included to shunt the Drive Output to ground when Undervoltage Lockout is active. In addition, a separate Drive Ground is provided in order to reduce the effects of switching transient noise

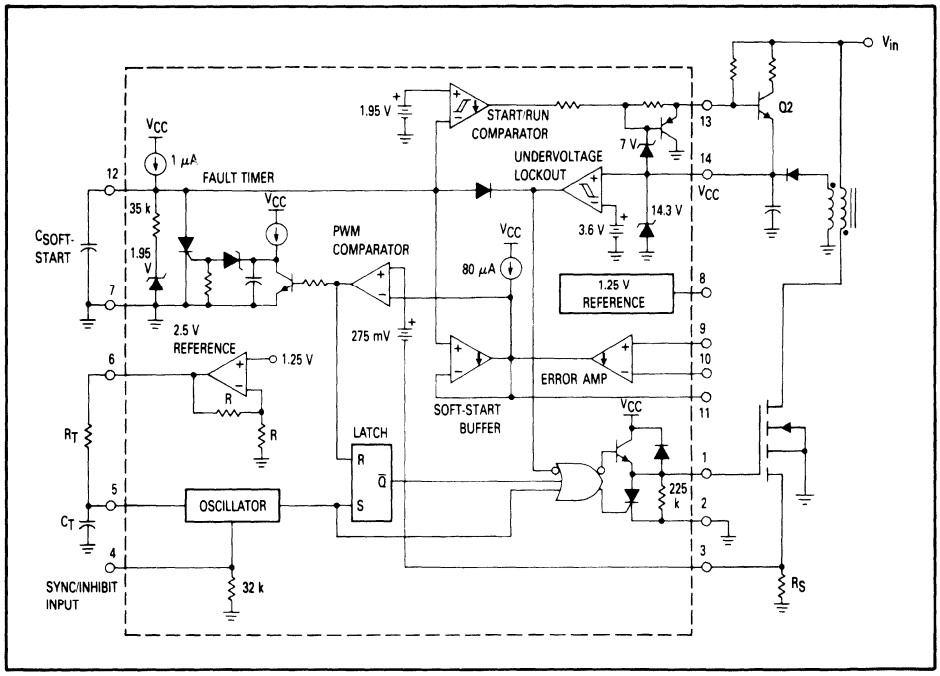


Figure 13-41. Bootstrap Bias

imposed on the Ramp Input. This feature becomes particularly useful when ramp voltage is provided by a current sensing power MOSFET.

Undervoltage Lockout:

An Undervoltage Lockout comparator holds both Drive Output and $C_{soft\text{-}start}$ pins low when V_{CC} is less than 3.6 volts. This ensures that the MC34129 is fully functional before the output stage is enabled and a soft-start cycle begins. Built in hysteresis of 350 mV prevents erratic behavior as V_{CC} crosses the threshold voltage. In addition, a 14.3 volt zener is connected as a shunt regulator to protect the output transistor's gate from excessive drive voltage during system startup. An external 9.1 volt zener is required when driving low threshold MOSFET's as shown in Figure 13-42. The minimum operating voltage range is 4.2 volts to 12 volts.

References:

Two reference voltages are provided. The 1.25 volt bandgap reference at Pin 8 is trimmed to a ±2% tolerance at 25°C. It is intended to be used in conjunction with the Error Amp for output voltage regulation. An additional 2.5 volt reference is derived from the 1.25 volt bandgap by an internal Op amp that has a fixed gain of 2. It has a tolerance of ±5% at 25°C. Its primary purpose is to supply charging current for the oscillator's timing capacitor.

Lossless Current Sensing

Lossless current sensing is a new circuit technique that is particularly well suited to current-mode control. It is derived from the parallel nature of power MOSFETs and implemented with new devices called SENSEFETs. These new

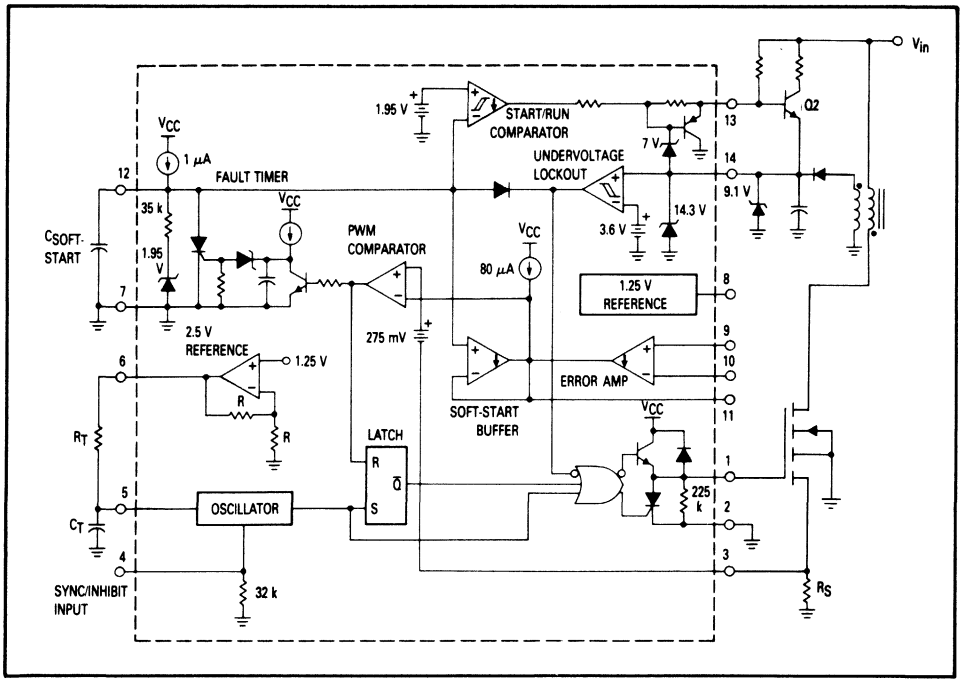


Figure 13-42. Gate Protection

devices are five leaded power MOSFETs that have the usual Gate, Drain, and Source connections; plus Current Sensing and Kelvin Source pins. The Sense pin connects to a small fraction of many paralleled Source cells that make up a power MOSFET. The Kelvin connection provides a separate signal ground. A symbol and sense resistor connection are shown in Figure 13-43.

In the circuit of Figure 13-43, sense current is a small fraction of total drain current. Even at maximum rated drain current, sense current is only milliamps, allowing a signal level resistor to be used for Rs. Sense power is so small compared to using a power sense resistor that the circuit technique is called lossless current sensing.

Lossless current sensing is based upon the parallel nature of power MOSFETs, and the inherent tendency of individual paralleled cells in a monolithic structure to be well matched. Matching provides nearly equal on-resistance in each cell, and establishes a ratio between Sense current and Source current. When both Sense and Source leads are grounded this ratio approximates the cell ratio (n). In this situation, the Sense lead samples $1/(n+1)$ of a SENSEFET's total drain current.

Converting sense current to sense voltage in a resistor disturbs this ratio, but in a predictable way. Sense resistance attenuates sense current in proportion to the amount that it increases total resistance in the sense leg. It is tempting to model sense resistor interaction with the circuit in Figure 13-44. From this model you would expect sense current to halve when Rs and the sense section's on-resistance ($r_{DM(on)}$) are equal.

Although this is a reasonable first order approximation for low voltage devices, two significant deviations make an accurate calculation of sense current rather complex. One of these is a non-linearity that results from the square law behavior of power MOSFETs. As Rs and sense voltage are increased, the sense section's drain-source voltage is decreased and $r_{DM(on)}$ increases non-linearly. The result is an apparent cell ratio n′ that increases with increasing sense voltage. An approximate expression for n′ can be derived from the model in Figure 13-44 as follows:

$$n' = \frac{n}{1 - \dfrac{V_{sense}\,(V_{GS} - V_T - 1/2\,V_{sense})}{V_{DS(on)}\,(V_{GS} - V_T - 1/2\,V_{DS(on)})}}$$

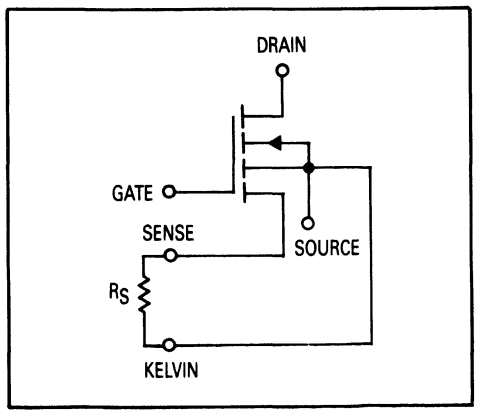


Figure 13-43. SENSEFET Symbol

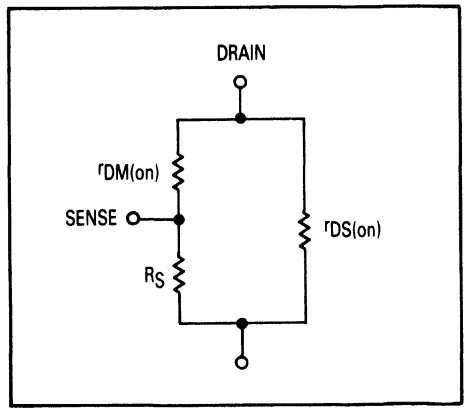


Figure 13-44. Current Sensing Model

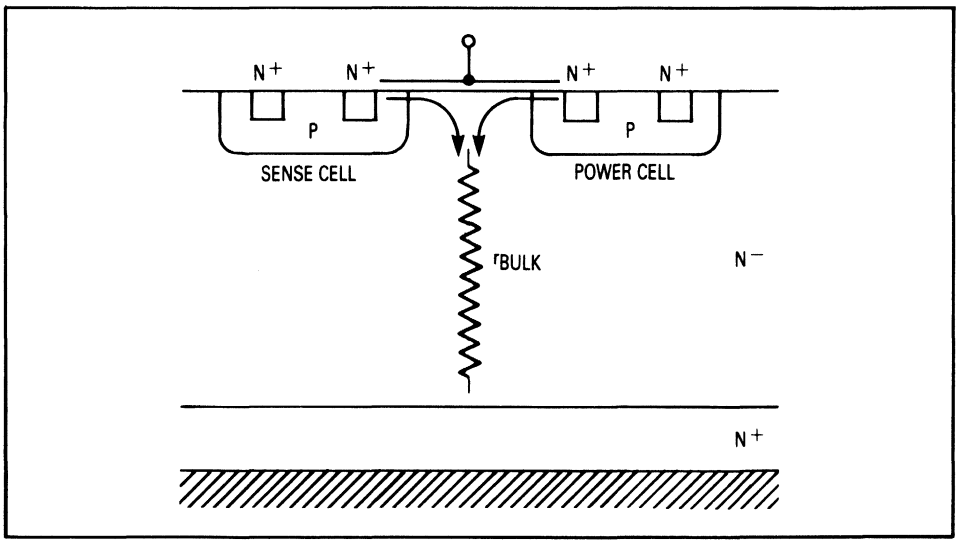


Figure 13-45. SENSEFET Cross-Sectional View

where V_{GS} is the applied gate-to-source voltage, V_T is gate-to-source threshold voltage, and V_{sense} is the sense voltage.

The foregoing expression is approximately valid for low voltage SENSEFETs such as the MTP10N10M at sense voltages up to 25% of $V_{DS(on)}$. However, there is another level of complexity that is not taken into account by Figure 13-44. Although sense cells and power cells have a parallel drain connection, they are not paralleled at the physically available drain terminal. Figure 13-45 shows why. The drain voltage that a sense cell actually sees is influenced by high current flowing through the power section. Apparent drain voltage at the sense cell includes voltage drops across channel and pinch regions, but does not include voltage drop in the N-epitaxial layer that supports breakdown. Therefore, a more appropriate model includes bulk resistance that is common to both power and sense cells. Figure 13-46 shows the resulting schematic.

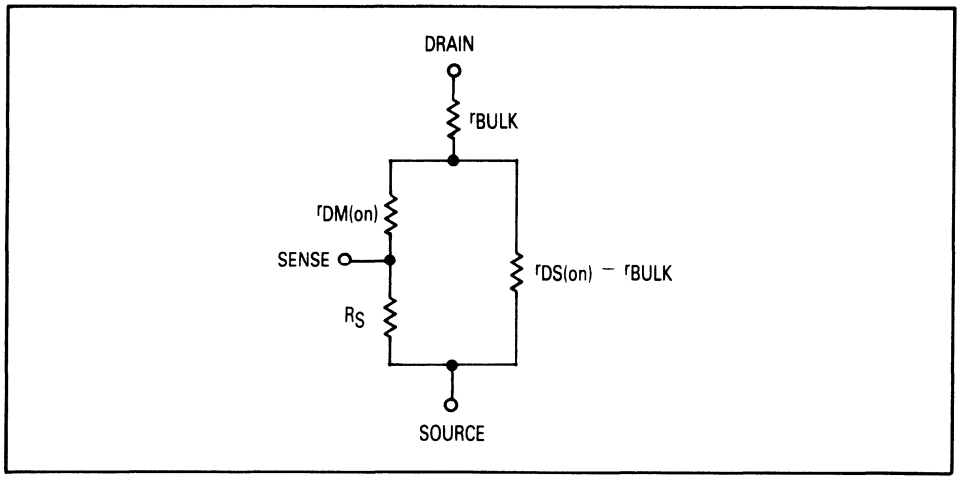


Figure 13-46. Refined Model

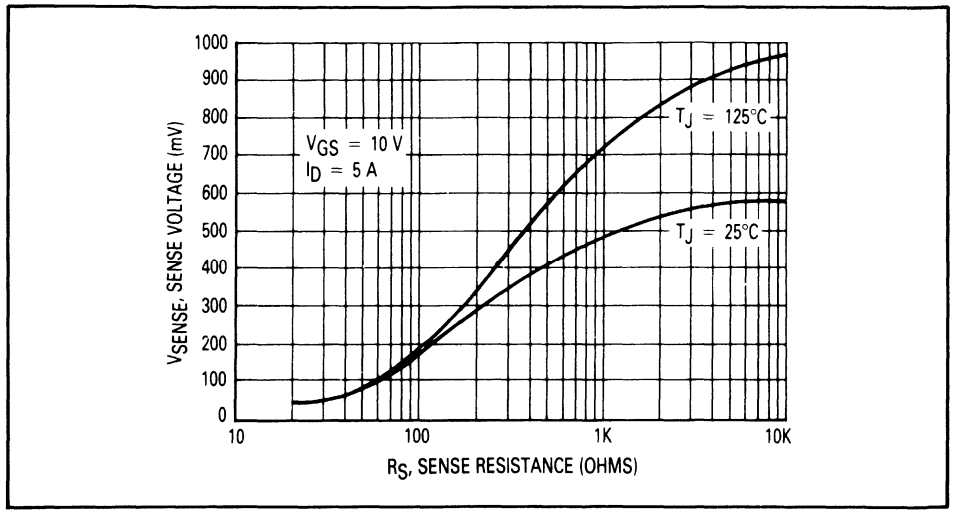


Figure 13-47. Sense Voltage versus Sense Resistance

Applying square law behavior to this model results in a rather complex calculation. Therefore, SENSEFET data sheets include curves of V_{sense} versus Rs at a fixed value of drain current and V_{sense} versus drain current for several values of sense resistance. Examples of these curves for an MTP10N10M, 10 amp/100 volt SENSEFET appear in Figures 13-47 and 13-48.

These curves illustrate a couple of interesting points. First, sense voltages are generally quite small. A 100 mV full load ramp voltage would not be unusual in a current-mode supply. Second, as the divergence in Figure 13-47 indicates, accuracy is maximized by minimizing Rs. In this case temperature tracking is almost perfect for values of Rs below 50 ohms, and diverges rapidly above 100 ohms. Initial tolerance follows a similar pattern. Below 20 ohms initial tolerance is within 6%, but increasing Rs to 2 kΩ increases this limit an estimated 25%.

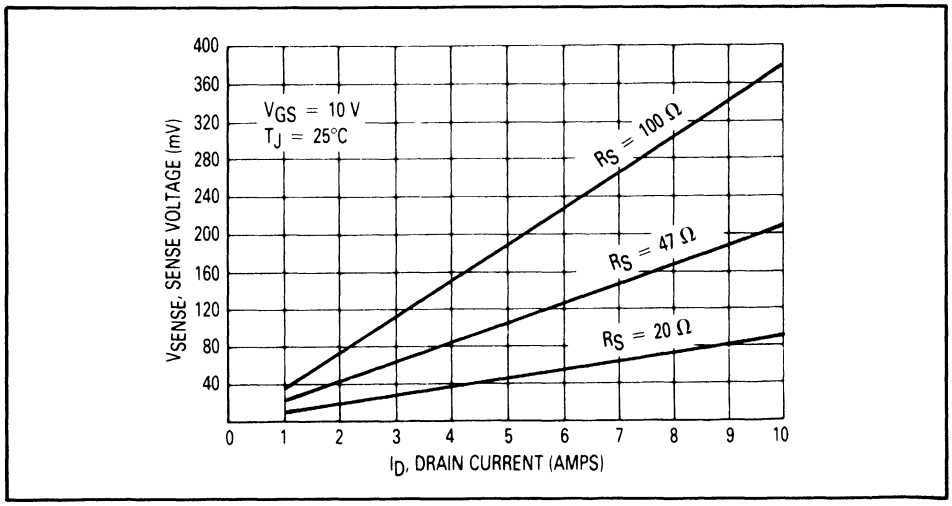


Figure 13-48. Drain Current versus Sense Voltage

The reason for this type of performance is simple. As Rs is minimized, the dependence of sense current upon matching within a monolithic device is maximized. On the other hand, as R_{sense} is increased, sense current depends more and more on the ratio of a fixed external resistor to $r_{DM(on)}$, r_{BULK}, and $r_{DS(on)}$. Matching produces by far the best results.

Using the MC34129 and SENSEFETs Together

An example which illustrates how the MC34129 and SENSEFETs are used appears in Figure 13-49. This figure describes an isolated 12 volt to 5 volt current-mode supply, and is a convenient vehicle for describing how both parts work together.

Starting with the oscillator, R_T and C_T are selected for operating frequency and dead time. A combination of 13 k for R_T and 1500 pF for C_T produces 28 kHz operation with slightly less than 50% maximum duty cycle. Ramp voltage is generated by Rs and fed into the PWM comparator's non-inverting input at Pin 3. The ramp's magnitude is determined by the value of Rs, the amount of primary current (I_P) that is switched, and $-120\ \mu A$ of nominal input bias current that flows from Pin 3. With the aid of Figure 13-47,

$$\begin{aligned} V_{ramp} &= 60\ mV/Amp \bullet I_P + 120\ \mu A \bullet 200 \\ &= 60\ mV/Amp \bullet I_P + 24\ mV \end{aligned}$$

Knowing the relationship between V_{sense} and primary current, maximum short circuit current is set with voltage divider R1, R2. The output voltage from this divider is coupled through a unity gain Error Amp configuration to set the PWM comparator's upper trip point. To calculate the trip point, 275 mV of offset is added to the SENSEFET's output voltage. With the values shown, R1 and R2 set the upper trip point at 470 mV, and peak current is limited to approximately 2.8 amps.

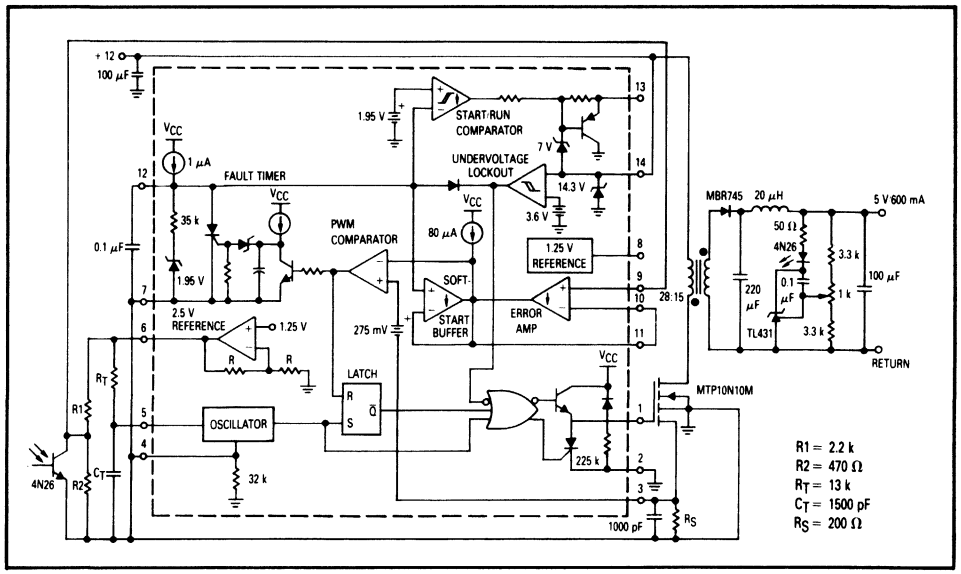


Figure 13-49. Application Example

Soft-start is provided with a 0.1 μF capacitor, which holds the output off for 27 ms, and allows full duty cycle after approximately 47 ms. The regulation loop is closed with an opto isolator which pulls down the voltage at Pin 9, thereby reducing peak primary current and also duty cycle. This configuration is advantageous in that it saves components. R1 and R2 are used to both limit peak current and provide a connection for the optoisolator.

Subtle Considerations

There are a number of subtle considerations that can be crucial in an MC34129/SENSEFET power supply. Several important issues are highlighted as follows.

Noise Suppression:

The MC34129 will drive a typical SENSEFET with transition times approaching 10 ns. At this speed, noise pickup in the current sensing circuitry can be a first order design issue. Layout, therefore, is critical. In addition, some filtering of the ramp input is usually desirable. To help with the layout problem, both MC34129 and SENSEFETs have separate power and signal ground pins. Use of these connections as indicated in Figure 13-49 can prevent noise related instability. At lower operating frequencies, series gate resistance can also be added to slow transition times, and create an optimum balance between switching losses and noise immunity.

Feedback:

The feedback configuration in Figure 13-49 has a number of interrelated constraints. One constraint is short circuit current. R1 and R2 are scaled to provide its desired value. These resistors are simultaneously subject to a 1 mA output current rating on the 2.5 volt reference. In addition, the opto transistor's collector works into an impedance determined by the parallel combination of R1 and R2. This configuration produces a voltage gain that influences loop gain, and therefore stability. With the components shown, a parallel combination of R1 and R2 that much exceeds 500 ohms tends to produce an open loop gain that is difficult to stabilize.

Opto Saturation:

In order to fully duty cycle the MC34129 back to zero, the opto transistor's collector has to pull Pin 9 below the voltage at the PWM comparator's non-inverting input. A 275 mV offset built into the MC34129 makes this relatively easy to do. However, the opto transistor's saturation voltage is a design consideration. Light load operation requires enough drive for the opto transistor to comfortably reach less than 275 mV of saturation voltage.

Conclusion

MC34129's and power SENSEFETs are significant new additions to the components available for current-mode control. By integrating power switching and current sense functions in a SENSEFET, and combining its features with the MC34129's control capabilities, simpler, more efficient, and more compact power supplies are possible.

Used together, these new components eliminate power sense resistors and make current-mode more attractive with respect to other architectures for switching power supplies. Both products will make a significant contribution in the shift toward current-mode topologies.

C. 60-WATT FLYBACK SWITCHING POWER SUPPLY DESIGN

The flyback-regulator circuit (Figures 13-50 and 13-51) with a single drive transistor needs only a few main parts:

A unique flyback transformer

A single control IC (MC34060)

A fast-switching high-voltage transistor

Single output filters in each of the four outputs

The flyback base-drive circuit

AC-line input voltage doublers.

In the power stage of Figure 13-50, a single 2N6545 transistor blocks 800 V and switches 1.0 A in 40 ns. The control section utilizes a low cost MC34060 Pulse Width Modulator control IC to minimize parts count.

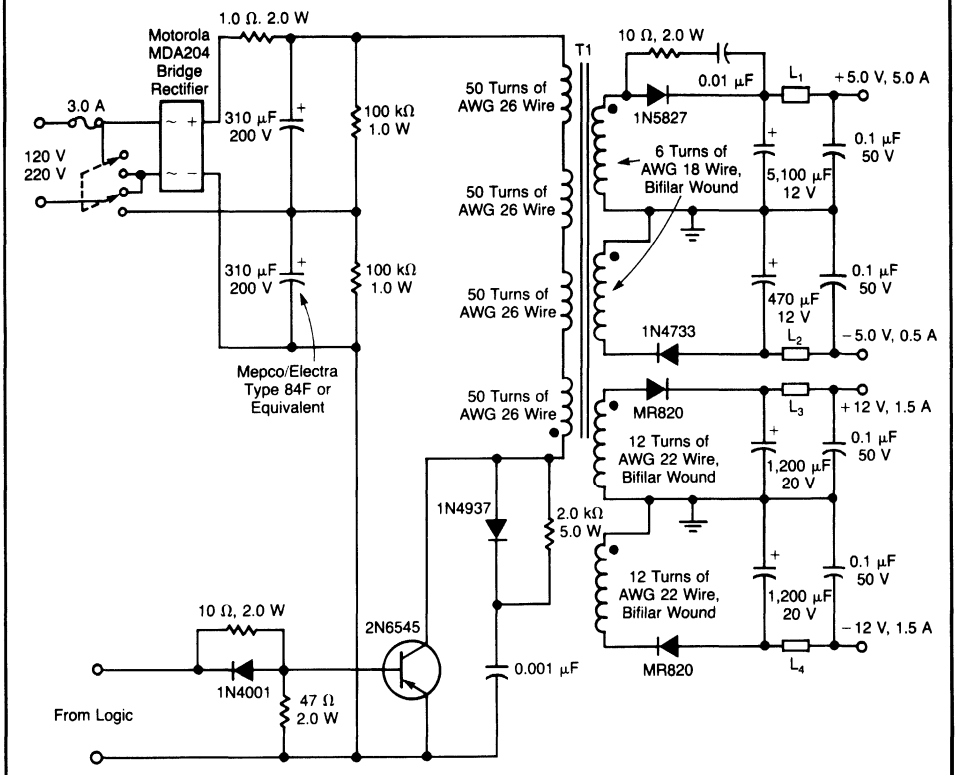
The following paragraphs provide useful information and performance results regarding this Flyback design.

1. Sandwiching The Windings

The flyback transformer uses an EC-41 ferrite core made by the Ferroxcube Corp. It has a 40:1 turns ratio and is wound by a sandwich technique that improves the coupling between its primary and secondary windings.

The primary winding consists of four split windings in series with each other. The four windings of the secondary alternate in a sandwich construction with the four primary windings. Total core gap is 100 mils, and primary-winding inductance is 4.5 millinenries at 2.5 amperes. Transformer performance can be gauged from the fact that although the output current ratings for the secondary transformer windings are specified as 5.0, 1.5, and 0.5 A for 5.0 ± 12, and −5.0 V, respectively, actual respective current values are 8, 3, and 4 A (Figure 13-52). The flyback transformer can be hand-wound over an EC-41 ferrite core obtainable from Ferroxcube Corp. The four secondary windings alternate in a sandwich construction with four split primary windings that are connected in series with each other. All of the power-supply control functions reside in the MC34060 pulse width modulation control IC. It includes a 20-kilohertz oscillator, a dead-time adjustment (50% maximum) for preventing transformer saturation, two error amplifiers to process both current and voltage feedback signals, and an output stage that produces 200 milliampere pulses to drive the power transistor. An undervoltage-inhibiting circuit is added externally to the control IC. Consisting of two transistors and a zener diode, it inhibits output pulses when the drive voltage is less than 10 V.

For fast switching, a Motorola type 2N6545 transistor is used. It is capable of switching 2.0 A in just 40 nanoseconds and can block up to 800 V under worst-case conditions. Because of the transistor's high speed, losses due to the snubber (the RC network in the collector circuit) are low — typically 2.0 W, or less than 2% of the total delivered power. Output Transistor current and voltage waveforms, along with load lines, are shown in Figures 13-53 and 13-54.



T1 Specifications
Ferroxcube E Core EC41-3C8. Gap Poles of 50 mils (100 mils Total). Primary Inductance Is 4.0 mH at 3.0 A. Transformer Also Available from Pulse Engineering. #PE62792.

Winding Locations

Primary
+12 V
Primary
±5 V
Primary
−12 V
Primary

Seven Layers

L_1 through L_4
Ferrite Beads
0.3 in. Outside Diameter
0.09 in. Inside Diameter
0.3 in. Length
µ of 3,000

Output Capacitors
Sangamo Type 301, Mepco/Electra Type 3428, or Equivalent.

Figure 13-50. Flyback Power Stage Provides Output Voltages of +5, −5, +12 and −12 V

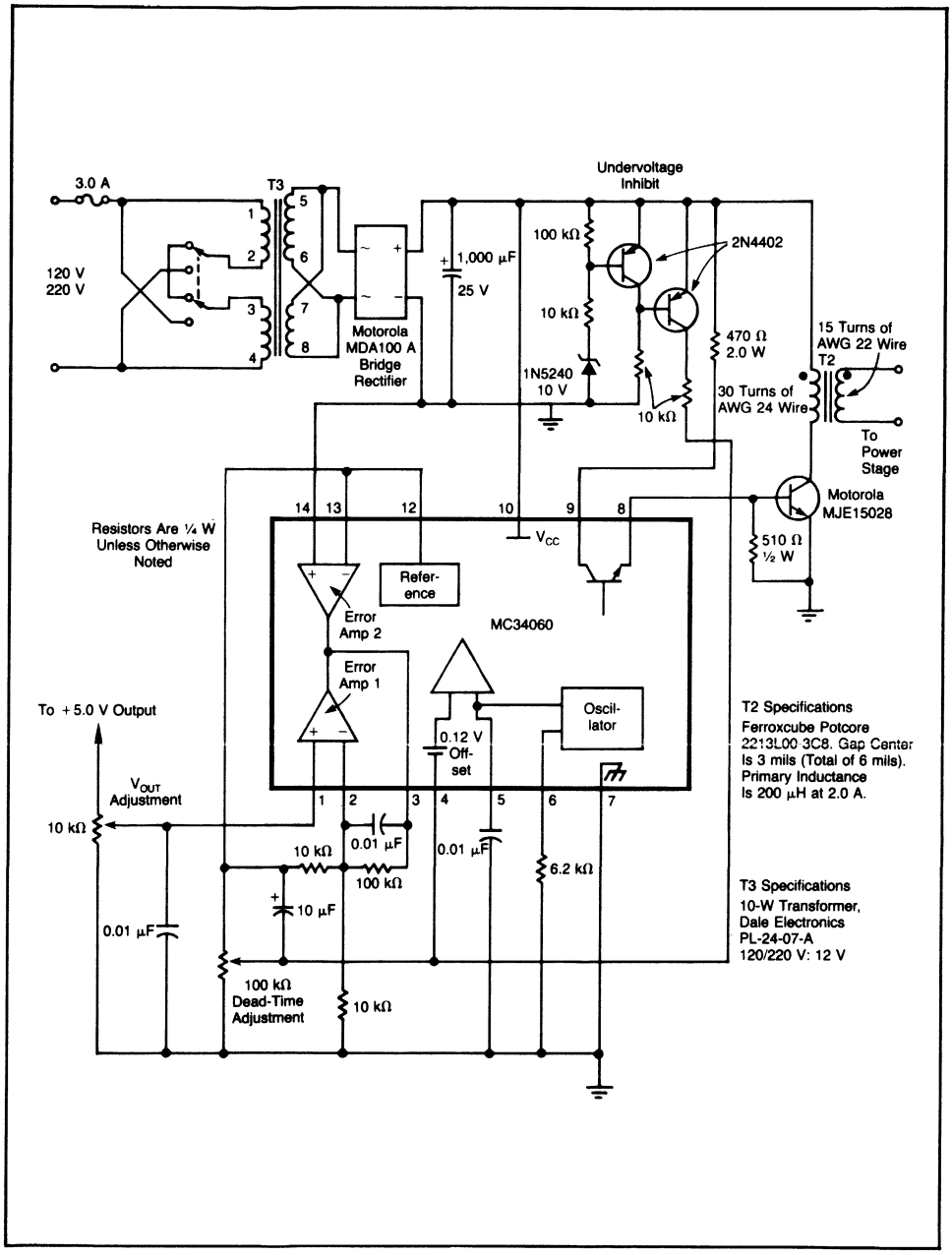


Figure 13-51. The Power Supply's Control Functions Are Obtained from The MC34060

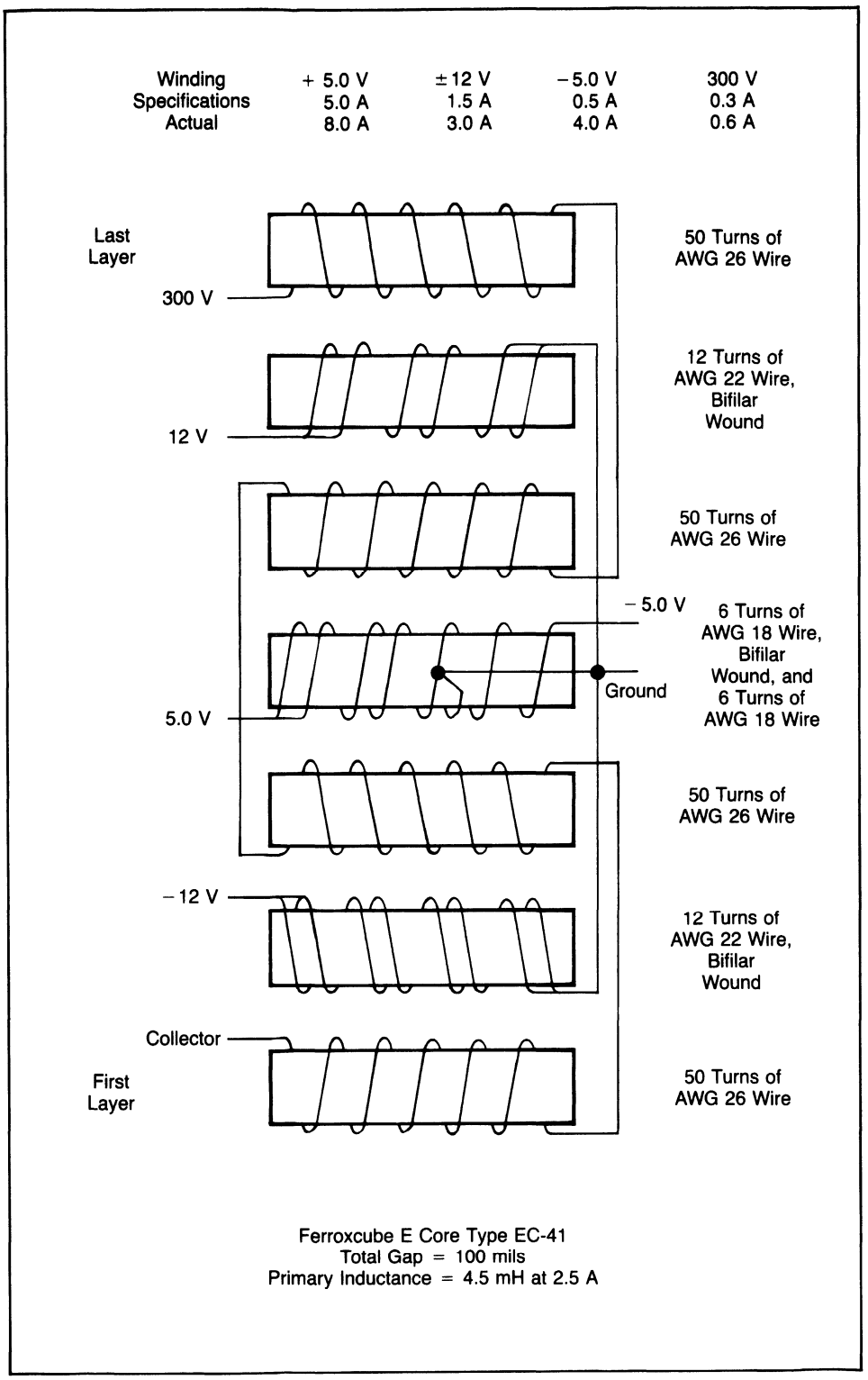
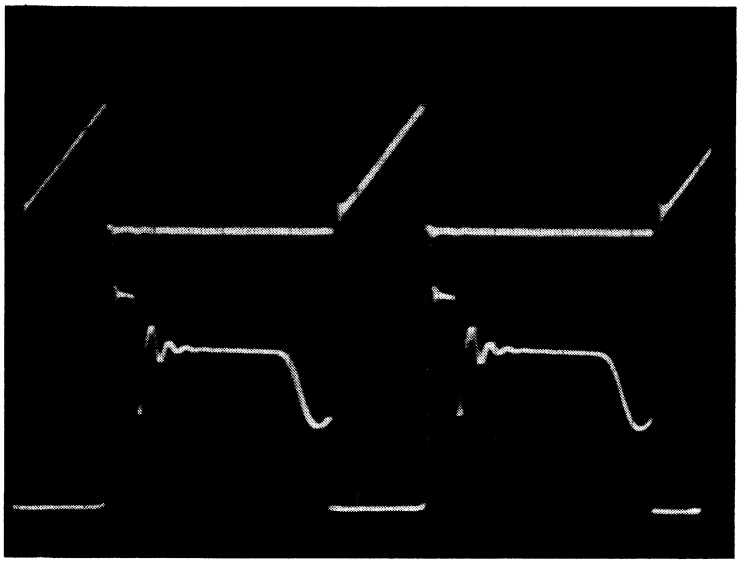


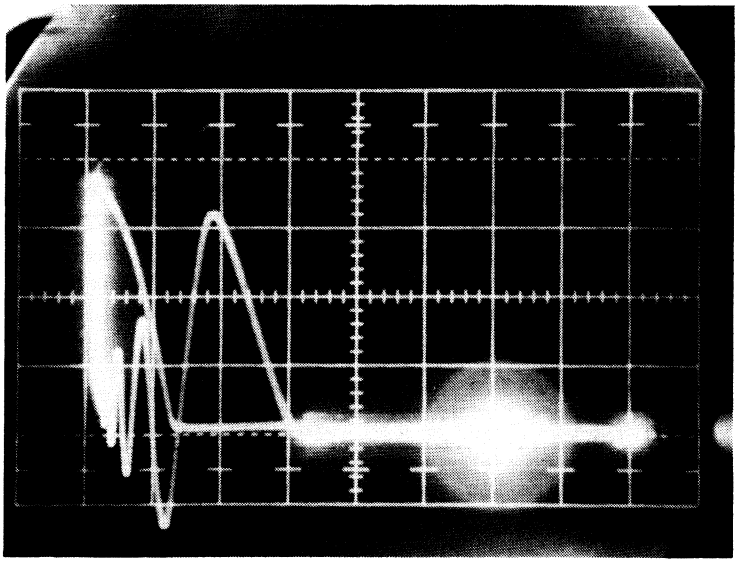
Figure 13-52. Flyback Transformer



Vertical Scale:
I_C = 0.5 A/cm

Horizontal Scale:
t = 10 μs/cm

Figure 13-53. 2N6545 Current and Voltage Waveforms



Vertical Scale:
I = 0.2 A/cm

Horizontal Scale:
V = 100 V/cm

Figure 13-54. 2N6545 Load Line

Each of the four output stages employs one filter capacitor and one diode. The capacitors (series 301 from Sangamo, 3428 from Mepco/Electra, or UPT from Cornell-Dubilier), exhibit low equivalent series resistance, typically 10 to 100 milliohms, Noise spikes are reduced dramatically (by as much as a factor of four) by the addition of a ferrite bead and ceramic capacitor across each of the output filter capacitors. Ripple test data for various types of capacitors is shown in Table 13-1.

The use of a flyback transformer for base drive greatly simplifies the drive circuit. Besides the transformer, only three other components are employed: a drive transistor capable of handling 2.0 A, a resistor, and a diode. The flyback transformer turns on the transistor with a 5.0 V drive pulse while simultaneously storing the energy from the 2.0 A current drawn by the transistor. This stored energy becomes the reverse bias drive when the pulse from the transformer is terminated. The reverse bias drive removes stored charge quickly — within 2 μs — and then causes the transistor's base to avalanche for the short while it takes to reset the transformer. Typically, if the transistor is initially turned on for 20 μs with a 5.0 V pulse, a 10 μs 10 V pulse is needed to reset it after it has been turned off.

At the ac line input, two axial-lead 310 μF, 200 V capacitors (Mepco/Electra series 84F) are connected in series with each other across the bridge rectifier output, thus acting as a voltage doubler when operating from 120 Vac line. A nominal 320 V bus is thus provided across the transformer's primary winding, regardless of whether it operates from a 120 Vac or a 220 Vac line input.

2. Advantages of Flyback — One of the most popular low wattage switching-regulator power supply circuits is the forward converter. The transformer, having only a 15:1 ratio of primary to secondary turns, is simpler than the flyback type approach, but requires four expensive filtering chokes. In addition, the secondary windings are unregulated, so output voltages vary with line and load variations more than they do in the case of a flyback transformer.

A flyback regulator with a control IC isolated from the primary side has a number of advantages. Feedback signals can be coupled directly to the transformer. Also, current-limiting protection on any or all of the output windings is simplified. Since the control IC has an extra amplifier, the addition of a sense resistor and simple divider network to the high-current 5.0 V output makes it easy to protect that output against short circuits (Figure 13-55). The addition of

TABLE 13-1. Ripple Test Data for Various Capacitors

Output	Test	Sangamo 301	Mepco/Electra 3428	CDE UPT	Mallory VPR	Sprague 432D
+5.0 V	Capacitance/volts	5,100 µF, 12 V	800 µF, 7.5 V	5,000 µF, 12 V	5,300 µF, 20 V	5,600 µF, 10 V
	Ripple (P-P)	200 mV	360 mV	170 mV	250 mV	200 mV
	Spikes (P-P)	660 mV	640 mV	980 mV	880 mV	580 mV
+12 V	Capacitance/volts	1,200 µF, 20 V	1,400 µF, 20 V	1,000 µF, 20 V	1,200 µF, 12 V	1,200 µF, 20 V
	Ripple	210 mV	260 mV	200 mV	200 mV	n.a.
	Spikes	740 mV	1,100 mV	1,800 mV	1,440 mV	n.a.
−5.0 V	Capacitance/volts	470 µF, 12 V	2,100 µF, 10 V	680 µF, 12 V	1,200 µF, 12 V	560 µF, 40 V
	Ripple	160 mV	160 mV	180 mV	140 mV	180 mV
	Spikes	540 mV	1,300 mV	680 mV	360 mV	440 mV

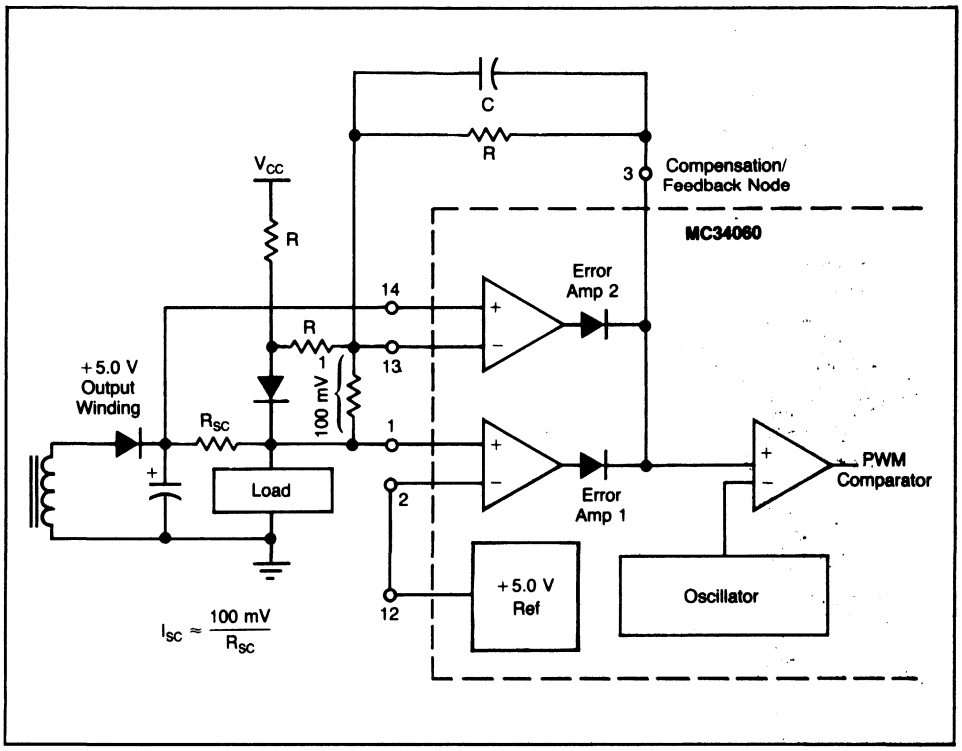


Figure 13-55. Current Limiting with the MC34060

three more similar networks and a quad operational amplifier makes it a simple matter to protect all four outputs against short circuits.

This approach breaks with convention. Other switching regulator schemes place the control IC at the primary side of the transformer, where the transistor emitter current is sensed for overcurrent protection. Optocouplers then have to be inserted in the feedback loop for proper isolation. Moreover, optocouplers drift over temperature.

3. Final Results — The output power stage can be checked out by using a pulse generator to energize the drive transistor and transformer; and subsequently, to calculate the snubber values. To improve coupling and reduce the 13 to 14 V nominal output to 12 V, the 5.0 V secondary winding can be increased from an initial five turns to six.

Adding control logic involves designing the base drive transformer and finding values for the feedback network that will provide optimum performance without creating instability. An operational amplifier gain of 20 with a rolloff at 160 Hz is sufficient. A dead-time limit of 50% keeps the drive transformer from saturation without interfering with low-line-voltage performance. An undervoltage-inhibiting circuit keeps the control circuit disabled at voltages under 10 V to prevent output pulses from occurring before sufficient drive is available to the output stage.

Despite the power supply's low parts count and simplicity of design, it has an impressive level of performance. For a nominal input of 120 Vac, it maintains regulation over an input range of 90 to 140 Vac and load range of 2:1 (half load to full load). For example, line and load regulation for the 5.0

V output are 2.5% and 1%, respectively. At an input of 90 Vac, full-load output voltages are 4.848, −4.930, −12.78 and 12.68 V, respectively, for the 5.0, −5.0, −12 and 12 V outputs. At 120 Vac, full-load output voltages are 5.001, −4.977, −12.98 and 12.94 V. At 140 Vac, full-load voltages are 5.983, −5.061, −13.16 and 13.10 V.

Half-load regulation is equally impressive. At a 90 Vac input, output voltages are 5.040, −5.075, −13.13 and 13.07 V. At a 120-V input, they are 5.098, −5.162, −13.30 and 13.20 V. At a 140-V input, they are 5.114, −5.191, −13.35, and 13.28 V.

Should it become necessary to work over a wider load range, such as from full to no load, the power transformer would have to be redesigned to protect the drive transistor from load dump conditions. This can be done by increasing the transformer's core size from the present EC-41 to EC-52 and by adding a primary bifilar winding coupled through a diode to the dc bus.

The power supply is also very efficient. At 120 Vac in a full-load condition, its efficiency was an impressive 80%. The only noticeable heat rise is in the small components like the snubber resistor and Schottky diode. All other components remain cool to the touch.

D. A SIMPLIFIED POWER-SUPPLY DESIGN USING THE TL494 CONTROL CIRCUIT

The TL494 is a fixed-frequency pulse width modulation control circuit, incorporating the primary building blocks required for the control of a switching power supply. (See Figure 13-56.) An internal-linear sawtooth oscillator is frequency-programmable by two external components, R_T and C_T. The oscillator frequency is determined by:

$$f_{osc} \cong \frac{1.1}{R_T C_T}$$

Output pulse width modulation is accomplished by comparison of the positive sawtooth waveform across capacitor C_T to either of two control signals. The NOR gates, which drive output transistors Q1 and Q2, are enabled only when the flip-flop clock-input line is in its low state. This happens only during that portion of time when the sawtooth voltage is greater than the control signals. Therefore, an increase in control-signal amplitude causes a corresponding linear decrease of output pulse width. (Refer to the timing diagram shown in Figure 13-57.)

The control signals are external inputs that can be fed into the dead-time control (Figure 13-56, Pin 4), the error amplifier inputs (pins 1, 2, 15, 16), or the feedback input (Pin 3). The dead-time control comparator has an effective 120 mV input offset which limits the minimum output dead time to approximately the first 4% of the sawtooth-cycle time. This would result in a maximum duty cycle of 96% with the output mode control (Pin 13) grounded, and 48% with it connected to the reference line. Additional dead time may be imposed on the output by setting the dead time-control input to a fixed voltage, ranging between 0 to 3.3 V.

The pulse width modulator comparator provides a means for the error amplifiers to adjust the output pulse width from the maximum percent on-time, established by the dead time control input, down to zero, as the voltage at the feedback pin varies from 0.5 to 3.5 V. Both error amplifiers have a common-mode input range from −0.3 V to (V_{CC} −2.0 V), and may be used to sense power-supply

output voltage and current. The error-amplifier outputs are active high and are ORed together at the non-inverting input of the pulse-width modulator comparator. With this configuration, the amplifier that demands minimum output on time, dominates control of the loop.

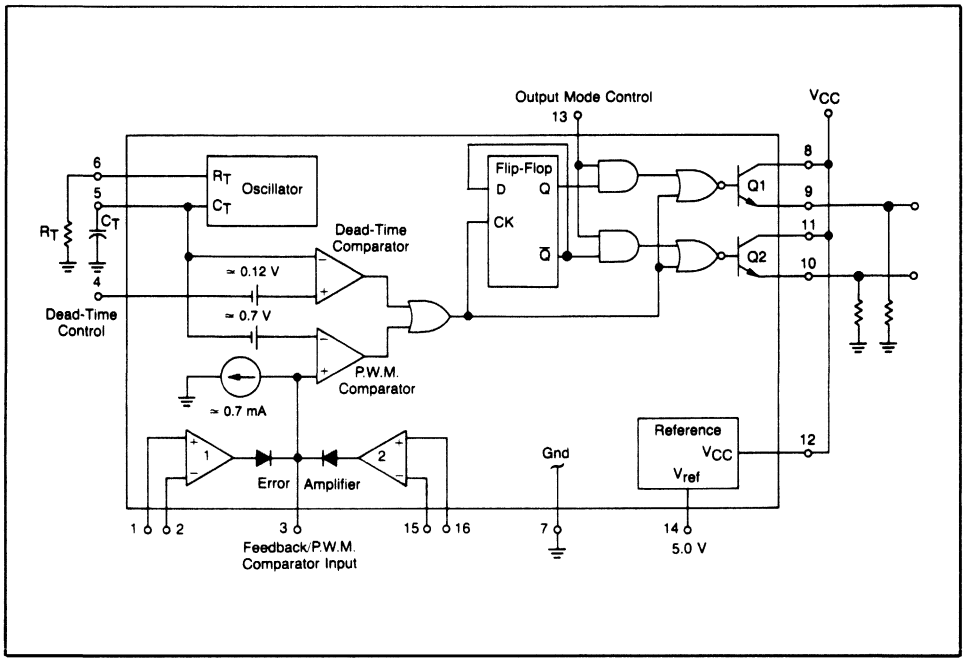


Figure 13-56. TL494 Block Diagram

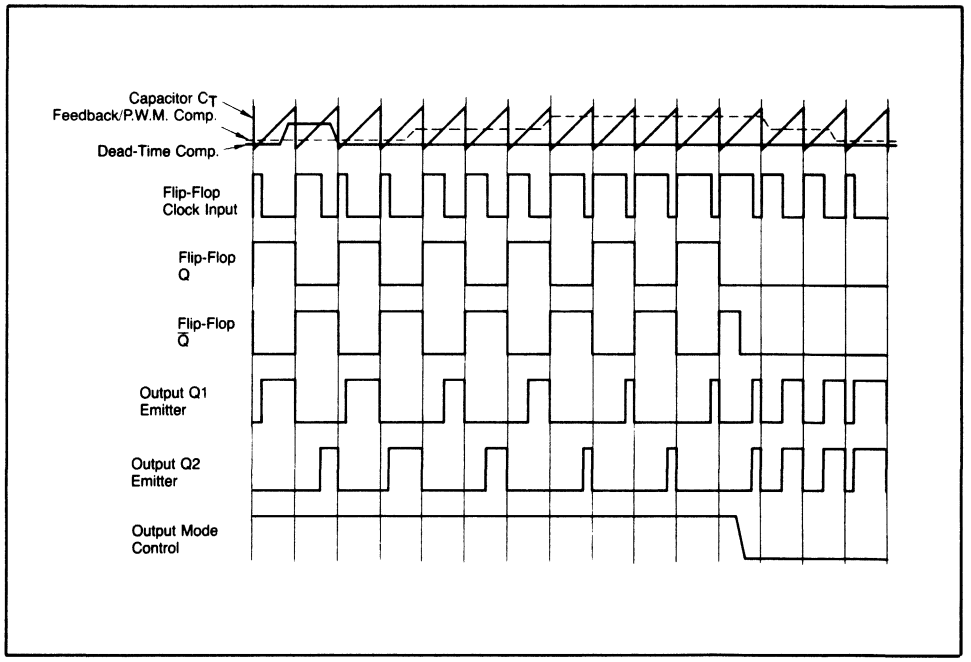


Figure 13-57. TL494 Timing Diagram

When capacitor C_T is discharged, a positive pulse is generated on the output of the dead-time comparator, which clocks the pulse-steering flip-flop and inhibits the otuput transistors, Q1 and Q2. With the output-mode control connected to the reference line, the pulse-steering flip-flop directs the modulated pulses to each of the two output transistors alternately for push-pull operation. The output frequency is equal to half that of the oscillator. Output drive can also be taken from Q1 or Q2, when single-ended operation with a maximum on time of less than 50% is required. This is desirable when the output transformer has a ringback winding with a catch diode used for snubbing. When higher output drive currents are required for single-ended operation, Q1 and Q1 may be connected in parallel, and the output mode control pin must be tied to ground to disable the flip-flop. The output frequency will now be equal to that of the oscillator.

The TL494 has an internal 5.0 V reference capable of sourcing up to 10 mA of load currents for external bias circuits. The reference has an accuracy of $\pm 5\%$ over an operating temperature range of 0 to 70°C.

Application of The TL494 in a 400 W and 1000 Watt Off-Line Power Supply

A 5 V, 80 A line operated 25 kHz switching power supply, designed around the TL494, is shown in Figure 13-58, and the performance data is shown in Table 13-2. The explanation of each section of the power supply, which follows, applies not only to this model but to the higher power (12 V, 84 A) model shown in Figure 13-59, as well. In comparing the two, note that the 400-watt design is a half-bridge, while the 1,000 watt is a full bridge. The 1,000 watt power supply components switching transistors, transformers, and output rectifiers have been beefed up.

1. AC Input Section

The operating ac line voltage is selectable for a nominal of 115 or 230 volts by moving the jumper links to their appropriate positions. The input circuit is a full wave voltage doubler when connected for 115 Vac operation with both halves of the bridge connected in parallel for added line surge capability. When connected for 230 Vac operation, the input circuit forms a standard full wave bridge.

The line voltage tolerance for proper operation is -10, $+20\%$ of nominal. The ac line inrush current, during power-up, is limited by resistor R1. It is shorted out of the circuit by triac Q1, only after capacitors C1 and C2 are fully charged, and the high frequency output transformer T1, commences operation.

TABLE 13-2

400 Watt Switcher Performance Data

Test	Conditions		Results
	Input	Output	
Line Regulation	103.5 to 138 VAC	5 volts and 80 amps	8 mV 0.16%
Load Regulation	115 VAC	5 volts, 0 to 80 amps	20 mV 0.4%
Output Ripple	115 VAC	5 volts and 80 amps	P.A.R.D. 50 mV P-P
Efficiency	115 VAC	5 volts and 80 amps	73%
Line Inrush Current	115 VAC	5 volts and 80 amps	24 amps peak

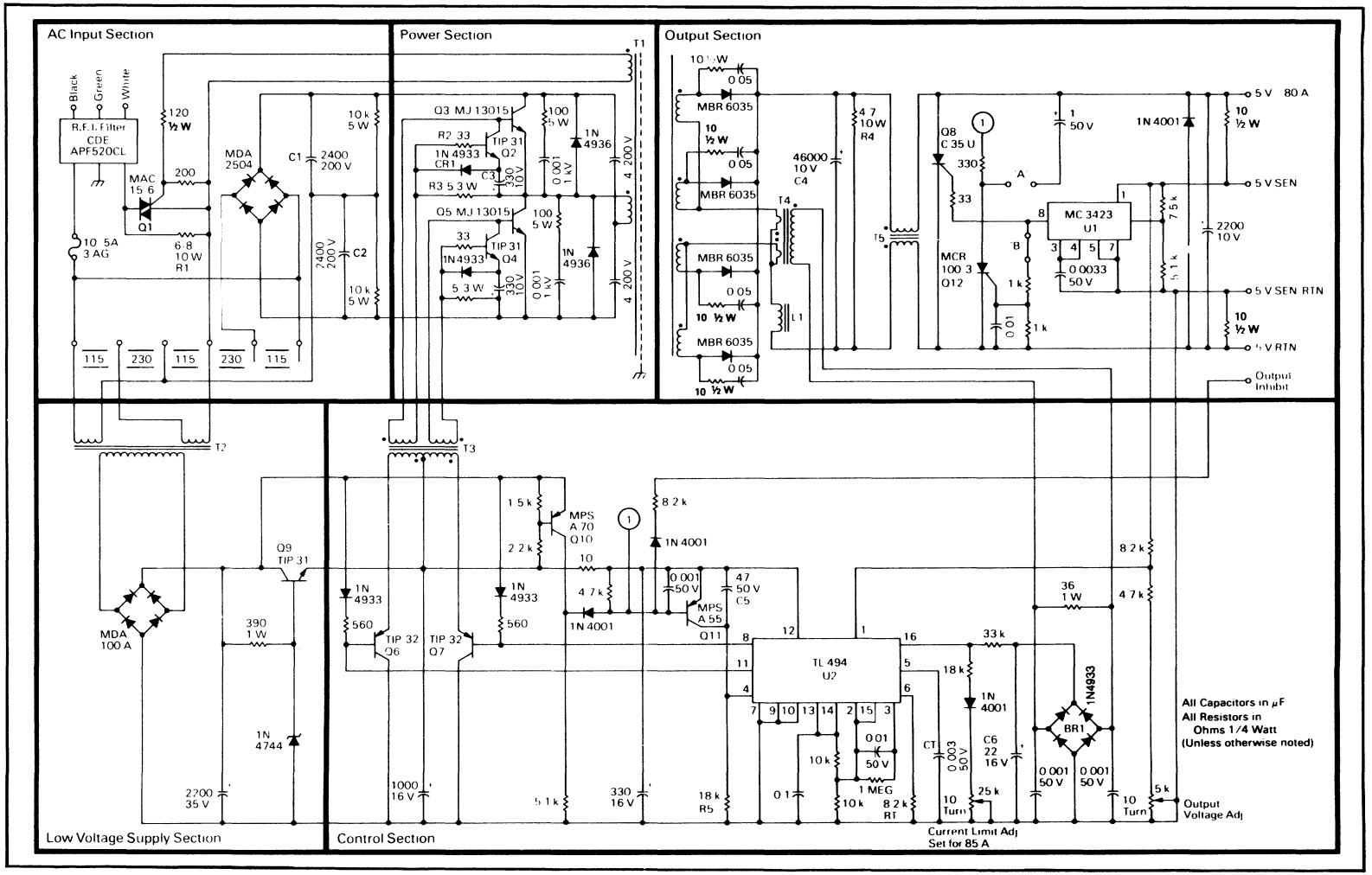


Figure 13-58. 400 Watt SWITCHMODE Power Supply

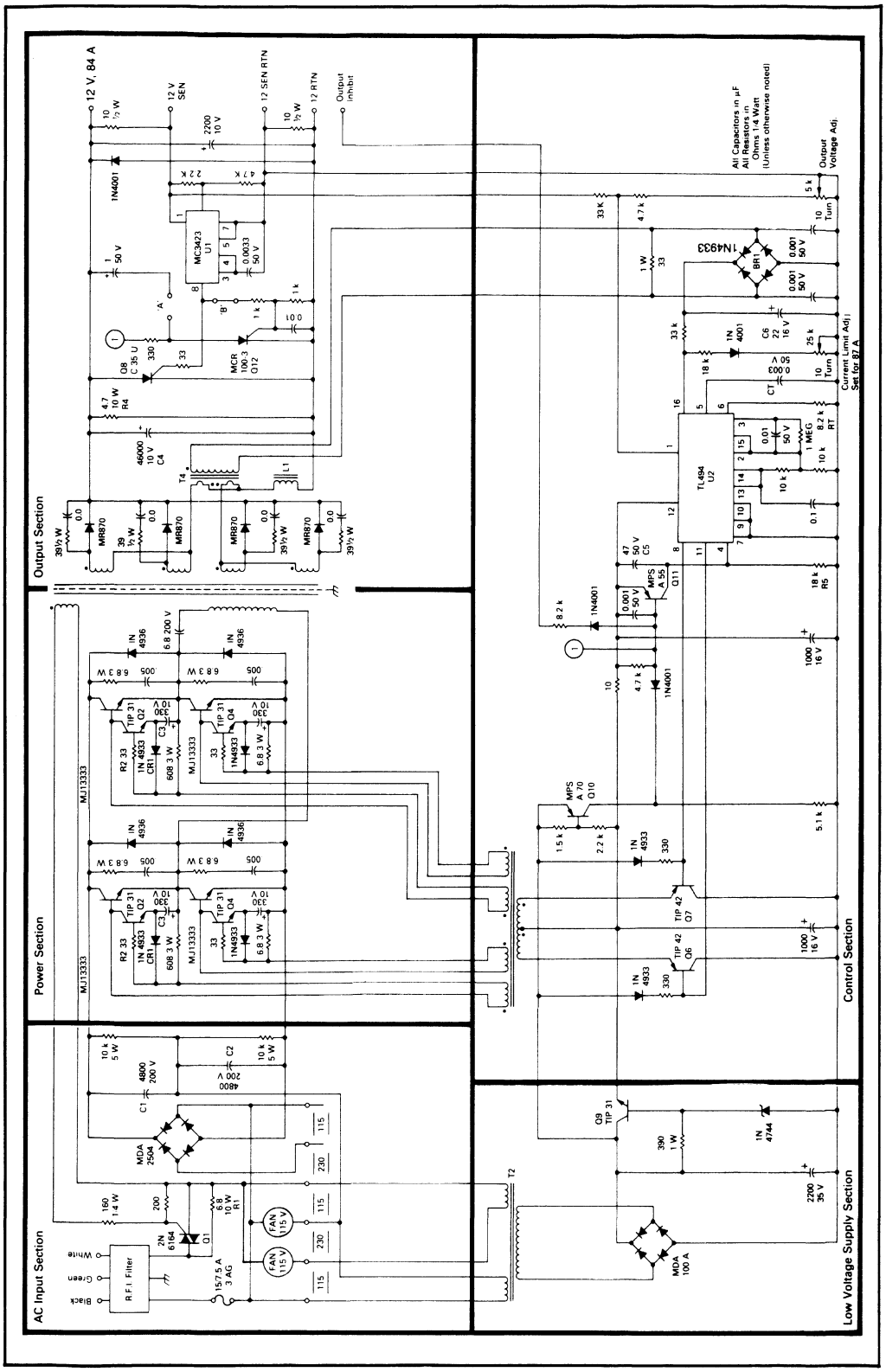


Figure 13-59. 1000 Watt SWITCHMODE Power Supply

2. Power Section

The high frequency output transformer is driven in a half-bridge configuration by transistors Q3 and Q5. Each transistor is protected from inductive turn-off voltage transients by an R-C snubber and a fast recovery clamp rectifier. Transistors Q2 and Q4 provide turn-off drive to Q3 and Q5, respectively. In order to describe the operation of Q2, consider that Q6 and Q3 are turned on. Energy is coupled from the primary to the secondary of T3, forward biasing the base-emitter of Q3, and charging C3 through CR1. Resistor R3 provides a dc path for the 'on' drive after C3 is fully charged. Note that the emitter-base of Q2 is reverse biased during this time. Turn-off drive to Q3 commences during the dead-time period, when both Q6 and Q7 are off. During this time, capacitor C3 will forward bias the base-emitter of Q2 through R3 and R2 causing it to turn-on. The base-emitter of Q3 will now be reverse biased by the charge stored in C3 coupled through the collector-emitter of Q2.

TABLE 13-3

Transformer Data for 400 Watt SWITCHMODE Power Supply

T1	Core:	Ferroxcube EC 70-3C8, 0.002" gap in each leg.	
	Bobbin:	Ferroxcube 70 PTB.	
	Windings:	Primary (Q3, Q5):	50 turns total, #17 AWG Split wound about secondary.
		Primary (Q1):	4 turns, #17 AWG.
		Secondary, 4 each:	3 turns, #14 AWG Quad Filar wound.
		Shield, 2 each:	Made from soft allow copper 0.002" thick.
T2	Core:	Allegheny Ludlum EI-75-M6, 29 gauge.	
	Bobbin:	Bobbin Cosmo EI75.	
	Windings:	Primary, 2 each:	1000 turns, #36 AWG.
		Secondary:	200 turns, #24 AWG.
T3	Core:	Ferroxcube 846T250-3C8.	
	Windings:	Primary, 2 each:	30 turns, #30 AWG Bifilar wound.
		Secondary, 4 each:	12 turns, #20 AWG Bifilar wound.
T4	Core:	Magnetics Inc. 55059-A2	
	Windings:	Primary, 2 each:	1 turn, #14 AWG Quad Filar wound. Taken from secondary to T1.
		Secondary:	500 turns, #30 AWG.
T5	Core:	Magnetics Inc. 55071-A2	
	Windings:	Primary:	4 turns, #16 AWG Hex Filar wound.
		Secondary:	4 turns, #16 AWG Hex Filar wound.
L1	Core:	TDK H7C2DR56 x 35	
	Winding:	5 turns, soft alloy copper strap, 0.9" wide x 0.020" thick, 6.0 μH.	

3. Output Section

The ac voltage present at the secondaries of T1 is rectified by four MBR6035 Schottky devices connected in a full wave center tapped configuration. Each device is protected from excessive switching voltage spikes by an R-C snubber, and output current sharing is aided by having separate secondary windings. Output current limit protection is achieved by incorporating a current sense transformer T4. The out-of-phase secondary halves of T1 are cross connected through the core of T4, forming a 1-turn primary. The 50 kHz output is filtered by inductor L1, and capacitor C4. Resistor R4 is used to guarantee that the power supply will have a minimum output load current of 1.0 ampere. This prevents the output transistors Q3 and/or Q5 from cycle skipping, as the required on-time to maintain regulation into an open circuit load is less than that of the devices' storage time. Transformer T5 is used to reduce output switching spikes by providing common mode noise rejection, and its use is optional.

The MC3423, U1, is used to sense an overvoltage condition at the output, and will trigger the crowbar S.C.R., Q8. The trip voltage is centered at 6.4 V with a programmed delay of 40 μs. In the event that a fault condition has caused the crowbar to fire, a signal is sent to the control section via jumper 'A' or 'B.' This signal is needed to shut down the output, which will prevent the crowbar

TABLE 13-4

Transformer Data for 1,000 Watt Switching Power Supply

T1	Core:	Ferroxcube EC70-3C8, 0.002" gap in each leg.	
	Bobbin:	Ferroxcube 70 PTB.	
	Windings:	Primary (Q3, Q5):	44 turns total, #18 AWG Bifilar Split wound about secondary.
		Primary (Q1):	3 turns, #18 AWG.
		Secondary, 4 each:	4 turns, #16 AWG Septe Filar wound.
		Shield, 2 each:	Made from soft alloy copper 0.002" thick.
T2	Core:	Allegheny Ludlum EI-75-M6, 29 gauge.	
	Bobbin:	Bobbin Cosmo EI75.	
	Windings:	Primary, 2 each:	1000 turns, #36 AWG.
		Secondary:	200 turns, #24 AWG.
T3	Core:	Ferroxcube 846 T250-3C8.	
	Windings:	Primary, 2 each:	30 turns, #30 AWG Bifilar wound.
		Secondary, 4 each:	12 turns, #20 AWG Bifilar wound.
T4	Core:	Magnetics Inc. 55071-A2	
	Windings:	Primary, 2 each:	1 turn, #14 AWG Quad Filar wound. Taken from secondary to T1.
		Secondary:	500 turns, #30 AWG.
L1	Core:	TDK H7C2 DR 56 x 35	5 turns, soft alloy copper strap, 0.9" wide x 0.020" thick, 6.0 μH
	Winding:		

S.C.R. from destruction due to over dissipation. Automatic over voltage reset is achieved by connecting jumper 'A.' The control section will cycle the power supply output every 2 seconds until the fault has cleared. If jumper 'B' is connected, S.C.R. Q12 will inhibit the output until the ac line is disconnected.

4. Low Voltage Supply Section

A low current internal power supply is used to keep the control circuitry active and independent from external loading of the output section. Transformer T2, Q9 and CR2 form a simple 14.3 V series pass regulator.

5. Control Section

The TL494 provides the pulse-width modulation control for the power supply. The minimum output dead-time is set to approximately 4% by grounding Pin 4 through R5. The soft start is controlled by C5 and R5. Transistor Q11 is used to discharge C5 and to inhibit the operation of the power supply if a low ac line voltage condition is sensed indirectly by Q10, or the output inhibit line is grounded.

Error amplifiers 1 and 2 are used for output voltage and current-level sensing, respectively. The inverting inputs of both amplifiers are connected together to a 2.5 V reference derived from Pin 14. By connecting the two inputs together, only one R-C feedback network is needed to set the voltage gain and roll-off characteristics for both amplifiers. Remote output voltage sensing capability is provided, and the supply will compensate for a combined total of 0.5 V drop in the power busses to the load. The secondary of the output current sense transformer T4, is terminated into 36 Ω and peak detected by BR1 and C6. The current limit adjust is set for a maximum output current of 85 amperes.

The oscillator frequency is set to 50 kHz by the timing components R_T and C_T. This results in a 25 kHz two phase output drive signal, when the output mode (Pin 13) is connected to the reference output (Pin 14).

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Mallory Capacitor Co.
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(317) 856-3731

United Chemi-Con
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Rosemont, IL 60018
(312) 696-2000

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Burbank, CA
(213) 849-2481

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Dallas, Texas 75234
(214) 243-4321

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Coilcraft, Inc.
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Cary, IL 60013
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Pulse Engineering
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San Diego, CA 92112
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Saugerties, NY 12477
(914) 246-2811

Magnetics Inc.
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Butler, PA 16001
(412) 282-8282

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SECTION 14
POWER SUPPLY SUPERVISORY AND PROTECTION CONSIDERATIONS

The use of SCR crowbar overvoltage protection (OVP) circuits has been, for many years, a popular method of providing protection from accidental overvoltage stress for the load. In light of the recent advances in LSI circuitry, this technique has taken on added importance. It is not uncommon to have several hundred dollars worth of electronics supplied from a single low voltage supply. If this supply were to fail due to component failure or other accidental shorting of higher voltage supply busses to the low voltage bus, several hundred dollars worth of circuitry could literally go up in smoke. The small additional investment in protection circuitry can easily be justified in such applications.

A. THE CROWBAR TECHNIQUE

One of the simplest and most effective methods of obtaining overvoltage protection is to use a "crowbar" SCR placed across the equipment's dc power supply bus. As the name implies, the SCR is used much like a crowbar would be, to short the dc supply when an overvoltage condition is detected. Typical circuit configurations for this circuit are shown on Figure 14-1. This method is

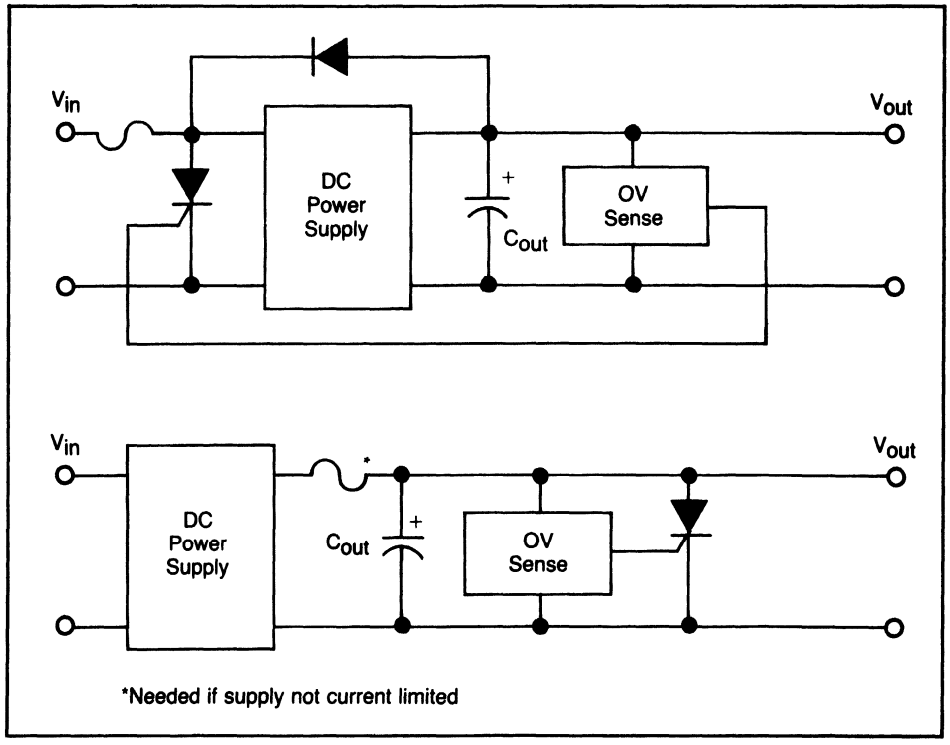


Figure 14-1. Typical Crowbar OVP Circuit Configurations

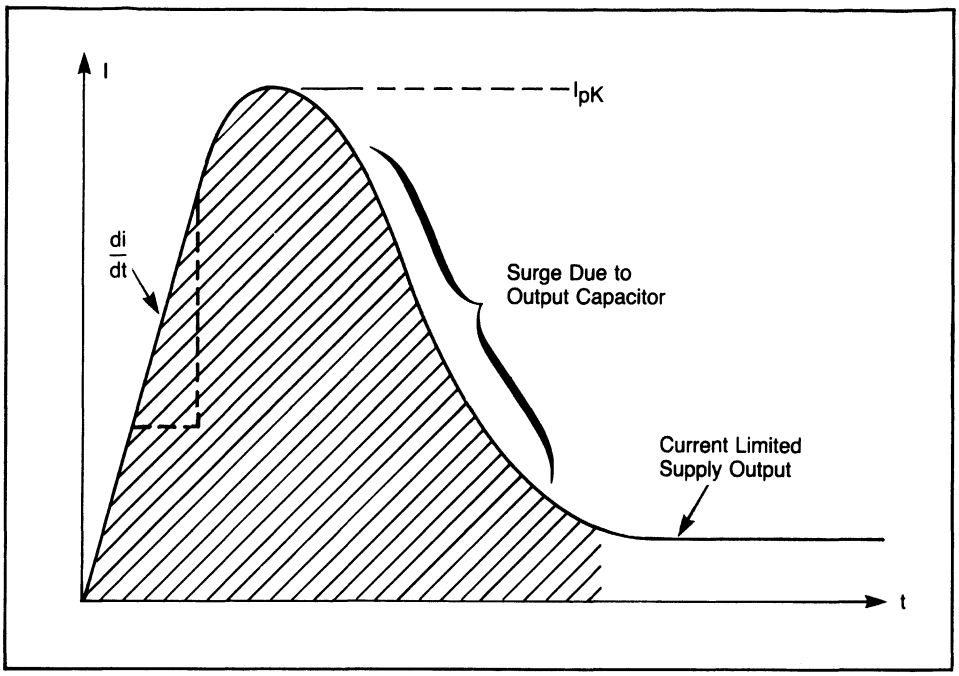


Figure 14-2. Crowbar SCR Surge Current Waveform

very effective in eliminating the destructive overvoltage condition. However, the effectiveness is lost if the OVP circuitry is not reliable.

B. SCR CONSIDERATIONS

Referring to Figure 14-1, it can easily been seen that, when activated, the crowbar SCR is subjected to a large current surge from the filter and output capacitors. This large current surge, illustrated in Figure 14-2, can cause SCR failure or degradation by any one of three mechanisms: di/dt, peak surge current, or I^2t. In many instances the designer must empirically determine the SCR and circuit elements which will result in reliable and effective OVP operation. To aid in the selection of devices for this application, Motorola has characterized several devices specifically for crowbar applications. A summary of these specifications and a selection guide for this application is shown in Table 14-1. This significantly reduces the amount of empirical testing that must be done by the designer. A good understanding of the factors that influence the SCR's di/dt and surge current capability will greatly simplify the total circuit design task.

TABLE 14-1

Crowbar SCRs

Device Type**	Peak Discharge Current*	di/dt*
MCR67	300 A	75 A/μs
MCR68	300 A	75 A/μs
MCR69	750 A	100 A/μs
MCR70	850 A	100 A/μs
MCR71	1700 A	200 A/μs

* tw = 1 μs, exponentially decaying
** All devices available with 25, 50, and 100 V ratings

1. di/dt — As the gate region of the SCR is driven on, its area of conduction takes a finite amount of time to grow, starting as a very small region and gradually spreading. Since the anode current flows through this turned-on gate region, very high current densities can occur in the gate region if high anode currents appear quickly (di/dt). This can result in immediate destruction of the SCR or gradual degradation of its forward blocking voltage capabilities, depending upon the severity of the occasion.

The value of di/dt that an SCR can safely handle is influenced by its construction and the characteristics of the gate drive signal. A center-gate-fire SCR has more di/dt capability than a corner-gate-fire type, and heavily overdriving (3 to 5 times I_{GT}) the SCR gate with a fast <1.0 μs rise time signal will maximize its di/dt capability. A typical maximum di/dt in phase control SCRs of less than 50 A rms rating might be 200 A/μs, assuming a gate current of five times I_{GT} and <1.0 μs rise time. If having done this, a di/dt problem still exists, the designer can also decrease the di/dt of the current saveform by adding inductance in series with the SCR, as shown in Figure 14-3. Of course, this reduces the circuit's ability to rapidly reduce the dc bus voltage, and a tradeoff must be made between speedy voltage reduction and di/dt.

2. Surge Current — If the peak current and/or the duration of the surge is excessive, immediate destruction due to device overheating will result. The surge capability of the SCR is directly proportional to its die area. If the surge current cannot be reduced (by adding series resistance — see Figure 14-3) to a safe level which is consistent with the system's requirements for speedy bus voltage reduction, the designer must use a higher current SCR. This may result in the average current capability of the SCR exceeding the steady state current requirements imposed by the dc power supply.

(For additional information on SCRs in crowbar applications refer to "Characterizing the SCR for Crowbar Applications," Al Pshaenich, Motorola AN-789).

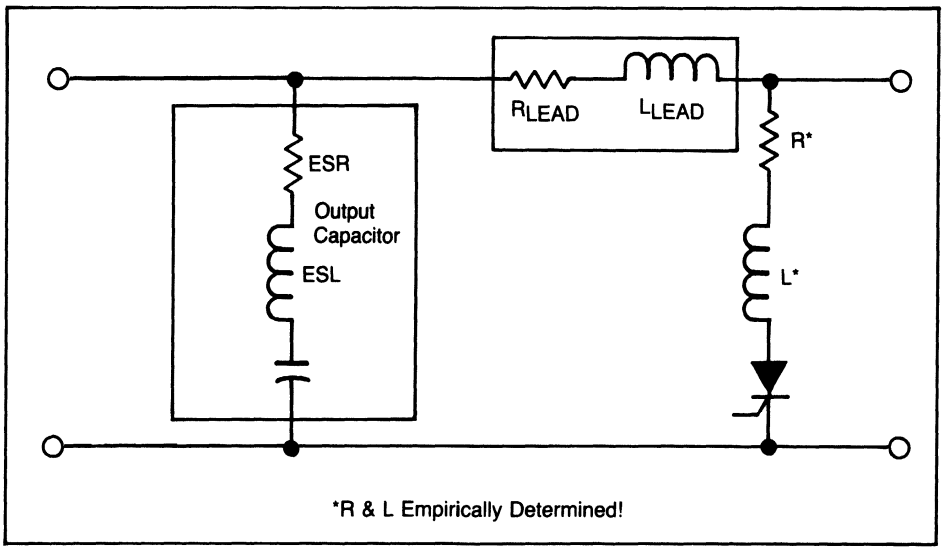


Figure 14-3. Circuit Elements Affecting SCR Surge & dI/dt

C. THE SENSE AND DRIVE CIRCUIT

In order to maximize the crowbar SCR's di/dt capability, it should receive a fast rise time high-amplitude gate-drive signal. This must be one of the primary factors considered when selecting the sensing and drive circuitry. Also important is the sense circuitry's noise immunity.

Noise immunity can be a major factor in the selection of the sense circuitry employed. If the sensing circuit has low immunity and is operated in a noisy environment, nuisance tripping of the OVP circuit can occur on short localized noise spikes, which would not normally damage the load. This results in excessive system down time. There are several types of sense circuits presently being used in OVP applications. These can be classified into three types: zener, discrete, and "723."

1. The Zener Sense Circuit — Figure 14-4 shows the use of a zener to trigger the crowbar SCR. This method is NOT recommended since it provides very poor gate drive and greatly decreases the SCR's di/dt handling capability, especially since the SCR steals its own very necessary gate drive as it turns on. Additionally, this method does not allow the trip point to be adjusted except by zener replacement.

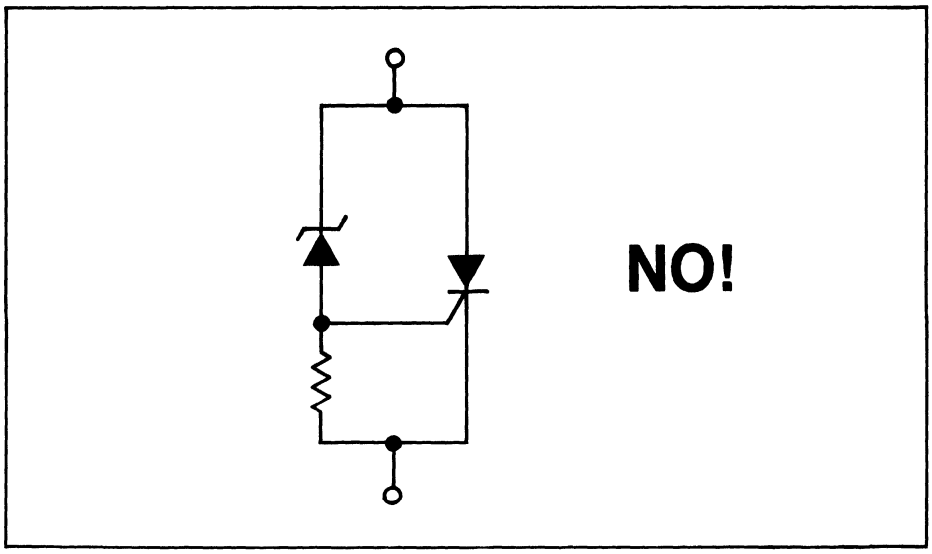


Figure 14-4. The Zener Sense Circuit

2. The Discrete Sense Circuit — A technique which can provide adequate gate drive and an adjustable, low temperature coefficient trip point is shown in Figure 14-5. While overcoming the disadvantages of the zener sense circuit, this technique requires many components and is more costly. In addition, this method is not particularly noise immune and often suffers from nuisance tripping.

3. The "723" Sense Circuit — By using an integrated circuit voltage regulator, such as the industry standard "723" type, a considerable reduction in component count can be achieved. This is illustrated in Figure 14-6. Unfortunately, this technique is not noise immune, and suffers an additional disadvantage in that it must be operated at voltages above 9.5 volts.

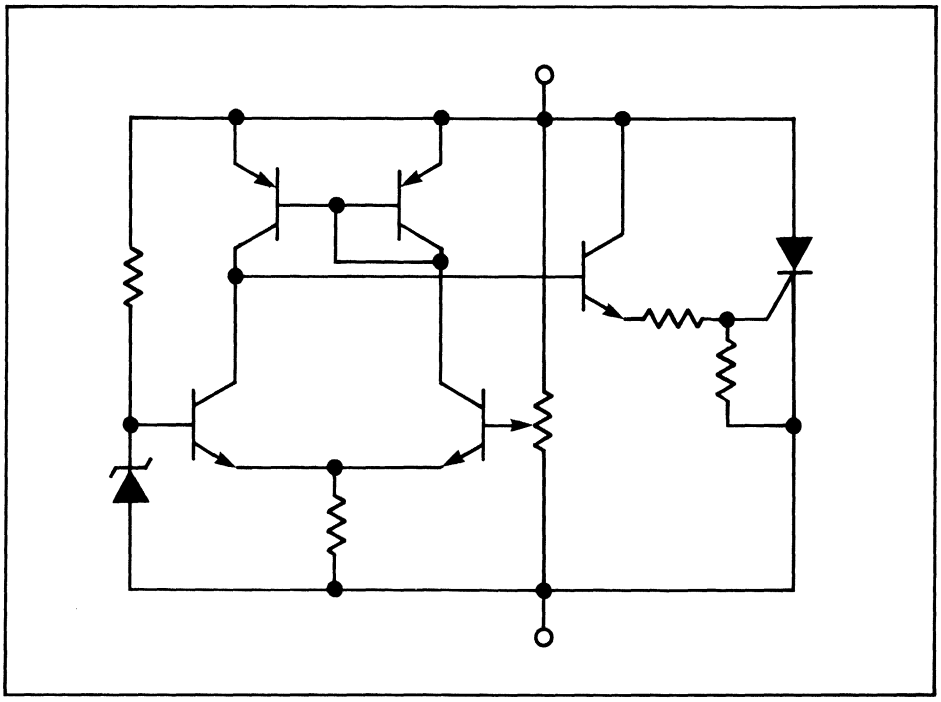


Figure 14-5. The Discrete Sense Circuit

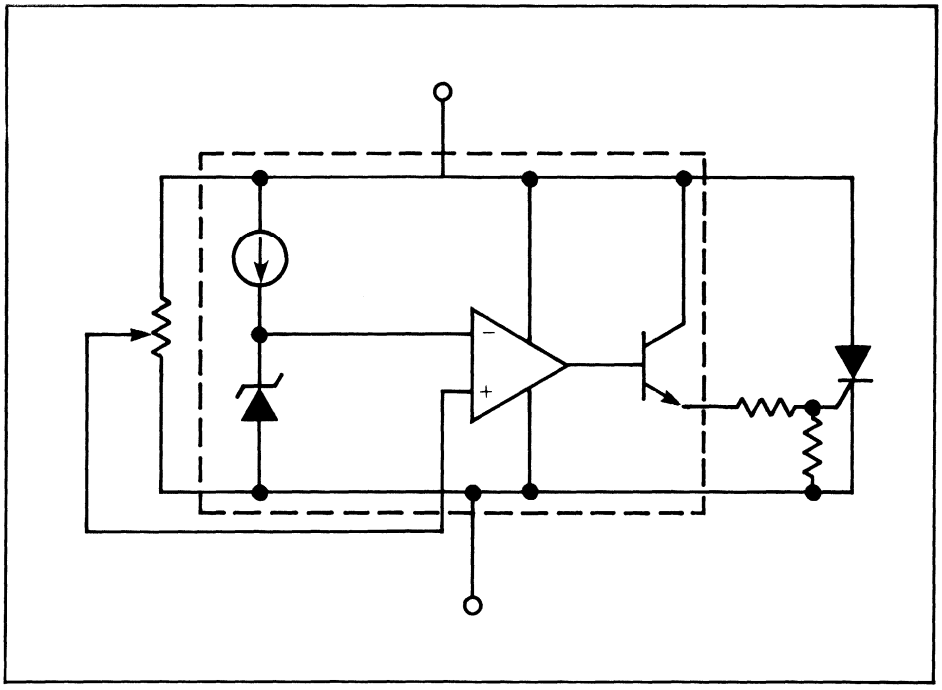


Figure 14-6. The "723" Sense Circuit

4. The MC3423 — To fill the need for a low cost, low complexity method of implementing crowbar overvoltage protection which does not suffer the disadvantages of previous techniques, an IC has been developed for use as an OVP sense and drive circuit, the MC3423.

The MC3423 was designed to provide output currents of up to 300 mA with a 400 mA/μs rise time in order to maximize the di/dt capabilities of the crowbar SCR. In addition, its features include:

1. Operation off 4.5 V to 40 V supply voltages.
2. Adustable, low temperature coefficient trip point.
3. Adjustable minimum overvoltage duration before actuation to reduce nuisance tripping in noisy environments.
4. Remote activation input.
5. Indication output.

5. Block Diagram — The block diagram of the MC3423 is shown in Figure 14-7. It consists of a stable 2.6 V reference, two comparators and a high current output. This output, together with the indication output transistor, is activated either by a voltage greater than 2.6 V on Pin 3 or by a TTL/5 volt CMOS high logic level on the remote activation input, Pin 5.

The circuit also has a comparator-controlled current source which can be used in conjunction with and external timing capacitor to set a minimum overvoltage duration (0.5 μs to 1.0 ms) before actuation occurs. This feature allows the OVP circuit to operate in noisy environments without nuisance tripping.

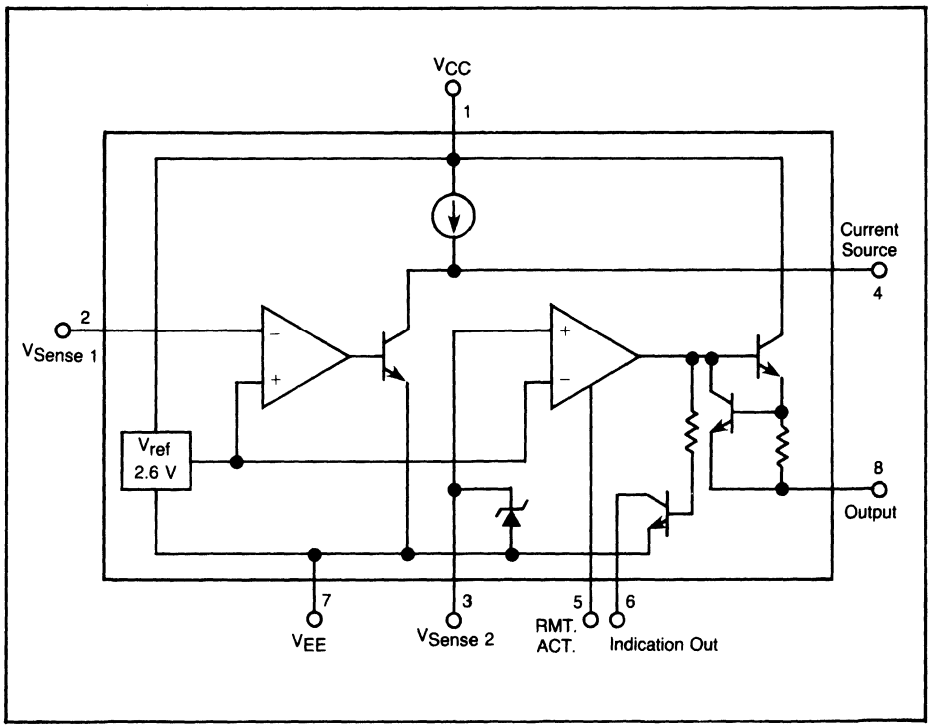


Figure 14-7. MC3423 Block Diagram

6. Basic Circuit Configuration — The basic circuit configuration of the MC3423 OVP is shown in Figure 14-8. In this circuit the voltage sensing inputs of both the internal amplifiers are tied together for sensing the overvoltage condition. The shortest possible propagation delay is thus obtained. The threshold or trip voltage at which the MC3423 will trigger and supply gate drive to the crowbar SCR, Q1, is determined by the selection of R1 and R2. Their values can be determined by the equations given in Figure 14-8 or by the graph shown in Figure 14-9. The switch, S1, shown in Figure 14-8 may be used to reset the SCR crowbar. Otherwise, the power supply, across which the SCR is connected, must be shut down to reset the crowbar. If a non current-limited supply is used a fuse or circuit breaker, F1, should be used to protect the SCR and/or the load.

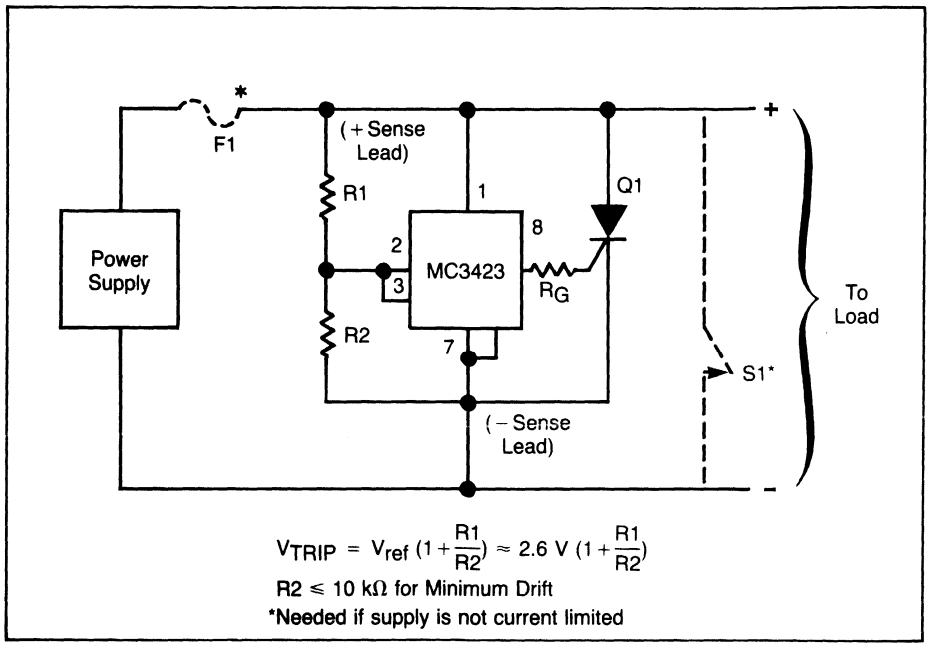


Figure 14-8. MC3423 Basic Circuit Configuration

7. MC3423 Programmable Configuration — In many instances, MC3423 OVP will be used in a noisy environment. To prevent false tripping of the OVP circuit by noise which would not normally harm the load, MC3423 has a programmable delay feature. To implement this feature, the circuit configuration of Figure 14-10 is used.

Here a capacitor is connected from Pin 3 and Pin 4 to V_{EE}. The value of this capacitor determines the minimum duration of the overvoltage condition (t_D) which is necessary to trip the OVP. The value of C_D can be found from Figure 14-11. The circuit operates in the following manner: when V_{CC} rises above the trip point set by R1 and R2, the internal current source begins charging the capacitor, C_D, connected to pins 3 and 4. If the overvoltage condition remains present long enough for the capacitor voltage, V_{CD} to reach V_{ref}, the ouput is activated. If the overvoltage condition disappears before this occurs, the capacitor is discharged at a rate 10 times faster than the charging rate, resetting the timing feature until the next over-voltage condition occurs.

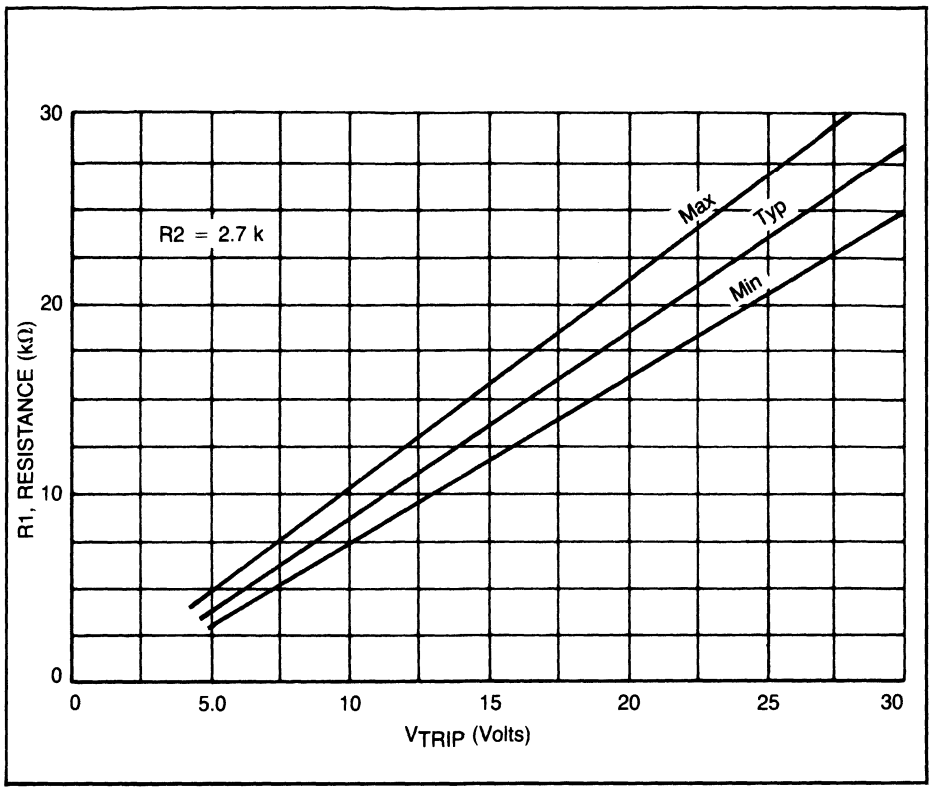


Figure 14-9. R1 versus Trip Voltage for The MC3423 OVP

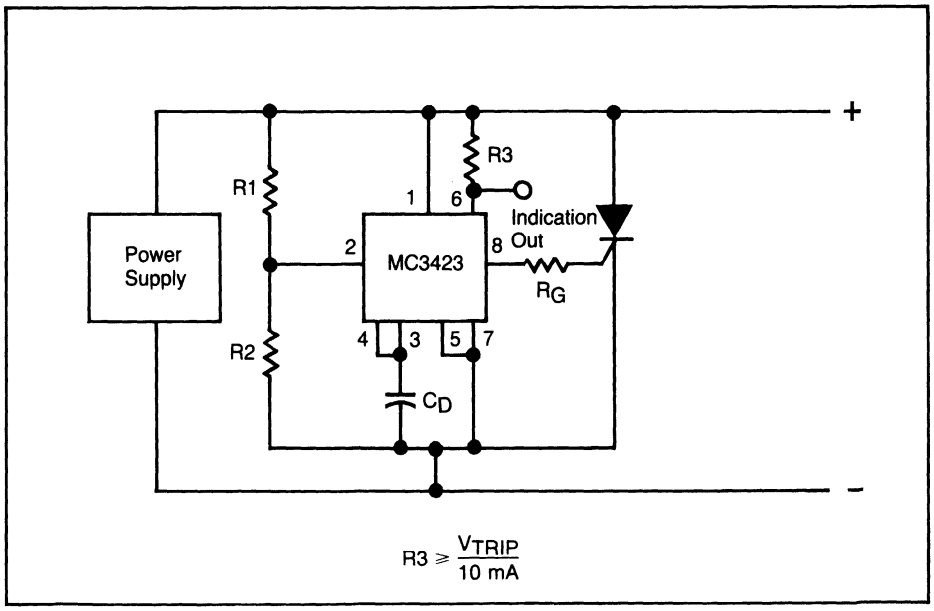


Figure 14-10. MC3423 Configuration for Programmable Minimum Duration of Overvoltage Condition before Tripping

8. Indication Output — An additional output for use as an indicator of OVP activation is provided by the MC3423. This output (Pin 6) is an open collector transistor which saturates when the MC3423 OVP is activated. It will remain in a saturated state until the SCR crowbar pulls the supply voltage, V_{CC}, below 4.5 V as in Figure 14-10. This output can be used to clock an edge triggered flop-flop whose output inhibits or shuts down the power supply when the OVP trips. This reduces or eliminates the heatsinking requirements for the crowbar SCR.

9. Remote Activation Input — Another feature of the MC3423 is its Remote Activation Input, Pin 5. If the voltage on this CMOS/TTL compatible input is held below 0.7 V, the MC3423 operates normally. However, if it is raised to a voltage above 2.0 V, the OVP output is activated independent of whether or not an overvoltage condition is present.

This feature can be used to accomplish an orderly and sequenced shutdown of system power supplies during a system fault condition. In addition, the Indication Output of one MC3423 can be used to activate another MC3423, if a single transistor inverter is used to interface the former's Indication Output to the latter's Remote Activation Input.

D. MC3425

In addition to the MC3423 a second IC, the MC3425 has been developed. Similar in many respects to the MC3423, the MC3425 is a power supply supervisory circuit containing all the necessary functions required to monitor over-and under-voltage fault conditions. The block diagram is shown below in Figure 14-12. The Over-Voltage (O.V.) and Under-Voltage (U.V.) Input Comparators

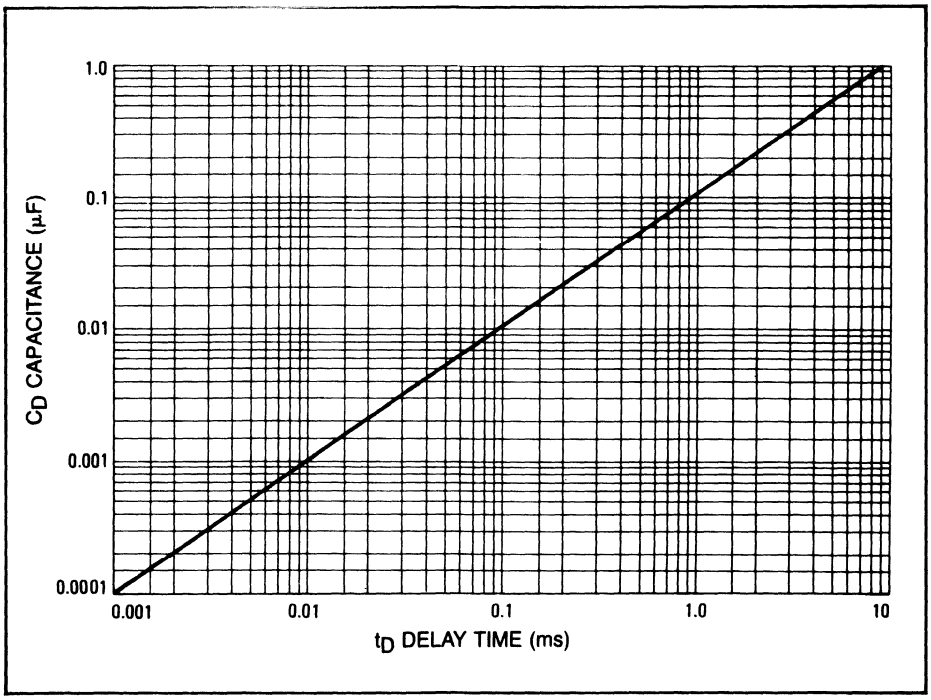


Figure 14-11. C_D versus Minimum Overvoltage Duration, t_D for The MC3423 OVP

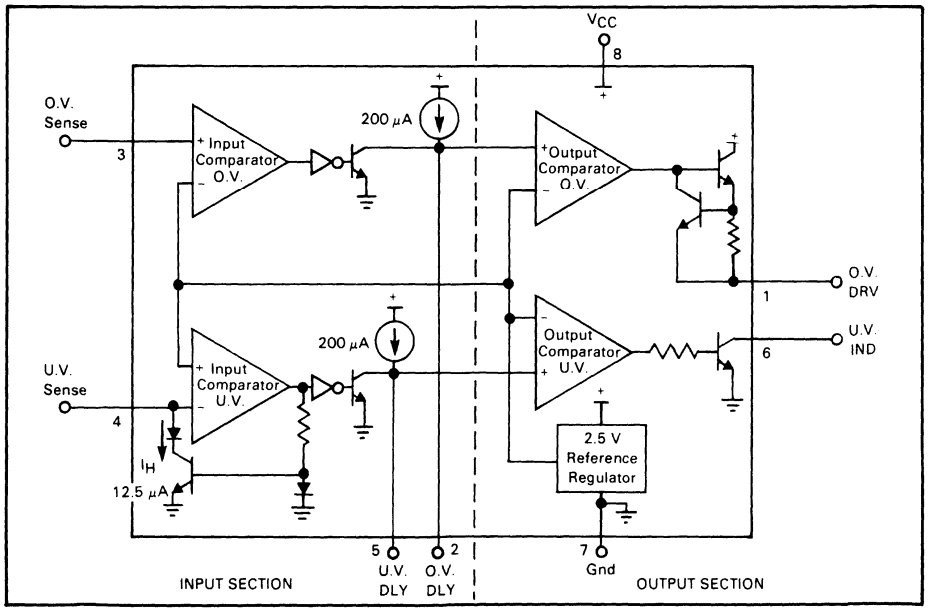
are both referenced to an internal 2.5 V regulator. The U.V. Input Comparator has a feedback activated 12.5 μA current sink (I_H) which is used for programming the input hysteresis voltage (V_H). The source resistance feeding this input (R_H) determines the amount of hysteresis voltage by $V_H = I_H R_H = 12.5 \times 10^{-6} R_H$.

Separate Delay pins (O.V. DLY, U.V. DLY) are provided for each channel to independently delay the Drive and Indicator outputs, thus providing greater input noise immunity. The two Delay pins are essentially the outputs of the respective input comparators, and provide a constant current source, $I_{DLY(source)}$, of typically 200 μA when the non-inverting input voltage is greater than the inverting input level. A capacitor connected from these Delay pins to ground, will establish a predictable delay time (t_{DLY}) for the Drive and Indicator outputs. The Delay pins are internally connected to the non-inverting inputs of the O.V. and U.V. Output Comparators, which are referenced to the internal 2.5 V regulator. Therefore, delay time (t_{DLY}) is based on the constant current source, $I_{DLY(source)}$, charging the external delay capacitor (C_{DLY}) to 2.5 volts.

$$t_{DLY} = \frac{V_{ref}\, C_{DLY}}{I_{DLY(source)}} = \frac{2.5\, C_{DLY}}{200\ \mu A} = 12500\, C_{DLY}$$

Figure 14-13 provides C_{DLY} values for a wide range of time delays. The Delay pins are pulled low when the respective input comparator's non-inverting input is less than the inverting input. The sink current, $I_{DLY(sink)}$, capability of the Delay pins is $\geq$1.8 mA and is much greater than the typical 200 μA source current, thus enabling a relatively fast delay capacitor discharge time.

The Over-Voltage Drive Output is a current-limited emitter-follower capable of sourcing 300 mA at a turn-on slew rate of 2.0 A/μs, ideal for driving "Crowbar" SCR's. The Under-Voltage Indicator Output is an open-collector, NPN transistor, capable of sinking 30 mA to provide sufficient drive for LED's, small



Note: All voltages and currents are nominal.

Figure 14-12. Block Diagram

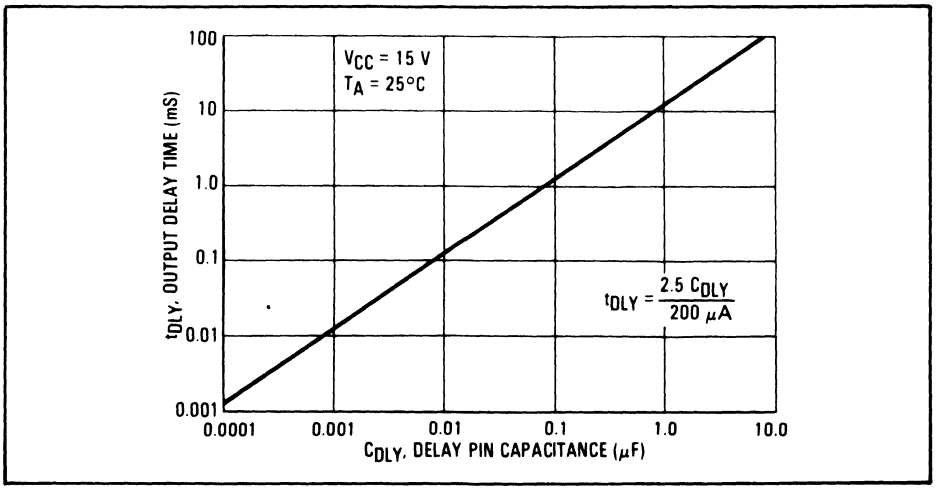


Figure 14-13. Output Delay Time versus Delay Capacitance

relays or shut-down circuitry. These current capabilities apply to both channels operating simultaneously, providing device power dissipation limits are not exceeded. The MC3425 has an internal 2.5 V bandgap reference regulator with an accuracy of ±4.0% for the basic devices.

REFERENCES

1. "Characterizing the SCR for Crowbar Applications," Al Pshaenich, Motorola AN-789.

2. "Semiconductor Considerations for DC Power Supply SCR Crowbar Circuits," Henry Wurzburg, Third National Sold-State Power Conversion Conference, June 25, 1976.

3. "Is a Crowbar Enough?" Willis C. Pierce Jr., Hewlett-Packard, Electronic Design 20, Sept. 27, 1974.

4. "Transient Thermal Response-General Data and Its Use," Bill Roehr and Brice Shiner, Motorola AN-569.

SECTION 15
HEATSINKING

A. THE THERMAL EQUATION

A necessary and primary requirement for the safe operation of any semiconductor device, whether it be an IC or a transistor, is that its junction temperature be kept below the specified maximum value given on its data sheet. The operating junction temperature is given by:

$$T_j = T_A + P_D \theta_{JA} \tag{15.1}$$

where T_j = junction temperature (°C)

T_A = ambient air temperature (°C)

P_D = power dissipated by device (watts)

θ_{JA} = thermal resistance from junction to ambient air (°C/W)

The junction-to-ambient thermal resistance, θ_{JA}, in Equation (15.1) can be expressed as a sum of thermal resistances as shown below:

$$\theta_{JA} = \theta_{JC} + \theta_{CS} + \theta_{SA} \tag{15.2}$$

where θ_{JC} = junction-to-case thermal resistance

θ_{CS} = case-to-heatsink thermal resistance

θ_{SA} = heatsink-to-ambient thermal resistance

(Equation (15.2) applies only when an external heatsink is used. If no heatsink is used, θ_{JA} is equal to the device package θ_{JA} given on the data sheet.)

θ_{JC} depends on the device and its package (case) type, while θ_{SA} is a property of the heatsink and θ_{CS} depends on the type of package/heatsink interface employed. Values for θ_{JC} and θ_{SA} are found on the device and heatsink data sheets, while θ_{CS} is given in Table 15-1.

TABLE 15-1

θ_{CS} For Various Packages & Mounting Arrangements

	θ_{CS}			
	METAL-TO-METAL*		USING AN INSULATOR*	
CASE	DRY	With Heatsink Compound	With Heatsink Compound	Type
TO-204	0.5°C/W	0.1°C/W	0.36°C/W 0.28°C/W	3 mil MICA Anodized Aluminum
TO-220	1.2°C/W	1.0°C/W	1.6°C/W	2 mil MICA

*Typical values; heatsink surface should be free of oxidation, paint, and anodization

Examples showing the use of Equations 15.1 and 15.2 in thermal calculations are as follows:

Example 1: Find required heatsink θ_{SA} for an MC7805CT; given:

T_{jmax} (desired) = +125°C

T_{Amax} = +70°C

P_D = 2 watts

Mounted directly to heatsink with silicon thermal grease at interface

1. From MC7805CT data sheet, θ_{JC} = 5°C/W
2. From Table 15-1. θ_{CS} = 1.6°C/W
3. Using Equation 15.1 and 15.2, solve for θ_{SA}:

$$\theta_{SA} = \frac{(T_j - T_A)}{P_D} - \theta_{CS} - \theta_{JC}$$

$$\theta_{SA} = \frac{(125 - 70)}{2} - 5.0 - 1.6$$

$$\leq 20.9°C/W \text{ required}$$

Example 2: Find the maximum allowable T_A for an unheatsinked MC78L15CT, given:

$T_j$max (desired) = +125°C

P_D = .25 watt

1. From MC78L15CT data sheet, θ_{JA} = 200°C/W
2. Using Equation 15.1 find T_A:

$$T_A = T_j - P_D \theta_{JA}$$

$$= 125 - .25\ (200)$$

$$= +75°C$$

B. SELECTING A HEATSINK

Usually, the maximum ambient temperature, power being dissipated, the T_{jmax}, and θ_{JC} for the device being used are known. The required θ_{SA} for the heatsink is then determined using Equations 15.1 and 15.2, as in Example 1. The designer may elect to use a commercially available heatsink, or if packaging or economy demands it, design his own.

1. Commercial Heatsinks

As an aid in selecting a heatsink, a representative listing is shown in Table 15-2. This listing is by no means complete and is only included to give the designer an idea of what is available.

TABLE 15-2

Commercial Heatsink Selection Guide

No attempt has been made to provide a complete list of all heatsink manufacturers. This list is only representative.

TO-204AA (TO-3)	
θ_{SA}*(°C/W)	**Manufacturer/Series or Part Number**
0.3-1.0	Thermalloy — 6441, 6443, 6450, 6470, 6560, 6590, 6660, 6690
1.0-3.0	Wakefield — 641 Thermalloy — 6123, 6135, 6169, 6306, 6401, 6403, 6421, 6423, 6427, 6442, 6463, 6500
3.0-5.0	Wakefield — 621, 623 Thermalloy — 6606, 6129, 6141, 6303 IERC — HP Staver — V3-3-2
5.0-7.0	Wakefield — 690 Thermalloy — 6002, 6003, 6004, 6005, 6052, 6053, 6054, 6176, 6301 IERC — LB Staver — V3-5-2
7.0-10.0	Wakefield — 672 Thermalloy — 6001, 6016, 6051, 6105, 6601 IERC — LA, uP Staver — V1-3, V1-5, V3-3, V3-5, V3-7
10.0-25.0	Thermalloy — 6013, 6014, 6015, 6103, 6104, 6105, 6117

*All values are typical as given by mfgr. or as determined from characteristic curves supplied by manufacturer.

TO-205AA (TO-5)	
θ_{SA}*(°C/W)	**Manufacturer/Series or Part Number**
12.0-20.0	Wakefield — 260 Thermalloy — 1101, 1103 Staver — V3A-5
20.0-30.0	Wakefield — 209 Thermalloy — 1116, 1121, 1123, 1130, 1131, 1132, 2227, 3005 IERC — LP Staver — F5-5
30.0-50.0	Wakefield — 207 Thermalloy — 2212, 2215, 225, 2228, 2259, 2263, 2264 Staver — F5-5, F6-5
	Wakefield — 204, 205, 208 Thermalloy — 1115, 1129, 2205, 2207, 2209, 2210, 2211, 2226, 2230, 2257, 2260, 2262 Staver — F1-5, F5-5
θ_{SA}*(°C/W)	**TO-220AB**
5.0-10.0	IERC H P3 Series Staver — V3-7-225, V3-7-96
10.0-15.0	Thermalloy — 6030, 6032, 6034 Staver — V4-3-192, V-5-1
15.0-20.0	Thermalloy — 6106 Staver — V4-3-128, V6-2
20.0-30.0	Wakefield — 295 Thermalloy — 6025, 6107

*All values are typical as given by mfgr. or as determined from characteristic curves supplied by manufacturer.

TO-226AA (TO-92)	
θ_{SA}*(°C/W)	Manufacturer/Series or Part Number
46	Staver F5-7A, F5-8
50	IERC RUR
57	Staver F5-7D
65	IERC RU
72	Staver F1-8, F2-7
80-90	Wakefield 292
85	Thermalloy 2224
DUAL-INLINE-PIN ICS	
20	Thermalloy — 6007
30	Thermalloy — 6010
32	Thermalloy — 6011
34	Thermalloy — 6012
45	IERC — LIC
60	Wakefield — 650, 651

*All values are typical as given by mfgr. or as determined from characteristic curves supplied by manufacturer.

Staver Co., Inc.: 41-51 N. Saxon Ave., Bay Shore, NY 11706
IERC: 135 W. Magnolia Blvd., Burbank, CA 91502
Thermalloy: P.O. Box 34829, 2021 W. Valley View Ln. Dallas, TX
Wakefield Engin Ind: Wakefield, MA 01880

2. Custom Heat Sink Design

Custom heatsinks are usually either forced air cooled or convection cooled. The design of forced air cooled heatsinks is usually done empirically, since it is difficult to obtain accurate air flow measurements. On the other hand, convection cooled heatsinks can be designed with fairly predictable characteristics. It must be emphasized, however, that any custom heatsink design should be thoroughly tested in the actual equipment configuration to be certain of its performance. In the following sections, a design procedure for convection cooled heatsinks is given.

Obviously, the basic goal of any heatsink design is to produce a heatsink with an adequately low thermal resistance, θ_{SA}. Therefore, a means of determining θ_{SA} is necessary in the design. Unfortunately, a precise calculation method for θ_{SA} is beyond the scope of this book.* However, a first order approximation can be calculated for a convection cooled heatsink if the following conditions are met:

1. The heatsink is a flat rectangular or circular plate whose thickness is much smaller than its length or width.
2. The heatsink will not be located near other heat radiating surfaces.
3. The aspect ratio of a rectangular heatsink (length:width) is not greater than 2:1.
4. Unrestricted convective air flow.

For the above conditions, the heatsink thermal resistance can be approximated by:

$$\theta_{SA} \simeq \frac{1}{A\eta\,(F_c h_c + \epsilon H_r)}\ (°C/W) \qquad (15\text{-}3)$$

where A = area of the heatsink surface

η = heatsink effectiveness

*If greater precision is desired, or more information on heat flow and heatsinking is sought, consult the references list at the end of this section.

F_c = convective correction factor

h_c = convection heat transfer coefficient

ϵ = emissivity

H_r = normalized radiation heat transfer coefficient

The convective heat transfer coefficient, h_c, can be found from Figure 15-1. Note that it is a function of the heatsink fin temperature rise, $T_S - T_A$, and the heatsink significant dimension, L. The fin temperature rise, $T_S - T_A$, is given by:

$$T_S - T_A = \theta_{SA} P_D \tag{15.4}$$

where T_S = heatsink temperature

T_A = ambient temperature

θ_{SA} = heatsink-to-ambient thermal resistance

P_D = power dissipated

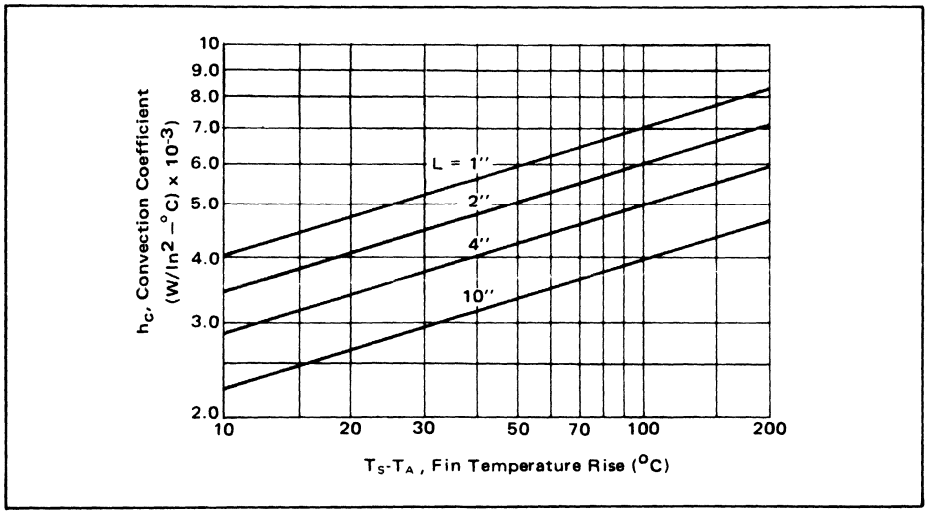


Figure 15-1. Convection Coefficient, h_C

The significant heatsink dimension, L, is dependent on the heatsink shape and mounting place and is given in Table 15-3.

The convective correction factor, F_c, is likewise dependent on shape and mounting plane of the heatsink and is also given in Table 15-3.

TABLE 15-3

Significant Dimension L and Correction Factor F_c for Convection Thermal Resistance

Surface	Significant Dimension L		Correction Factor F_c	
	Position	L	Position	F_c
Rectangular Plane	vertical	height — (max 2 ft)	Vertical Plane	1.0
	horizontal	$\frac{\text{length x width}}{\text{length + width}}$	Horizontal Plane both surfaces exposed	1.35
Circular Plane	vertical	π / 1 x diameter	top only exposed	0.9

The normalized radiation heat transfer coefficient, H_r, is dependent on the ambient temperature, T_A, and the heatsink temperature rise, $T_S - T_A$, given by Equation (15.4). H_r can be determined from Figure 15-2.

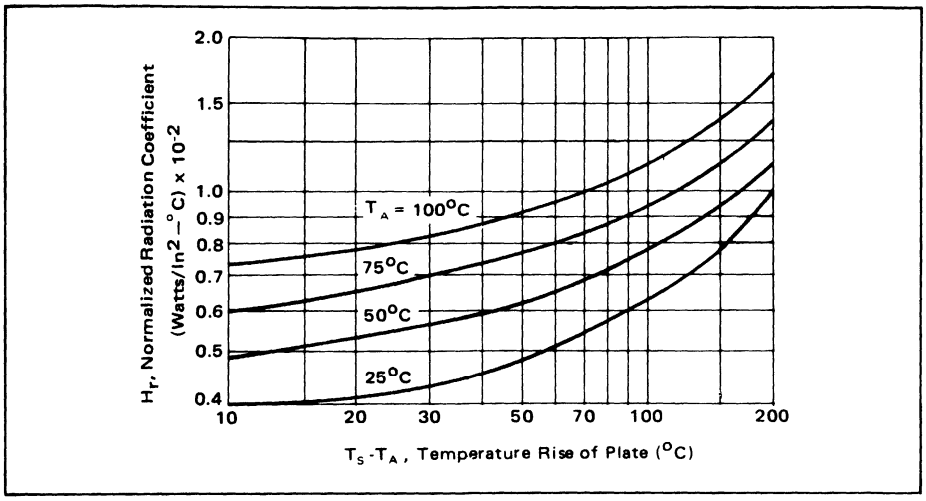


Figure 15-2. Normalized Radiation Coefficient, H_r

The emissivity, ϵ, can be found in Table 15-4 for various heatsink surfaces.

TABLE 15-4.

Typical Emissivities of Common Surfaces

Surface	Emissivity, ϵ
Aluminum, Anodized	0.7 — 0.9
Alodine on Aluminum	0.15
Aluminum, Polished	0.05
Copper, Polished	0.07
Copper, Oxidized	0.70
Rolled Sheet Steel	0.66
Air Drying Enamel (any color)	0.85 — 0.91
Oil Paints (any color)	0.92 — 0.96
Varnish	0.89 — 0.93

Finally, the heatsink efficient, η, can be found from the nomograph of Figure 15-3. Use of the nomograph is as follows:

a. Find $h_T = F_c h_c + \epsilon H_r$ from Figures 15-1, 15-2 and Tables 15-3 and 15-4, and locate this point on the nomograph.

b. Draw a line from h_T through chosen heatsink fin thickness, x, to find α.

c. Determine D for the heatsink shape as given in Figure 15-4 and draw a line from this point through α, which was found in (b), to determine η.

d. If power dissipating element is not located at heatsink's center of symmetry, multiply η by 0.7 (for vertically mounted plates only).

Note that in order to calculate θ_{SA} from Equation (15.3), it is necessary to know the heatsink size. Therefore, in order to arrive at a suitable heatsink design, a trial size is selected, its θ_{SA} evaluated, and the original size reduced or enlarged as necessary. This process is iterated until the smallest heatsink is obtained that has the required θ_{SA}. The following design example is given to illustrate this procedure:

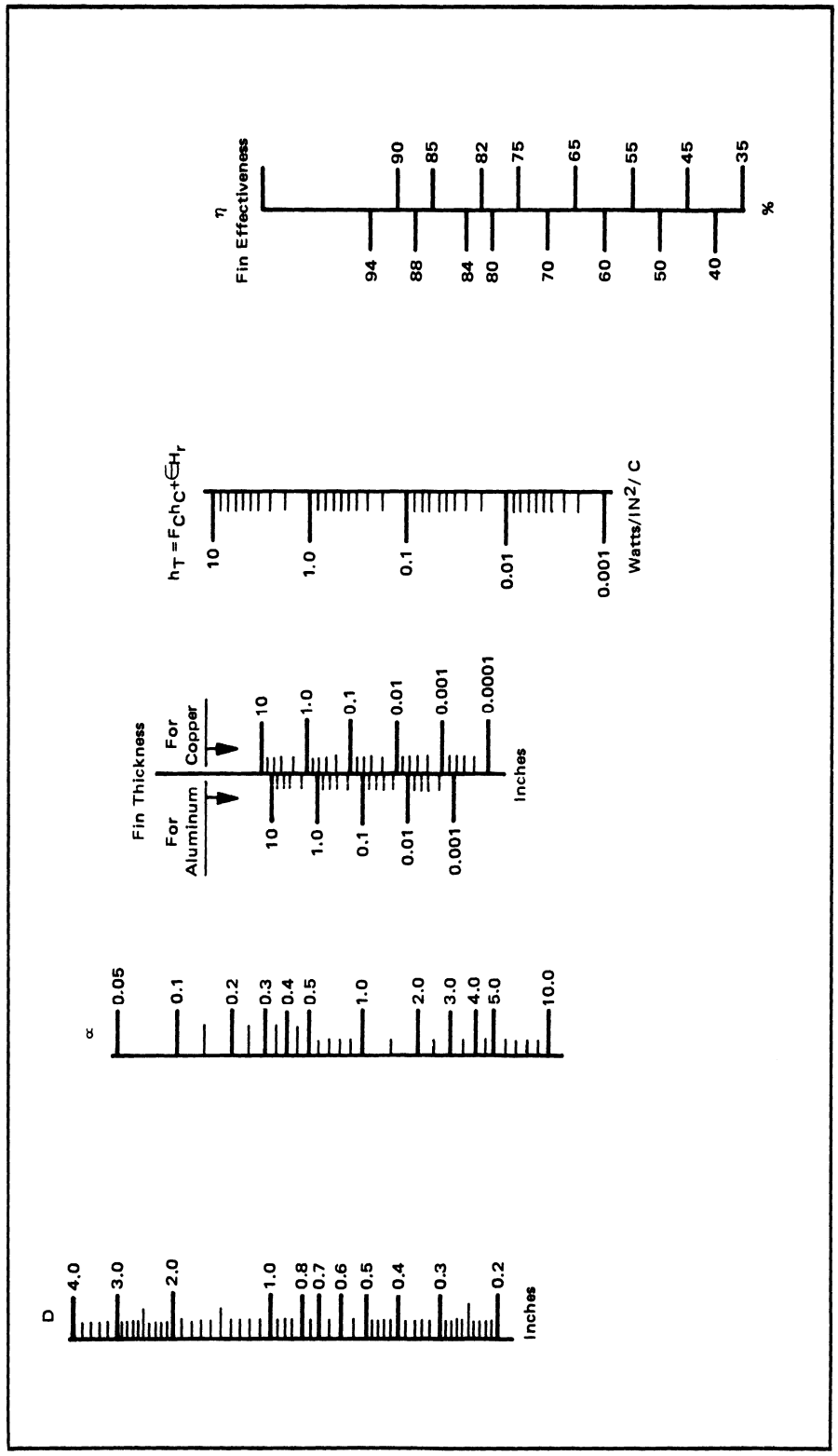


Figure 15-3. Fin Effectiveness Nomogram for Symmetrical Flat, Uniformly Thick Fins

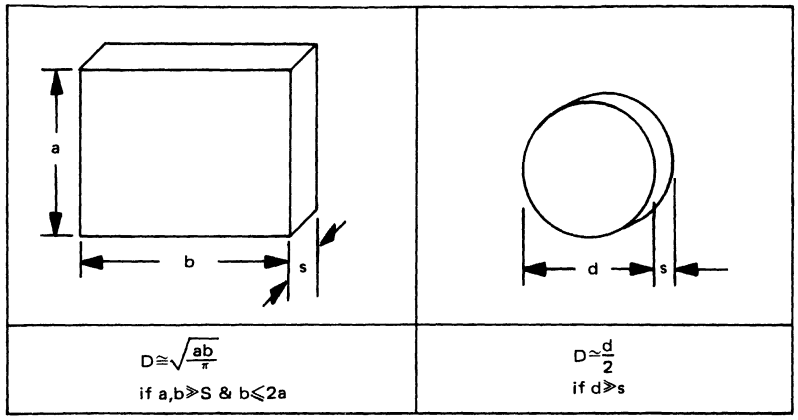


Figure 15-4. Determination of D for Use in η Nomograph of Figure 15-3

Heatsink Design Example

Design a flat rectangular heatsink for use with a horizontally mounted power device on a PC card, given the following:

1. Heatsink θ_{SA} = 25°C/W
2. Power to be dissipated, P_D = 2W
3. Maximum ambient temperature, T_A = 50°C
4. Heatsink to be constructed from ⅛″ (0.125″) thick anodized aluminum.

a. First, a trial heatsink is chosen: 2″ x 3″ (experience will simplify this selection and reduce the number of necessary iterations.)

b. The factors in Equation (15.3) are evaluated by using the Figures and Tables given.

A = 2″ x 3″ = 6 sq. in.

L = 6/5″ = 1.2 in. (from Table 15-3)

$T_S - T_A$ = 50°C (from Equation 15.4)

$h_c = 5.8 \times 10^{-3}$ W/in^2 – °C from Figure 15-1)

F_c = 0.9 (from Table 15-3)

$H_r = 6.1 \times 10^{-3}$ W/in^2 – °C (from Figure 15-2)

ϵ = 0.9 (from Table 15-4)

$h_T = F_c h_c + H_r \epsilon = 10.7 \times 10^{-3}$ w/in^2 – °C

α = 0.13 (from Figure 15-3)

D = 1.77 (from Figure 15-4)

$\eta > 0.94 \simeq 1$ (from Figure 15-3)

c. Using Equation 15.3, find θ_{SA}

$$\theta_{SA} \simeq \frac{1}{A\eta\,(F_c h_c + \epsilon H_r)} = 16.66°C/W < 25°C/W$$

d. Since 2″ x 3″ is too large, try 2″ x 2″. Following the same procedure, θ_{SA} is found to be 25°C/W, which exactly meets the design requirements.

SOIC MINIATURE IC PLASTIC PACKAGE

Thermal Information

The maximum power consumption an integrated circuit can tolerate at a given operating ambient temperature, can be found from the equation:

$$P_{(DT_A)} = \frac{T_{J(max)} - T_A}{R_{\theta JA}\ (Typ)}$$

Where: $P_{D(T_A)}$ = power dissipation allowable at a given operating ambient temperature.

$T_{J(max)}$ = Maximum operating junction temperature as listed in the maximum ratings section

T_A = Desired operating ambient temperature

$R_{\theta JA}$ (Typ) = Typical thermal resistance junction to ambient

Maximum Ratings

Rating	Symbol	Value	Unit
Operating Ambient Temperature Range	T_A	0 to +70 −40 to +85	°C °C
Operating Junction Temperature	T_J	150	°C
Storage Temperature Range	T_{stg}	−55 to +150	°C

THERMAL RESISTANCE OF SOIC PACKAGES

Measurement specimens are solder mounted on a Philips SO test board #7322-078, 80873 in still air. No auxiliary thermal conduction aids are used. As thermal resistance varies inversely with die area, a given package takes thermal resistance values between the max and min curves shown. These curves represent the smallest (2000 square mils) and largest (8000 square mils) die areas expected to be assembled in the SOIC package.

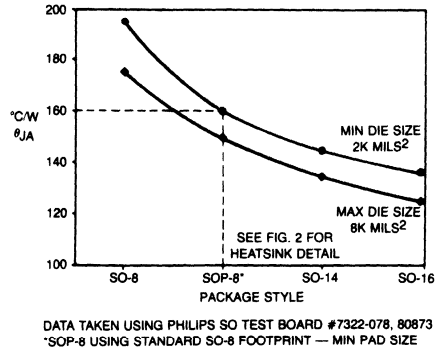


Figure 1. Thermal Resistance, Junction-to-Ambient (°C/W)

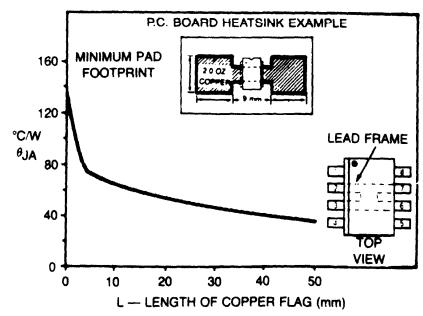
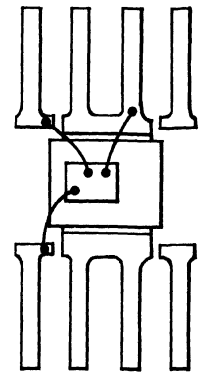


Figure 2. Thermal Resistance for SOP-8 Package Die 2K mils²

SOP-8 Packaged Devices



Three families of voltage regulators and one family of programmable precision references have been introduced in a surface mounted package which was developed by the Bipolar Analog I.C. Division. The SOP-8 package has external dimensions which are identical to the standard SO-8 surface mount device, but the center four leads of the 8-lead device are all connected to the leadframe die flag. This internal modification decreases the package thermal resistance and therefore increases its power dissipation capability. This advantage is fully realized when the package is mounted on a printed circuit board with a single pad for the four center leads. This large area of copper then acts as an external heat spreader, efficiently conducting heat away from the package.

The 100 mA output current MC78L series of positive voltage regulators (in four voltages), the 100 mA MC79L series of negative regulators (in three voltages), and the 100 mA LM317L positive adjustable voltage regulator have been introduced in the SOP-8. In addition, the TL431 family of precision voltage references (in two temperature ranges) are available in the SOP-8 package.

THERMAL RESISTANCE OF DPAK PACKAGE

The evaluation was performed using an active device (4900 square mils) mounted on 2.0 ounce copper foil epoxied to a G10 type printed circuit board. Measurements were made in still air and no auxiliary thermal conduction aids were used. The size of a square copper pad was varied, and all measurements were made with the unit mounted as shown in Figure 3. The curve shown is a plot of junction-to-air thermal resistance versus the length of the square copper pad in millimeters. This shows that when the DPAK is mounted on a 10 mm x 10 mm square pad of 2.0 ounce copper it has a thermal resistance which is comparable to a TO-220 device mounted vertically without additional heatsinking.

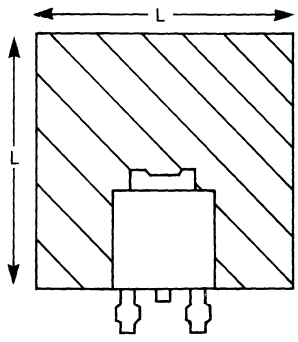


Figure 3. P.C. Board Heatsink Example

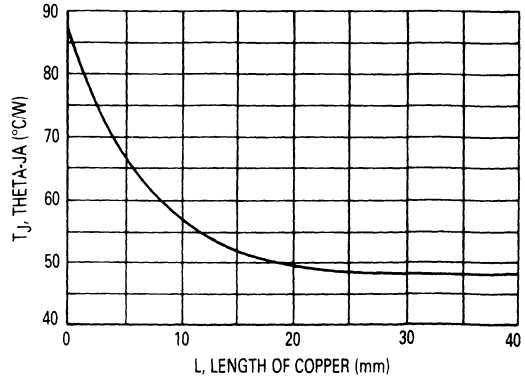


Figure 4. DPAK Thermal Evaluation

SECTION 16
QUALITY AND RELIABILITY ASSURANCE

Quality Concepts

The word **Quality** has been used to describe many things, such as fitness for use, customer satisfaction, customer enthusiasm, what the customer says quality is, etc. These descriptions convey important truths, however quality should be described in a way that precipitates immediate action. With that in mind **quality** can be described **as reduction of variability around a target, so that conformance to customer requirements/expectations can be achieved in a cost effective way.** This definition provides direction and potential for immediate action for a person desiring to improve quality. **Quality Improvement** for a task or a process can be quickly described in terms of the target, current status with respect to target (variability), reduction of variability (commitment to never ending improvement), customer requirements (who receives output, what are person's requirements/expectations) and economics (cost of nonconformance; loss function, etc.).

The definition of quality as described above can be applied to a task, process or a whole company. If we are to reap the benefits of quality and obtain a competitive advantage, quality must be applied to the whole company.

Application of quality to the whole company has come to be known by such names as **"Total Quality Control" (TQC); "Company Wide Quality Control" (CWQC); "Total Quality Excellence" (TQE); "Total Quality Involvement" (TQI).** These names attempt to convey the idea that quality is a process (a way of acting continuously) rather than a program (implying a beginning and an end). Nevertheless for this process to be successful it must be able to show measurable results.

Implementation of quality ideas, company, wide requires a quality plan showing: A philosophy (belief) of operation, measurable goals, training of individuals and methods of communicating this philosophy of operation to the whole organization.

Motorola, for example, believes that **quality** and **reliability** are the **responsibility of every person. Participative Management Program (PMP)** is the process by which problem solving and quality improvement are facilitated at all levels of the organization. **Continuous improvement** for the individual is facilitated by a broad educational program covering on-site, university and college courses. The **Motorola Training and Education Center (MTEC)** provides leadership and administers this educational effort on a company wide basis.

Another key belief is that **quality excellence** is accomplished by **people doing things right the first time** and **committed to never ending improvement.** The **Six Sigma (6σ)** challenge is designed to convey and facilitate the idea of continuous improvement at all levels.

"**Six Sigma** is the required capability level to approach the standard. The **standard** is **zero defects.** Our goal is to be Best-In-Class in product, sales and service." (For a more detailed explanation, contact your Motorola Representative for a pamphlet of the Six Sigma Challenge.)

Quick insight into Six Sigma is obtained if we realize that a Six Sigma process has variability which is one half of the variation allowed (tolerance; spread) by the customer requirements (i.e. natural variation is one half of the customer specification range for a given characteristic). When Six Sigma is achieved, virtually zero defects are observed in the output of a process/product even allowing for potential process shifts (Figure 16-1).

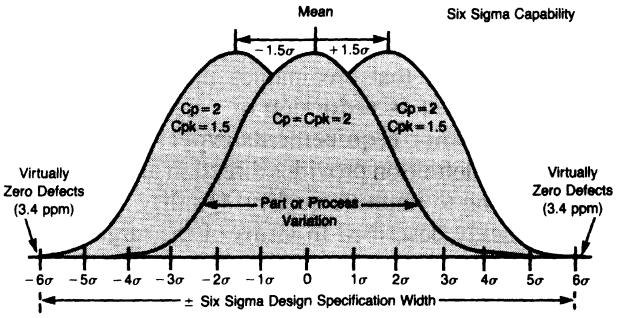


Figure 16-1. A Six Sigma Process Has Virtually Zero Defects Allowing For 1.5σ Shift

Policies, **objectives** and **five year plans** are the mechanisms for communicating the key beliefs and measurable goals to all personnel and continuously keeping them in focus. This is done at the corporate, sector, group, division, and department levels.

The Analog Division, for example, evaluates performance to the corporate goals of **10 Fold Improvement by 1989; 100 Fold Improvement by 1991** and achievement of **Six Sigma capability by 1992** by utilizing indices such as Outgoing Electrical and Visual Mechanical Quality (**AOQ**) in terms of PPM (parts per million or sometimes given in 'parts per billion'); **% of devices with zero PPB; product quality returns** (RMR); number of processes/products with specified **capability indices (cp; cpk); Six Sigma capability roadmaps; failure rates for various reliability tests** (operating life, temperature humidity bias, hast, temperature cycling, etc.); **on time delivery; customer product evaluation and failure analysis turnaround; cost of nonconformance; productivity improvement and personnel development.**

Figure 16-2 shows the improvement in electrical outgoing quality for bipolar analog products over recent years in a normalized form.

Documentation control is an important part of statistical process control. Process flow charting with documentation identified allows visualization and therefore optimization of the process. Figure 16-4 shows a portion of a flow chart for Wafer Fabrication. Control plans are an important part of Statistical Process Control, these plans identify in detail critical points where data for process control is taken, parameters measured, frequency of measurements, type of control device used, measuring equipment, responsibilities and reaction plans. Figure 16-5 shows a portion of a control plan for wafer fabrication. These flow charts and control plans exist for all product flows.

Six Sigma progress is tracked by roadmaps. A portion of a roadmap is shown for example on Figure 16-6.

On Time Delivery is of great importance, with the current emphasis on just-in-time systems. Tracking is done on an overall basis, and at the device level.

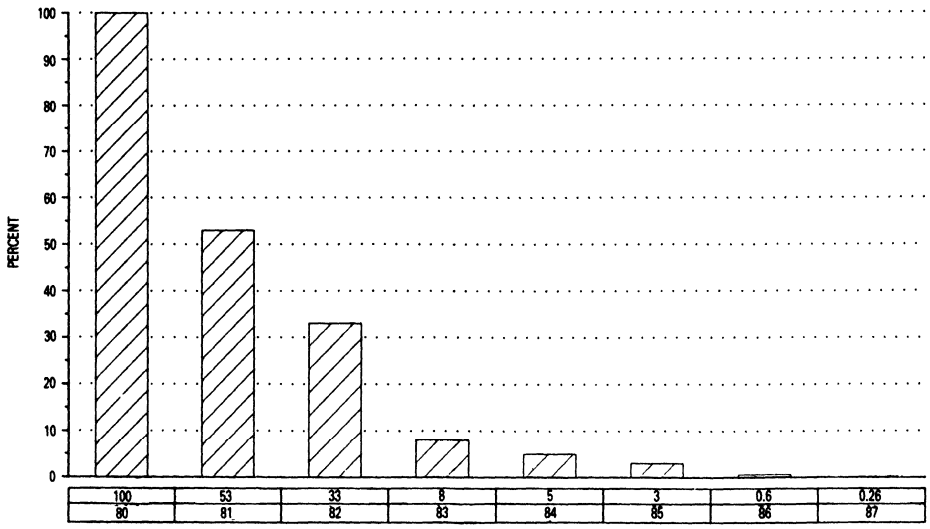


Figure 16-2. Outgoing Electrical Quality (AOQ) Trend/Normalized 1980 = 100%

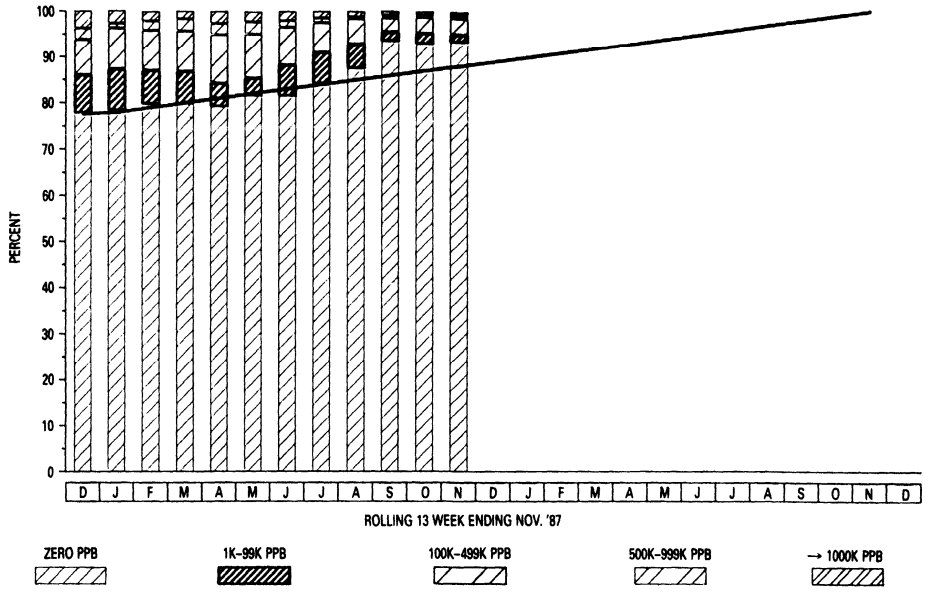


Figure 16-3. Percent (%) of Devices with Zero Parts Per Billion (AOQ)

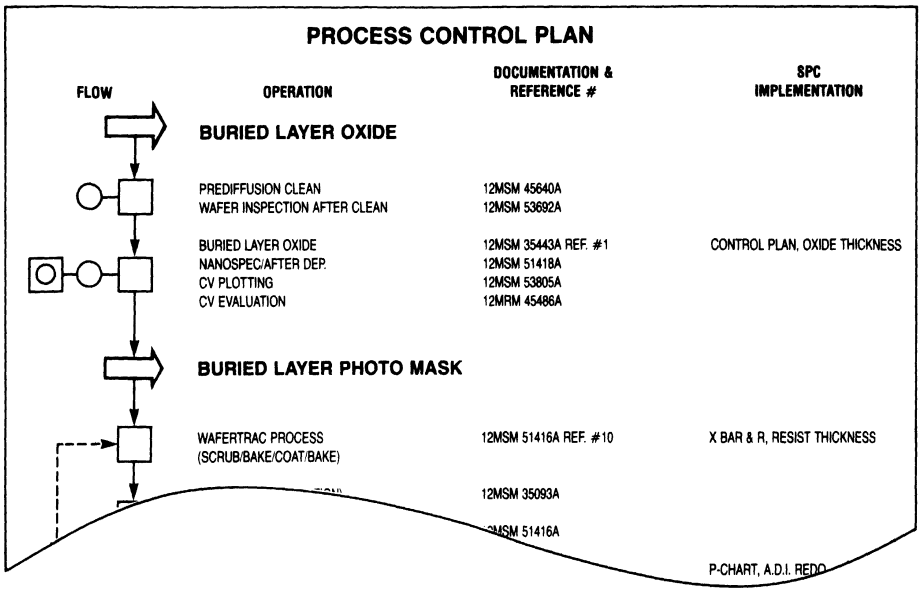


Figure 16-4. Portion of a Process Flow Chart From Wafer Fab, Showing Documentation Control and SPC

Characteristics:	Code	Description	Code	Description
	A.	VISUAL DEFECTS	E.	FILM SHEET RESISTANCE
	B.	VISUAL DEFECTS . . . MICROSCOPE	F.	REFRACTIVE INDEX
	C.	PARTICLE . . . MONITOR	G.	CRITICAL DIMENSION
	D.	FILM THICKNESS	H.	CV PLOT

Process Location	Ref. No.	Characteristic Affected	Part/Process Detail	Measurements Method	Analysis Methods	Frequency Sample Size	Reaction Plan: Point out of Limit (3) (4)
B.L. OXIDE	1	D	OXIDE THICKNESS	NANOMETRIC	CONTROL GRAPH	EVERY RUN 3 WFR/RUN	IMPOUND LOT (1) ADJUST TIME TO CENTER PROCESS PER SPEC
EPI	2	D	THICKNESS	DIGILAB	$\bar{X}$ R CHART	EVERY RUN 5SITES/WFR	IMPOUND LOT (1) NOTIFY ENGR.
QA		D	THICKNESS	DIGILAB	$\bar{X}$ R CHART	1WFR/SHIFT 5SITES/WFR	IMPOUND LOT (2) NOTIFY ENGR.
		E	FILM RESISTIVITY	4PT PROBE	$\bar{X}$ R CHART	EVERY RUN 5SITES/WFR	IMPOUND LOT (1) NOTIFY ENGR.
QA		E	FILM [illegible]	4PT PROBE	$\bar{X}$ R CHART	1WFR/SHIFT 5SITES/WFR	IMPOUND LOT (2) NOTIFY ENGR.
DEEP			[illegible]PROBE		MOVING R	EVERY LOT 1 CTRL WFR PER LOT	IMPOUND LOT NOTIFY LPC [illegible]

Figure 16-5. Part of a Wafer Fab Control Plan, Showing Statistical Process Control Details

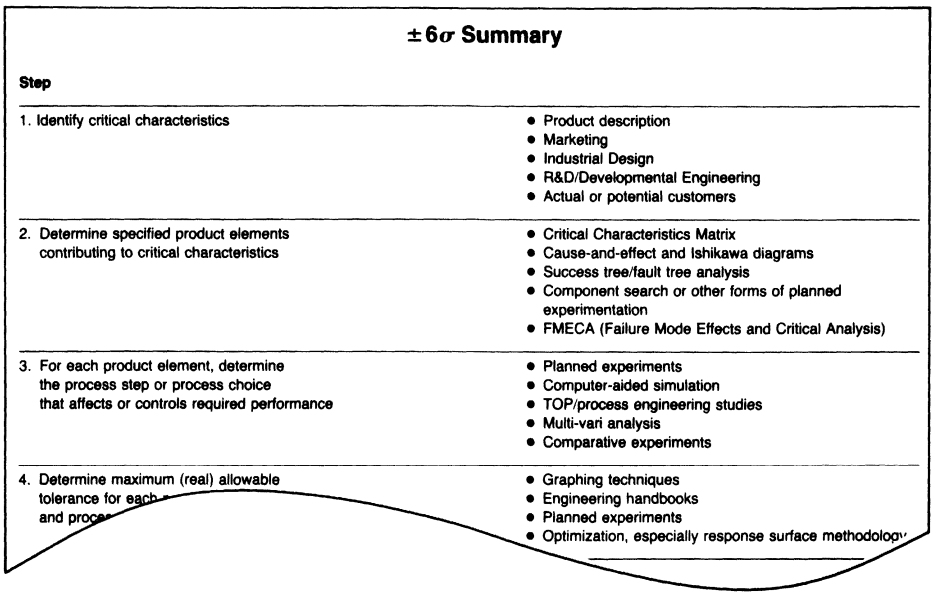


Figure 16-6. Part of Six Sigma (6σ) Roadmap Showing Steps to Six Sigma Capability

Reliability Concepts

Reliability is the probability that a Linear integrated circuit will perform its specified function in a given environment for a specified period of time. This is the classical definition of reliability applied to Linear integrated circuits.

Another way of thinking about reliability is in relationship to quality. While quality is a measure of variability (extending to potential nonconformances-rejects) in the population domain, reliability is a measure of variability (extending to potential nonconformances-failures) in the population, time and environmental conditions domain. In brief **reliability** can be thought of as **quality over time and environmental conditions.**

The most frequently used reliability measure for integrated circuits is the **failure rate expressed** in percent per thousand devices hours (%/1000 hrs.). If the time interval is small the failure rate is called **"Instantaneous Failure Rate"** [λ (t)] or "Hazard Rate." If the time interval is long (for example total operational time) the failure rate is called **"Cumulative Failure Rate."**

The number of failures observed, taken over the number of device hours accumulated at the end of the observation period and expressed as a percent is called the point estimate failure rate. This however, is a number obtained from observations from a sample of all integrated circuits. If we are to use this number to estimate the failure rate of all integrated circuits (total population), we need to say something about the risk we are taking by using this estimate. A **risk** statement is provided by the **confidence level** expressed together with the failure rate. For example, a 0.1% per 1000 device hours failure rate at 90% confidence level can be thought of as 90% of the integrated circuits will have a failure rate below 0.1%/1000 hours. Mathematically the failure rate at a given confidence level is obtained from the point estimate and the **CHI square** (X^2) distribution. (The X^2 is a statistical distribution used to relate the observed and expected

frequencies of an event.) In practice, a reliability calculator rule is used which gives the failure rate at the confidence level desired for the number of failures and device hours under question.

As the number of device hours increases, our confidence in the estimate increases. In integrated circuits, it is preferred to make estimates on the basis of failures per 1,000,000,000 (10^9) device hours (**FITS**) or more. If such large numbers of device hours are not available for a particular device, then the point estimate is obtained by pooling the data from devices that are similar in process, voltage, construction, design, etc., and for which we expect to see the same failure modes in the field.

The environment is specified in terms of the temperature, electric field, relative humidity, etc., by an **Eyring** type of an equation of the form:

$$\lambda = Ae^{-\frac{\emptyset}{KT}} \ldots e^{-\frac{B}{RH}} \ldots e^{-\frac{C}{E}} \ldots$$

Where A, B, C, Ø & K are constants, T is temperature, RH is relative humidity, E is the electric field, etc.

The most familiar form of this equation deals with the first exponential which shows an **Arrhenious type** relationship of the **failure rate** versus the **junction temperature** of integrated circuits, while the causes of failure generally remain the same. Thus, we can test devices near their maximum junction temperatures, analyze the failures to assure that they are the types that are accelerated by temperature and then applying known acceleration factors, estimate the failure rates for lower junction temperatures. Figure 16-7 shows an example of a curve which gives estimates of typical failure rates versus temperature for integrated circuits.

Arrhenious type of equation: $\lambda = Ae^{-\frac{\emptyset}{KT}}$

Where: λ = Failure Rate
A = Constant
e = 2.72
Ø = Activation Energy
K = Botzman's Constant
T = Temperature in Degrees Kelvin

$T_J = T_A + \theta_{JA} P_D$ or $T_J = T_C + \theta_{JC} P_D$

Where: T_J = Junction Temperature
T_A = Ambient Temperature
T_C = Case Temperature
θ_{JA} = Junction to Ambient Thermal Resistance
θ_{JC} = Junction to Case Thermal Resistance
P_D = Power Dissipation

Failure rate curves for equipment and devices can be represented by an idealized graph called the **Bathtub Curve** (Figure 16-8).

There are three important regions identified on this curve. In Region A, the failure rate decreases with time and it is generally called **infant mortality** or early life failure region. In Region B, the failure rate has reached a relatively constant level and it is called **constant failure rate** or **useful life region.** In the

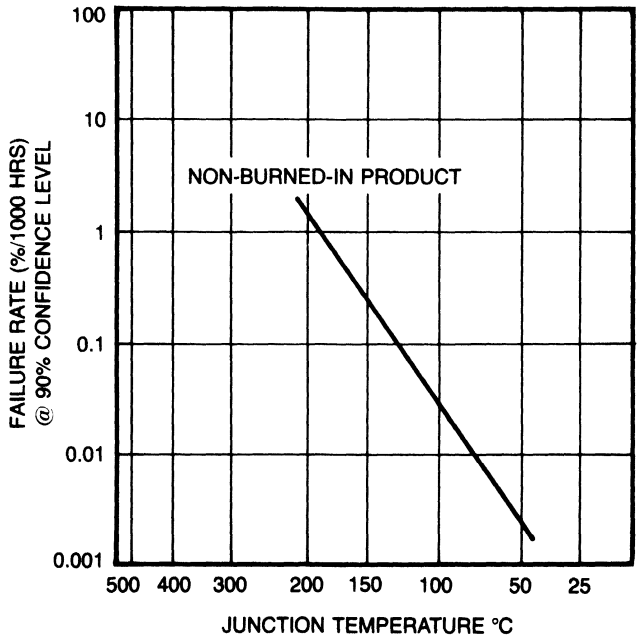


Figure 16-7. Typical Failure Rate versus Junction Temperature

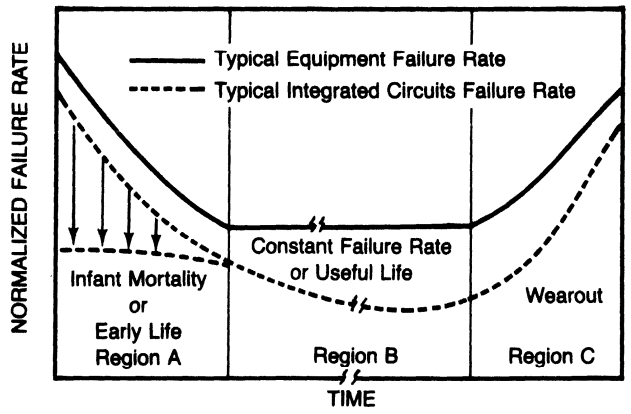


Figure 16-8. Failure Rate versus Time (Bathtub Curve)

third region, the failure rate increases again and it is called wearout region. Modern integrated circuits generally do not reach the wearout portion of the curve when operated under normal use conditions.

The **wearout** portion of the curve can usually be identified by using highly accelerated test conditions. For modern integrated circuits, even the useful life portion of the curve is characterized by so few failures compared to the accumulated device hours, that the **useful life** portion of the curve looks like a continuously decreasing failure rate curve (Figure 16-8, dotted line).

The **infant mortality** portion of the curve is of most interest to equipment manufacturers because of its impact on customer perception and potential warranty costs. In recent years the infant mortality portion of the curve for integrated

circuits, and even equipment, has been drastically reduced (Figure 16-8, note arrows showing reduction of infant mortality). The reduction was accomplished by improvements in technology, emphasis on statistical process control, reliability modeling in design and reliability, etc.). In this respect many integrated circuit families have a continuously decreasing failure rate curve.

Does a user still need to consider burn-in? For this question to be answered properly the IC user must consider the **target failure rate** of the equipment, **apportioned** to the components used, application environment, maturity of equipment and components (new versus mature technology), the impact of a failure (i.e. safety versus casual entertainment), maintenance costs, etc. Therefore, if the IC user is going through these considerations for the first time, the question of burn-in at the component level should be discussed during a user-vendor interface meeting.

A frequently asked question is about the reliability differences between **plastic** versus **hermetic** packaged integrated circuits. In general, for all bipolar integrated circuits including linear, the field removal rates are the same for normal use environments, with many claims of plastic being better because of their "solid block" structure.

The tremendous increase in reliability of plastic packages has been accomplished by the continuous improvements in piece parts, materials and processes. Nevertheless differences can still be observed under highly accelerated environmental conditions. For example, if a bimetallic (gold wire and aluminum metallization) system is used in plastic packages and they are placed on a high temperature operating life test (125°C) then failures in the form of opens will be observed after 10,000 hours of continuous operating life at the gold to aluminum interface. Packages, whether plastic or hermetic, with a monometallic system (aluminum wire to aluminum metallization) will have no opens because of the absence of the gold to aluminum interface. As a result, a difference in failure rates will be observable.

Differences in failure rates between plastics and hermetics could be observed if devices from both packaging systems are placed in an environment of 85°C; 85% RH with bias applied. At some point in time plastic encapsulated ICs should fail since they are considered pervious by moisture, (the failure mechanism being corrosion of the aluminum metallization) while hermetic packages should not fail since they are considered impervious by moisture. The reason the word **"should"** was used is because advances in plastic compounds, package piece parts, encapsulation processes and final chip passivation have made plastic integrated circuits capable of operating more than 5000 hours without failures in an 85°C; 85% RH environment. Differences in failure rates due to internal corrosion between plastic and hermetic packages may not be observable until well after 5000 operating hours.

The aforementioned two examples had environments substantially more accelerated than normal life so these two issues discussed are not even a factor under normal use conditions. In addition, mechanisms inherent in hermetic packages but absent in plastics were not even considered here. Improved reliability of plastic encapsulated ICs has decreased demand of hermetic packages to the point where many devices are offered only in plastic packages. The user then should feel comfortable in using the present plastic packaging systems.

A final question that is asked by the IC users is: how can one be assured that the reliability of standard product does not degrade over time? This is accomplished by our emphasis on statistical process control, in-line reliability assessment and reliability auditing by periodic and strategic sampling and accelerated testing of the various integrated circuit device packaging systems. A description of these audit programs follows below.

Linear Reliability Audit Program

The reliability of a product is a function of design and manufacturing. Inherent reliability is the reliability which a product would have if there were no imperfections in the materials, piece parts and manufacturing processes of the product. The presence of imperfections gives risk to the actual reliability of the product.

Motorola uses on-line and off-line reliability monitoring in an attempt to prevent situations which could degrade reliability. On-line reliability monitoring is at the wafer and assembly levels while off-line reliability monitoring involves reliability assessment of the finished product through the use of accelerated environmental tests.

Continuous monitoring of the reliability of Linear integrated circuits is accomplished by the Linear Reliability Audit Program, which is designed to compare the actual reliability to that specified. This objective is accomplished by periodic and strategic sampling of the various integrated circuit device packaging systems. The samples are tested by subjecting them to accelerated environmental conditions and the results are reviewed for unfavorable trends that would indicate a degradation of the reliability or quality of a particular packaging system. This provides the trigger mechanisms for initiating an investigation for cause and corrective action. Concurrently, in order to provide a minimum of interruption of product flow and assure that the product is fit for use, a lot by lot sampling or a nondestructive type 100% screen is used to assure that a particular packaging system released for shipment does have the expected reliability. This rigorous surveillance is continued until there is sufficient proof (many consecutive lots) that the problem has been corrected.

The Standard Logic and Analog Integrated Circuits Group has used reliability audits since the late sixties. Such programs have been identified by acronyms such as CRP (Consumer Reliability Program), EPIIC (Environmetal Package Indicators for Integrated Circuits), LAPP (Linear Accelerated Punishment Program), and RAP (Reliability Audit Program).

Currently, the Bipolar Analog Reliability Audit Program consists of a Weekly Reliability Audit and a Quarterly Reliability Audit. The Weekly Reliability Audit consists of rapid (short time) types of tests used to monitor the production lines on a real time basis. This type of testing is performed at the assembly/test sites worldwide. It provides data for use as an early warning system for identifying negative trends and triggering investigations for causes and corrective actions.

The Quarterly Reliability Audit consists of long term types of tests and is performed at the U.S. Bipolar Analog Division Center. The data obtained from the Quarterly Reliability Audit is used to assure that the correlation between the short term weekly tests and long term quarterly tests has not changed, and a new failure mechanism has not appeared.

A large data base is established by combining the results from the Weekly Reliability Audit with the results from the Quarterly Reliability Audit. Such a data base is necessary for estimating long term failure rates and evaluating potential process improvement changes. Also, after a process improvement change has been implemented, the Linear Reliability Audit Program provides a system for monitoring the change and the past history data base for evaluating the affect of the change.

Weekly Reliability Audit

The Weekly Reliability Audit is performed by each assembly/test site worldwide. The site must have capability for final electrical and quality assurance testing; reliability testing and first level of failure analysis. The results are reviewed on a continuous basis and corrective action is taken when appropriate. The results are accumulated on a monthly basis and published.

The Reliability Audit test plan is as follows:

Electrical Measurements: Performed initially and after each reliability test, consists of critical parameters and functional testing at 25°C on a go-no-go basis.

High Temperature Operating Life: Performed to detect failure mechanisms that are accelerated by a combination of temperature and electric fields. Procedure and conditions are per the MIL-STD-883, Method 1015 with an ambient temperature of 145°C for 40 hours or equivalent based on a 1.0eV activation energy and the Arrhenious equation.

Approximate Accelerated Factors

	125°C	50°C
145°C	4	4000
125°C	1	1000

Temperature Cycling/Thermal Shock: Performed to detect mechanisms related to thermal expansion and contraction of dissimilar materials, etc. Procedures and conditions are per MIL-STD-883, Methods 1010 or 1011, with ambient temperatures of −65°C to +150°C or −40°C to +125°C (JEDEC-STD-22-A104), minimum of 100 cycles.

Pressure Temperature Humidity (Autoclave): Performed to measure the moisture resistance of plastic encapsulated packages. It detects corrosion type failure mechanisms due to free ionic contaminants that may have entered the package during the manufacturing processes. Conditions are per JEDEC-STD-22, Method 102, a temperature of 121°C, steam environment and 15psig. The duration of the test is 40 hours.

Analysis Procedure: Devices failing to meet the electrical criteria after being subjected to an accelerated environment type test are verified and characterized electrically, then submitted for failure analysis.

Quarterly Reliability Audit

The Quarterly Bipolar Analog Reliability Audit Program is performed at the U.S. Bipolar Analog Division Center. This testing is designed to assure that the correlation between the short term weekly tests and the longer quarterly tests has not changed and that no new failure mechanisms have appeared. It also provides additional long term information for a data base for estimating failure rates and evaluation of potential process improvement changes.

Electrical Measurements: Performed initially and at interim readouts, consist of all standard dc and functional parameters at 25°C, measured on a go-no-go basis.

High Temperature Operating Life Test: Performed to detect failure mechanisms that are accelerated by a combination fo temperature and electric fields. Procedure and conditions are per MIL-STD-883, Method 1015, with an ambient temperature of 145°C for 40 and 250 hours or equivalent, based on 1.0eV activation energy and the Arrenious equation.

Approximate Acceleration Factors

	125°C	50°C
145°C	4	4000
125°C	1	1000

Temperature Cycling/Thermal Shock: Performed to detect mechanisms related to thermal expansion and contraction, mismatch effects, etc. Procedure and conditions are per MIL-STD-883, Methods 1010 or 1011, with ambient temperatures of −65°C to +150°C or −40°C to +125°C (JEDEC-STD-22-A104) for 100 and 1000 cycles. Temperature Cycling and Thermal Shock are used interchangeably.

Pressure Temperature Humidity (Autoclave): Performed to measure the moisture resistance of plastic encapsulated packages. It detects corrosion type failure mechanism due to free ionic contaminants that may have entered the package during the manufacturing processes. Conditions are per JEDEC-STD-22, Method 102, a temperature of 121°C, steam environment and 15psig. The duration of the test is for 96 hours, with a 48 hour interim readout.

Pressure Temperature Humidity Bias (Biased Autoclave): This test measures the moisture resistance of plastic encapsulated packages. It detects corrosion type failure mechanism due to free and bounded ionic contaminants that may have entered the package during the manufacturing processes, or they may be bound in the materials of the integrated circuit packaging system and activated by the moisture and the applied electric fields. Conditions are per JEDEC-STD-22, Method 102, with bias applied. Temperature is 121°C, steam environment and 15psig. Duration is for 32 hours, with a 16 hour interim readout. This test detects the same type of failures as the Temperature Humidity Bias (85°C, 85% RH, with bias) test, only faster. The acceleration factor between PTHB and THB is between 20 and 40 times, depending on the type of corrosion mechanism, electric field and packaging system.

Temperature, Humidity and Bias (THB): This test measures the moisture resistance of plastic encapsulated packages. It detects corrosion type failure mechanisms due to free and bounded ionic contaminants that may have entered the package during the manufacturing processes, or they may be bound in the materials of the integrated circuit packaging system and activated by moisture and the applied electric fields. Conditions are per JEDEC-STD-22, Method 102 (85°C, 85% RH), with bias applied. The duration is for 1008 hours, with a 504 hour interim readout. The acceleration factor between THB (85°C, 85% RH and bias) and the 30°C, 90% RH is typically 40–50 times, depending on the type of corrosion mechanism, electric field and packaging system.

Analysis Procedure: Devices failing to meet the electrical criteria after being subjected to an accelerated environment type test are verified and characterized electrically, then submitted for failure analysis.

SECTION 17
IC REGULATOR SELECTION GUIDES

The selection guides in this section are included as an aid to choosing an appropriate IC regulator. These guides are organized according to regulator type and list all the IC voltage regulators presently offered by Motorola.

A. ADJUSTABLE OUTPUT REGULATORS

When an adjustable output voltage is required, use of the regulators shown in Table 17-1 is recommended. Output voltage is set by adjusting the value of an external resistor or resistors. More complete data on individual devices can be found in the data sheets of Section 18. An explanation of the column headings shown in Table 17-1 follows:

Maximum Output Current ($I_{O\ max}$)

Maximum output current in which key device parameters are specified.

Device

Motorola part number for the IC regulator.

Suffix

Designator for case type; and, in some products, includes temperature range.

Output Voltage (V_{out})

The range of output voltages that can be obtained with the regulator basic circuit configuration. (Methods for extending output voltage range are shown in Section 3.)

Input Voltage (V_{in})

Range of allowable DC input voltages. These are instantaneous values. Exceeding maximum input voltage could result in regulator damage, while dropping below minimum value will cause loss of regulation.

Input-Output Differential (V_{in}–V_{out})

This is the minimum voltage across the regulator for proper operation.

Maximum Power Dissipation ($P_{D\ max}$)

Maximum power the device can dissipate in free air at T_A = 25°C without a heatsink; and with case temperature held constant at T_C = 25°C.

Line Regulation (Reg_{line})

The percent change of output voltage for a change in input supply voltage. Given by:

$$Reg_{line}\ (\%) = \frac{\Delta V_{out}}{V_{out}} \times \frac{1}{\Delta V_{in}} \times 100$$

where ΔV_{out} = change in V_{out}

ΔV_{in} = change in V_{in}

This performance figure applies for the entire output and input voltage range for the regulator. For actual test conditions, consult data sheets in Section 18.

Load Regulation (Reg_{load})

The percent change of output voltage for a change in output current. For actual test conditions, consult data sheets in Section 18.

Typical Temperature Coefficient of Output Voltage (T_C of V_{out})

Percent change in output voltage per degree Celsius rise in junction temperature.

Maximum Operating Junction Temperature ($T_{J\ max}$)

Maximum junction temperature allowed before damage occurs. For complete thermal information consult data sheets in Section 18. See Section 15 for heat-sinking techniques.

Packages

Case 1-03: "TO-204AA" metal can
Case 29-04: "TO-226AA" plastic package
Case 79-05: "TO-205AD" metal can
Case 221A-04: "TO-220AB" plastic package
Case 314D-02: 5-terminal plastic package
Case 603-04: 10-pin "TO-100" metal can
Case 632-08: 14-pin ceramic dual-in-line package
Case 646-06: 14-pin plastic dual-in-line package

For detailed outline drawings of these case styles, consult Section 19.

TABLE 17-1
ADJUSTABLE OUTPUT VOLTAGE REGULATORS

Motorola offers a broad line of adjustable output voltage regulators with a variety of output current capabilities. Adjustable voltage regulators provide users the capability of stocking a single integrated circuit providing a wide range of output voltages for industrial and communications applications. The three-terminal devices require only two external resistors to set the output voltage.

Positive Output Regulations

I_O mA Max	Device	Suffix	V_{out} Volts		V_{in} Volts		$V_{in} - V_{out}$ Differential Volts Min	P_D Watts Max		Regulation % V_{out} @ T_A = 25°C Max		T_C V_{out} Typ %/°C	T_J = °C Max	Case
			Min	Max	Min	Max		T_A = 25°C	T_C = 25°C	Line	Load			
100	LM317L	H,Z	1.2	37	5.0	40	3.0	Internally Limited		0.04	0.5	0.006	125	29,79
	LM217L#									0.02	0.3	0.004	150	
	LM117L*											0.003		
	LM2931C	T	3.0	24	3.16		0.6			0.15	1.0	—	125	314D
150	MC1723	CP	2.0	37	9.5	40	3.0	1.25	—	0.1	0.3	0.003	150	646
		CG						1.0	2.1			0.003		603C
		G										0.002		
		CL						1.5	—			0.003	175	632
		L							—			0.002		
500	LM317M	T	1.2	37	5.0	40	3.0	Internally Limited		0.04	0.5	0.0056	125	221A
1500	LM317	T	1.2	37	5.0	40	3.0	Internally Limited		0.04	0.5	0.006	125	221A
	LM317	H,K												79,1
	LM217#										0.3	0.004		
	LM117*									0.02		0.003	150	
3000	LM350	T	1.2	33	5.0	36	3.0	Internally Limited		0.03	0.5	0.008	125	221A
	LM350	K												1
	LM250#									0.01	0.3	0.0057	150	
	LM150*											0.0051		

Negative Output Regulators

I_O mA Max	Device	Suffix	V_{out} Volts		V_{in} Volts		$V_{in} - V_{out}$ Differential Volts Min	P_D Watts Max		Regulation % V_{out} @ T_A = 25°C Max		T_C V_{out} Typ %/°C	T_J = °C Max	Case
			Min	Max	Min	Max		T_A = 25°C	T_C = 25°C	Line	Load			
500	LM337M	T	−1.2	−37	5.0	40	3.0	Internally Limited		0.04	1.0	0.0048	125	221A
1500	LM337	T	−1.2	−37	5.0	40	3.0	Internally Limited		0.04	1.0	0.0048	125	221A
	LM337	H,K												79,1
	LM237#									0.02	0.5	0.0034	150	
	LM137*											0.0031		

#T_J = −25° to +150°C *T_J = −55° to +150°C

B. FIXED OUTPUT REGULATORS

If low cost and easy implementation are prime regulator design considerations, the fixed output, three terminal regulators shown in Table 17-2 are recommended. These are available with output current capabilities from 100 mA to 3.0 A. All have internal overcurrent, safe-operating area, and thermal protection circuitry. Complete device specifications are given in the data sheets of Section 18. An explanation of the column headings shown in Table 17-2 follows:

Output Voltage (V_{out})

Nominal output voltage for positive and negative regulators. The adjacent column indicates worst case tolerance (Volts). (Methods for adjusting output voltage are shown in Section 3.)

Maximum Output Current ($I_{O\ max}$)

Maximum output current available from regulator under normal operating conditions. (Methods for obtaining greater output currents are shown in Section 3.)

Device

Two columns are provided listing Motorola part numbers for positive and negative voltage outputs.

Input Voltage min/max (V_{in})

Range of allowable instantaneous dc input voltage. Exceeding maximum V_{in} could result in regulator damage, while dropping below minimum value will cause loss of regulation.

Line Regulation (Reg_{line})

Change in output voltage for a given change in input voltage. Test specifications are given in the data sheets of Section 18.

Load Regulation (Reg_{load})

Change in output voltage for a given change in output current. Test specifications are given in the data sheets of Section 18.

Typical Temperature Coefficient of Output Voltage ($\Delta V/\Delta T$)

Typical change in output voltage per degree celsius change in junction temperature.

Packages

Case 1-03: "TO-204AA" metal can
Case 29-04: "TO-226AA" plastic package
Case 79-05: "TO-205AD" metal can
Case 221A-04: "TO-220AB" plastic package

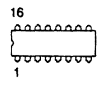
For detailed outline drawings of these case styles, consult Section 19.

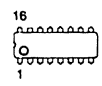
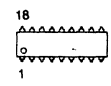
Package Styles

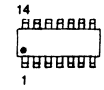





CASE	1 TO-204AA	29 TO-226AA	79 TO-205AD	221A TO-220AB	603 TO-100	603C
MATERIAL	Metal	Plastic	Metal	Plastic	Metal	Metal
SUFFIX	K	P, Z	G, H	T	G	G





CASE	620	632 (TO-116)	646	648	707	726	751A
MATERIAL	Ceramic	Ceramic	Plastic	Plastic	Plastic	Ceramic	Plastic
SUFFIX	J, L	L	P	N, P	N	J	D

TABLE 17-2
FIXED OUTPUT VOLTAGE REGULATORS

These low cost monolithic circuits provide positive and/or negative regulation at currents from 100 mA to 3.0 A. They are ideal for on-card regulation employing current limiting and thermal shutdown. Low V_{diff} devices are offered for battery powered systems.

Although designed primarily as fixed voltage regulators, these devices can be used with external components to obtain adjustable voltages and currents.

Fixed-Voltage, 3-Terminal Regulators for Positive or Negative Polarity Power Supplies

V_{out} Volts	Tol.† Volts	I_O mA Max	Device Positive Output	Device Negative Output	V_{in} Min/Max	Reg_{line} mV	Reg_{load} mV	$\Delta V_O/\Delta T$ mV/°C Typ	Case Suffix
5	±0.5	100	LM2931-5.0	—	5.6/40	30	50	1.0	Z, T
			MC78L05C	MC79L05C	6.7/30	200	60		P, G
	±0.25		LM2931A-5.0	—	5.6/40	30	50		Z, T
			MC78L05AC	MC79L05AC	6.7/30	150	60		P, G
		500	MC78M05C	MC79M05C	7/35	100	100	1.0	G, T
	±0.4	1500	LM109	—				1.1	K, H
			LM209	—		50			
	±0.25		LM309	—				1.0	
	±0.35		MC7805*	—	8.0/35			0.6	K
	±0.25		MC7805B#	—	8/35	100		1.0	T
			MC7805C	MC7905C	7/35				K, T
	±0.2		MC7805A*	—	7.5/35	10	50	0.6	K
			MC7805AC	MC7905AC			100		K, T
	±0.25		LM140-5*	—	7.0/35	50	50		K
	±0.2		LM140A-5*	—		10	25		
	±0.25		LM340-5	—		50	50		K, T
	±0.2		LM340A-5	—		10	25		
	±0.1		TL780-05C	—	7.0/35	5.0	25	0.06	KC

#T_J = −40° to +125°C †Output Voltage Tolerance for Worst Case *T_J = −55° to +150°C (continued)

Fixed Output Voltage Regulators (continued)

V_{out} Volts	Tol.† Volts	I_O mA Max	Device Positive Output	Device Negative Output	V_{in} Min/Max	Reg_{line} mV	Reg_{load} mV	$\Delta V_O/\Delta T$ mV/°C Typ	Case Suffix
5	±0.25	3000	MC78T05C	—	7.3/35	25	30	0.1	K, T
	±0.2		MC78T05AC	—		10	25		
	±0.4	3000	LM123*	—	7.5/20	25	100	0.1	K
			LM223	—					
	±0.25		LM323	—					T
	±0.2		LM123A	—					K
			LM223A	—		15	50		
			LM323A	—					T
5.2	±0.26	1500	—	MC7905.2C	7.2/35	105	105	1.0	T
6	±0.3	500	MC78M06C	—	8/35	100	120	1.0	T
	±0.35	1500	MC7806*	—	9/35	60	100	0.7	K
	±0.3		MC7806B#	—		120	120		T
			MC7806C	MC7906C	8/35				K, T
	±0.24		MC7806AC	—	8.6/35	11	100		T
			LM140-6*	—	8/35	60	60		K
	±0.3		LM340-6	—					K, T
8	±0.8	100	MC78L08C	—	9.7/30	200	80	—	P, G
			MC78L08AC	—		175			
	±0.4	500	MC78M08C	—	10/35	100	160	1.0	G, T
		1500	MC7808*	—	11.5/35	80	100		K
			MC7808B#	—		160	160		T
			MC7808C	MC7908C	10.5/35				K, T
	±0.3		MC7808AC	—	10.6/35	13	100		T
	±0.4		LM140-8*	—	10.5/35	80	80		K
			LM340-8	—					K, T
		3000	MC78T08C	—	10.4/35	35	30	0.16	
12	±1.2	100	MC78L12C	MC79L12C	13.7/35	250	100	—	P, G
	±0.6		MC78L12AC	MC79L12AC					
		500	MC78M12C	MC79M12C	14/35	100	240	1.0	G, T
		1500	MC7812*	—	15.5/35	120	120	1.5	K
			MC7812B#	—		240	240		T
			MC7812C	MC7912C	14.5/35				K, T
	±0.5		MC7812A*	—	14.8/35	18	50		K
			MC7812AC	—			100		T
	±0.6		LM140-12*	—	14.5/35	120	120	1.5	K
	±0.5		LM140A-12*	—		18	32		
	±0.6		LM340-12	—		120	120		K, T
	±0.5		LM340A-12	—		18	32		
	±0.24		TL780-12C	—		5.0		0.15	KC
	±0.6	3000	MC78T12C	—	14.5/35	45	30	0.24	K, T
	±0.5		MC78T12AC	—		18	25		

#T_J = −40° to +125°C †Output Voltage Tolerance for Worst Case *T_J = −55° to +150°C (continued)

Fixed Output Voltage Regulators (continued)

V_{out} Volts	Tol.† Volts	I_O mA Max	Device Positive Output	Device Negative Output	V_{in} Min/Max	Reg_{line} mV	Reg_{load} mV	$\Delta V_O/\Delta T$ mV/°C Typ	Case Suffix
15	±1.5	100	MC78L15C	MC79L15C	16.7/35	300	150	—	P, G
	±0.75		MC78L15AC	MC79L15A					
		500	MC78M15C	MC79M15C	17/35	100	300	1.0	G, T
		1500	MC7815*	—	18.5/35	150	150	1.8	K
			MC7815B#	—		300	300		T
			MC7815C	MC7915C	17.5/35				K, T
	±0.6		MC7815A*	—	17.9/35	22	50		K
			MC7815AC	—			100		K, T
	±0.75		LM140-15*	—	17.5/35	150	150		K
	±0.6		LM140A-15*	—		22	35		
	±0.75		LM340-15	—		150	150		K, T
	±0.6		LM340A-15	—		22	35		
	±0.3		TL780-15C	—		15	60	0.18	KC
	±0.75	3000	MC78T15C	—	17.5/40	55	30	0.3	K, T
	±0.6		MC78T15AC	—		22	25		
18	±1.8	100	MC78L18C	MC79L18C	19.7/35	325	170	—	P
	±0.9		MC78L18AC	MC79L18AC					
		500	MC78M18C	—	20/35	100	360	1.0	G, T
		1500	MC7818*	—	22/35	180	180	2.3	K
			MC7818B#	—		360	360		T
	±0.7		MC7818C	MC7918C	21/35				K, T
			MC7818AC	—		31	100		T
	±0.9		LM340-18	—		180	180		T
20	±1.0	500	MC78M20C	—	22/40	10	400	1.1	G, T
24	±2.4	100	MC78L24C	MC79L24C	25.7/40	350	200	—	P
	±1.2		MC78L24AC	MC79L24AC		300			
		500	MC78M24C	—	26/40	100	480	1.2	G, T
		1500	MC7824*	—	28/40	240	240	3.0	K
			MC7824B#	—		480	480		T
			MC7824C	MC7924C	27/40				K, T
	±1.0		MC7824AC	—	27.3/40	36	100		T
	±1.2		LM340-24	—		240	240		T

#T_J = −40° to +125°C †Output Voltage Tolerance for Worst Case *T_J = −55° to +150°C

C. SPECIALTY REGULATORS AND SWITCHING REGULATOR CONTROL CIRCUITS

In addition to the regulators of Tables 17-1 and 17-2, Motorola offers two specialty regulators: the MC1568/MC1468 ±15 V Tracking regulator and the MC1466 Precision Floating regulator. General specifications for these regulators are shown in Table 17-3. More complete data on these devices can be found in the data sheets of Section 18. An explanation of the column headings shown in Table 17-3 follows:

Device

Motorola part number for the IC regulator. (No symbol indicates 0°C to +70°C operating ambient temperature range. * Indicates −55°C to +125°C operating ambient temperature range.)

Output Voltage (V_O)

For the tracking regulators, the value of the preset output voltage. (Methods for obtaining adjustable output voltages are shown in Section 3.)

For the floating regulators, the range of output voltages that can be obtained with the regulator.

* Indicates that the maximum obtainable output voltage is dependent only on the characteristics of the external pass element.

Maximum Output Current ($I_{O\ max}$)

Absolute maximum output current that can be obtained without damaging regulator. (Methods for obtaining increased output current are shown in Section 3.)

* Indicates that the maximum obtainable output current is dependent only on the characteristics of the external pass element.)

Input Voltage (V_{in})

The range of allowable DC input voltage. This is an instantaneous value. Exceeding maximum V_{IN} could result in regulator damage, while dropping below minimum value will cause loss of regulation.

Auxiliary Supply Voltage (V_{aux})

The floating regulators require an additional dedicated voltage source which is floating with respect to the output ground. The values given are the limits for this auxiliary supply voltage.

Line Regulation (Reg_{line})

Percent change in output voltage for a given change in input voltage. Test specifications are given in the data sheets of Section 18.

Load Regulation (Reg_{load})

Percent change in output voltage for a given change in output current. Test specifications are given in the data sheets of Section 18.

Load Current Regulation

Percent change in output current for a given change in load voltage while in the current regulation mode. Test specifications are given in the data sheets of Section 18.

Typical Temperature Coefficient of Output Voltage (TC of Vo)

Typical percent change in output voltage per degree Celsius change in junction temperature.

Maximum Power Dissipation ($P_{D}max$)

Maximum power which device can safely dissipate when case temperature is held at +25°C; and junction temperature is at its maximum value of +125°C. For complete thermal information, consult data sheets in Section 18. For heat sinking information, see Section 15.

Package

Case 603C-01: 10-pin "TO-100" type metal can
Case 632-08: 14-pin ceramic dual-in-line package

For detailed outline drawings of these case styles, consult Section 18.

TABLE 17-3
SPECIAL REGULATORS

FLOATING VOLTAGE AND CURRENT REGULATORS

Designed for laboratory type power supplies. Voltage is limited only by the breakdown voltage of associated, external, series-pass transistors.

V_{out} Volts		I_O mA			V_{aux} Volts		P_D Watts	$\Delta V_{ref}/V_{ref}$ %		$\Delta I_L/L_L$ %	TC V_{out} %/°C	
Min	Max	Max	Device	Suffix	Min	Max	Max	Line	Load	Max	Typ	Case
0	*	*	MC1466	L	21	30	0.75	0.015	0.015	0.2	0.001	632

*Dependent on characteristics of external series-pass elements.

DUAL ±15 V TRACKING REGULATORS

Internally, the device is set for ±15 V, but an external adjustment can change both outputs simultaneously, from 8.0 V to 20 V.

V_{out} Volts		I_O mA	V_{in} Volts				P_D Watts	Reg_{line}	Reg_{load}	TC %/°C (T_{low} to T_{high})	T_A	
Min	Max	Max	Min	Max	Device	Suffix	Max	mV	mV	Typ	°C	Case
14.5	15.5	±100	17	30	MC1468	G	0.8	10	10	3.0	0 to +75	603C
						L	1.0					632
					MC1568	G	0.8				−55 to +125	603C
						L	1.0					632

MICROPROCESSOR VOLTAGE REGULATOR/SUPERVISORY CIRCUIT

A 5.0 V fixed output with many monitoring functions required in microprocessor-based systems.

V_{out}, V_{ref} Volts		I_{SINK} mA	V_{in} Volts		Reg_{line}	Reg_{load}			T_A	
Min	Max	Max	Min	Max	mV Max	mV Max	Device	Suffix	°C	Case
4.75	5.25	100	7.0	40	40	50	MC34160	P	0 to +70	648C
2.47	2.73	2.0	5.0		20	30	MC33160		−40 to +85	

Switching Regulator Control Circuits

Motorola offers a complete line of switching regulator I.C.s to meet the various demands of the market. Table 17-4 lists devices offered along with key parameters. For detailed specifications, refer to Section 18.

An explanation of the column headings shown in Table 17-4 follows:

Maximum Output Current ($I_{O\ max}$)

This is the maximum output current capability of the switching control circuit outputs.

Minimum Operating Voltage Range (Volts)

Minimum applied voltage to V_{CC} in which normal operation occurs. Maximum applied voltage to V_{CC}, beyond which damage to the I.C. can occur.

Maximum Useful Oscillator Frequency (kHz)

The maximum frequency at which the oscillator will operate to effectively drive the internal logic and outputs.

Operating Mode

This column indicates the feedback method used to maintain stability in the control loop of the switching regulator. Voltage, current, and resonant control modes are available.

Reference Volts

The voltage and tolerance of the on-chip voltage reference. The tolerance shown is at 25°C unless a footnote indicates otherwise.

Package

Case 620-10: 16-pin ceramic dual-in-line package
Case 632-08: 14-pin ceramic dual-in-line package
Case 646-06: 14-pin plastic dual-in-line package
Case 648-06: 16-pin plastic dual-in-line package
Case 693-02: 8-pin ceramic dual-in-line package
Case 707-02: 18-pin plastic dual-in-line package
Case 726-04: 18-pin ceramic dual-in-line package

TABLE 17-4
SWITCHING REGULATOR CONTROL CIRCUITS

These devices contain the primary building blocks which are required to implement a variety of switching power supplies. The product offerings fall into three major categories consisting of single-ended and double-ended controllers, plus single-ended ICs with on-chip power switch transistors. These circuits operate in voltage, current or resonant modes and are designed to drive many of the standard switching topologies. The single-ended configurations include buck, boost, flyback and forward converters. The double-ended devices control push-pull, half bridge and full bridge configurations.

SINGLE-ENDED CONTROLLERS

These single-ended voltage and current mode controllers are designed for use in buck, boost, flyback, and forward converters. They are cost effective in applications that range from 0.1 to 200 watts power output.

I_O mA Max	Minimum Operating Voltage Range Volts	Operating Mode	Reference Volts	Maximum Useful Oscillator Freq. (kHz)	Device	Suffix	T_A °C	Case
250	7.0 to 40	Voltage	5.0 ± 5.0%	200	MC34060	P	0 to +70	646
						L		632
					MC35060	L	−55 to +125	
500			5.0 ± 1.5%		MC34060A	D	0 to +70	751A
						P		646
					MC33060A	D	−40 to +85	751A
						P		646
					MC35060A	L	−55 to +125	632
1000	4.2 to 12	Current	1.25 ± 2.0%	300	MC34129	D	0 to +70	751A
						P		646
					MC33129	D	−40 to +85	751A
						P		646
	11.5 to 30		5.0 ± 2.0%	500	UC3842A	D	0 to +70	751A
						N		626
	11 to 30		5.0 ± 1.0%		UC2842A	D	−25 to +85	751A
						J		693
						N		626
	8.2 to 30		5.0 ± 2.0%		UC3843A	D	0 to +70	751A
						N		626
			5.0 ± 1.0%		UC2843A	D	−25 to +85	751A
						J		693
						N		626
	11.5 to 30		5.0 ± 2.0%		UC3844	D	0 to +70	751A
						N		626
	11 to 30		5.0 ± 1.0%		UC2844	D	−25 to +85	751A
						J		693
						N		626
	8.2 to 30		5.0 ± 2.0%		UC3845	D	0 to +70	751A
						N		626
			5.0 ± 1.0%		UC2845	D	−25 to +85	751A
						J		693
						N		626

TABLE 17-4
SWITCHING REGULATOR CONTROL CIRCUITS (CONTINUED)

SINGLE-ENDED CONTROLLERS WITH ON-CHIP POWER SWITCH

These monolithic power switching regulators contain all the active functions required to implement standard DC-to-DC converter configurations with a minimum number of external components.

I_O mA Max	Minimum Operating Voltage Range Volts	Operating Mode	Reference Volts	Maximum Useful Oscillator Freq. (kHz)	Device	Suffix	T_A °C	Case
1500	2.5 to 40	Voltage	1.25±5.2%#	100	μA78S40	PC	0 to +70	648
						DC		620
						PV	−40 to +85	648
						DM	−55 to +125	620
			1.25±5.6%#		MC34063	P1	0 to +70	626
						U		693
					MC33063	P1	−40 to +85	626
						U		693
					MC35063	U	−55 to +125	
			1.25±2.0%		MC34063A	D	0 to +70	751
						P1		626
					MC33063A	D	−40 to +85	751
						P1		626
					MC35063A	U	−55 to +125	693
3300			1.25±2.0% and 5.05±3.0%		MC34163	P	0 to +70	648
					MC33163		−40 to +85	
3600†	6.8 to 40		5.05±3.0%	70±12% Internally Fixed	MC34166	T	0 to +70	314D
					MC33166		−40 to +85	

#Tolerance applies over the specified operating temperature range.
†Guaranteed minimum, typically 4200 mA.

TABLE 17-4
SWITCHING REGULATOR CONTROL CIRCUITS (CONTINUED)

DOUBLE-ENDED CONTROLLERS

These double-ended voltage and resonant mode controllers are designed for use in push-pull, half-bridge, and full-bridge converters. They are cost effective in applications that range from 100 to 2000 watts power output.

I_O mA Max	Minimum Operating Voltage Range Volts	Operating Mode	Reference Volts	Maximum Useful Oscillator Freq. (kHz)	Device	Suffix	T_A °C	Case
500	7.0 to 40	Voltage	5.0 ± 5.0%#	200	TL494	CN	0 to +70	648
						CJ		620
						IN	−25 to +85	648
						IJ		620
						MJ	−55 to +125	
			5.0 ± 1.5%	300	TL594	CN	0 to +70	648
						IN	−25 to +85	
						MJ	−55 to +125	620
±500	8.0 to 40		5.1 ± 2.0%	400	SG3525A	N	0 to +70	648
						J		620
			5.1 ± 1.0%		SG2525A	N	−25 to +85	648
						J		620
					SG1525A	J	−55 to +125	
			5.1 ± 2.0%		SG3527A	N	0 to +70	648
						J		620
			5.1 ± 1.0%		SG2527A	N	−25 to +85	648
						J		620
					SG1527A	J	−55 to +125	
±200			5.0 ± 2.0%		SG3526	N	0 to +125*	707
						J		726
			5.0 ± 1.0%		SG2526	N	−25 to +150*	707
						J		726
					SG1526	J	−55 to +150*	
±1500	9.6 to 20	Resonant	5.1 ± 2.0%	1000	MC34066	DW	0 to +70	751G
						P		648
					MC33066	DW	−40 to +85	751G
						P		648

#Tolerance applies over the specified operating temperature range.
*Junction Temperature Range.

TABLE 17-5
SPECIAL POWER SUPPLY CONTROLLERS

DUAL CHANNEL CURRENT MODE CONTROLLERS

These high performance dual channel controllers are optimized for off-line AC-to-DC power supplies and DC-to-DC converters in the flyback topology. Applications include desktop computers, peripherals, televisions, games, and various consumer appliances.

I_O mA Max	Minimum Operating Voltage Range Volts	Operating Mode	Reference Volts	Maximum Useful Oscillator Freq. (kHz)	Device	Suffix	T_A °C	Case
±1000	11 to 15.5	Current	5.0±2.0%	500	MC34065	DW	0 to +70	751G
						P		648
					MC33065	DW	−40 to +85	751G
						P		648

UNIVERSAL MICROPROCESSOR POWER SUPPLY CONTROLLER

TCA5600 — T_A = −40° to +75°C, Case 707

A versatile power supply control circuit for microprocessor-based systems which is mainly intended for automotive applications and battery powered instruments. The device provides a power-on Reset delay and a Watchdog feature for orderly microprocessor operation.

Regulated Outputs	Output Current mA	V_{CC} Volts		Reference Volts	Key Supervisory Features
		Min	Max		
E^2PROM Programmable Output: 24 Volts (Write Mode) 5.0 Volts (Read Mode)	150 peak	6.0	35	2.5±3.2%	MPU Reset and Watchdog Circuit
Fixed Linear Output: 5.0 Volts	10 to external buffer transistor				

CONTROL IC FOR LINE-ISOLATED FREE RUNNING FLYBACK CONVERTER

Regulates and monitors the switching transistor in power supplies based on the free oscillating flyback converter principle. Provides excellent Switchmode performance in Hi-Fi equipment, active loudspeakers, as well as applications in TV receivers and video recorders.

I_O mA Max	Minimum Operating Voltage Range Volts	Operating Mode	Reference Volts	Maximum Useful Oscillator Freq. (kHz)	Device	Suffix	T_A °C	Case
±1500	12.3 to 20	Voltage	4.2±5.0%	100	TDA4601	—	−15 to +85	762
						B		707

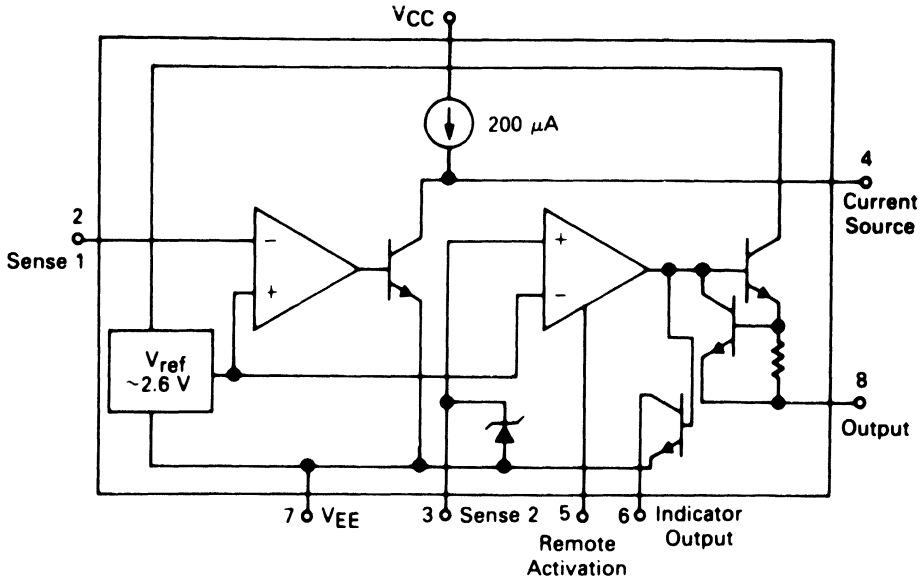
D. POWER SUPERVISORY CIRCUITS

A variety of Power Supervisory Circuits are offered. Overvoltage sensing circuits which drive "crowbar" SCR's are provided in two configurations available in 8-pin packages. These devices provide additional features such as an indicator output drive and remote activation capability, plus an over and undervoltage protection function. Two undervoltage sensing circuits designed as reset controllers in microprocessor-based systems are also available. In addition, a microprocessor voltage regulator/supervisory circuit is also offered.

Overvoltage "Crowbar" Sensing Circuit

MC3523U — T_A = −55° to +125°C, Case 693
MC3423P1,U — T_A = 0° to +70°C, Case 626, 693

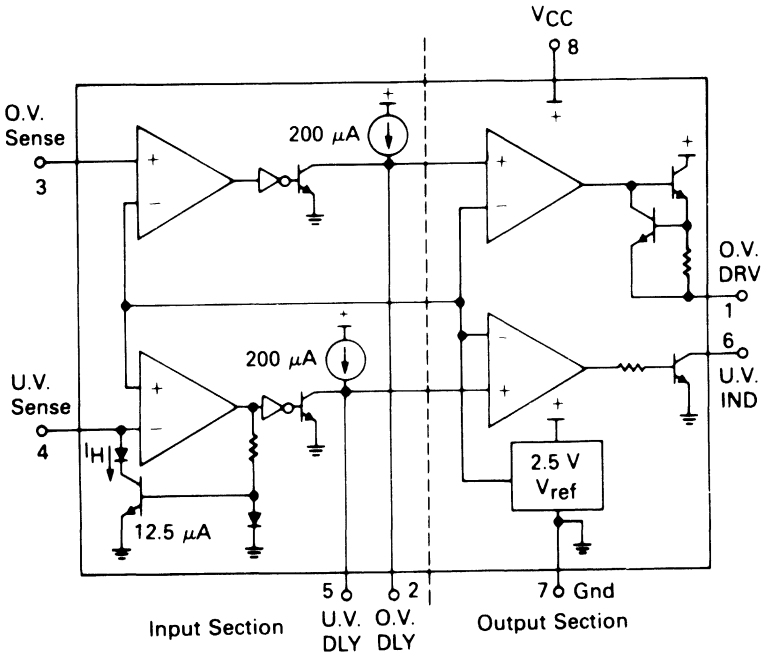
This device can protect sensitive circuitry from power supply transients or regulator failure when used with an external "Crowbar" SCR. The device senses voltage and compares it to an internal 2.6 V reference. Overvoltage trip is adjustable by means of an external resistive voltage divider. A minimum duration before trip is programmable with an external capacitor. Other features include a 300 mA high current output for driving the gate of a "Crowbar" SCR, an open-collector indicator output and remote activation capability.



Over-Under Voltage Protection Circuit

MC3425P1 — T_A = 0° to +70°C, Case 626

The MC3425 is a power supply supervisory circuit containing all the necessary functions required to monitor over and undervoltage fault conditions. This device features dedicated over and undervoltage sensing channels with independently programmable time delays. The overvoltage channel has a high current Drive Output for use in conjunction with an external SCR "Crowbar" for shutdown. The undervoltage channel input comparator has hysteresis which is externally programmable, and an open-collector output for fault indication.

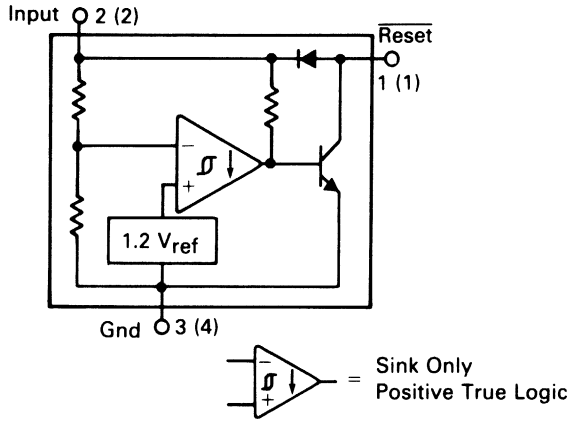


Undervoltage Sensing Circuit

MC34064P-5, D-5 — T_A = 0° to +70°C, Case 29, 751
MC33064P-5, D-5 — T_A = −40° to +85°C, Case 29, 751
MC34164P-5, D-5 — T_A = 0° to +70°C, Case 29, 751
MC33164P-5, D-5 — T_A = −40° to +85°C, Case 29, 751

The MC34064/MC34164 is a family of undervoltage sensing circuits specifically designed for use as reset controllers in microprocessor-based systems. They offer the designer an economical solution for low voltage detection with a single external resistor. Both parts feature a trimmed bandgap reference, and a comparator with precise thresholds and built-in hysteresis to prevent erratic reset operation. The MC34064 has a threshold voltage of 4.6 V, while the MC34164 threhold is at 4.3 V, and features a larger hysteresis window. The open collector reset outputs are capable of sinking in excess of 10 mA (MC34064) and 7.0 mA (MC34164). Operation is guaranteed down to 1.0 volt input with low standby current. The MC34164 is specifically designed for battery powered applications where low bias current (one/tenth of the MC34064's) is an important characteristic.

Applications include direct monitoring of the 5.0 volt MPU/logic power supply used in appliance, automotive, consumer, and industrial equipment.



Pin numbers adjacent to terminals are for the 3 pin TO-92 package.
Pin numbers in parenthesis are for the D suffix SO-8 package.

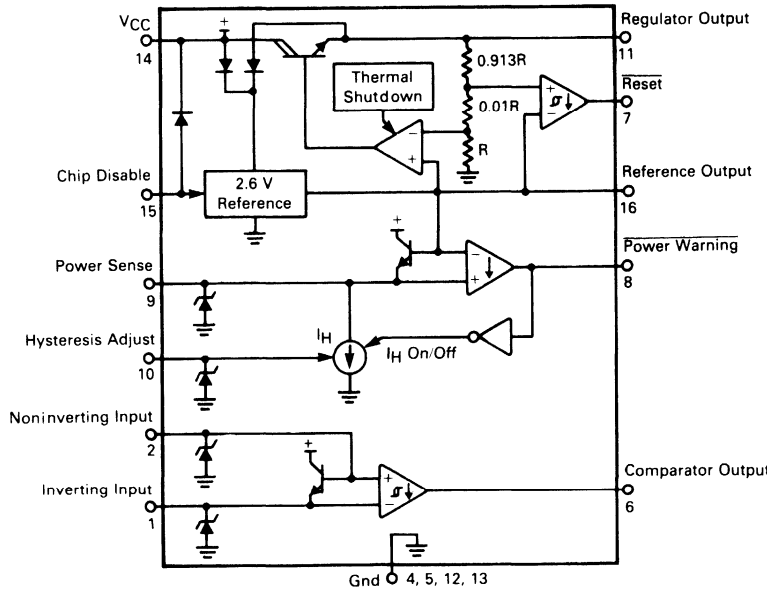
Microprocessor Voltage Regulator and Supervisory Circuit

MC34160P — T_A = 0° to +70°C, Case 648C
MC33160P — T_A = −40° to +85°C, Case 648C

The MC34160 Series is a voltage regulator and supervisory circuit containing many of the necessary monitoring functions required in microprocessor based systems. It is specifically designed for appliance and industrial applications offering the designer a cost effective solution with minimal external components. These integrated circuits feature a 5.0 V, 100 mA regulator with short circuit current limiting, pinned out 2.6 V bandgap reference, low voltage reset comparator, power warning comparator with programmable hysteresis, and an uncommitted comparator ideally suited for microprocessor line synchronization.

Additional features include a chip disable input for low standby current, and internal thermal shutdown for over temperature protection.

These devices are contained in a 16 pin dual-in-line heat tab plastic package for improved thermal conduction.



SECTION 18
REGULATOR DATA SHEETS

MOTOROLA

LM109
LM209
LM309

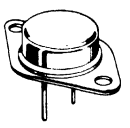
POSITIVE THREE-TERMINAL FIXED VOLTAGE REGULATORS

A versatile positive fixed +5.0-volt regulator designed for easy application as an on-card, local voltage regulator for digital logic systems. Current limiting and thermal shutdown are provided to make the units extremely rugged.

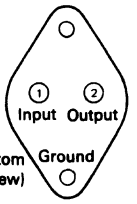
In most applications only one external component, a capacitor, is required in conjunction with the LM109 Series devices. Even this component may be omitted if the power-supply filter is not located an appreciable distance from the regulator.

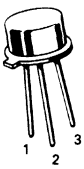
- High Maximum Output Current — Over 1.0 Ampere in K Suffix Package — Over 200 mA in H Suffix Package
- Minimum External Components Required
- Internal Short-Circuit Protection
- Internal Thermal Overload Protection
- Excellent Line and Load Transient Rejection
- Designed for Use with Popular MDTL and MTTL Logic

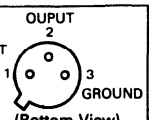
POSITIVE VOLTAGE REGULATORS



K SUFFIX
METAL PACKAGE
CASE 1-03







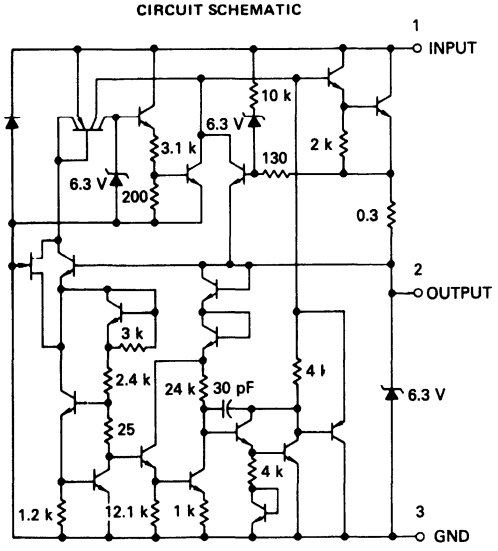
H SUFFIX
METAL PACKAGE
CASE 79-05

CASE IS GROUND

ORDERING INFORMATION

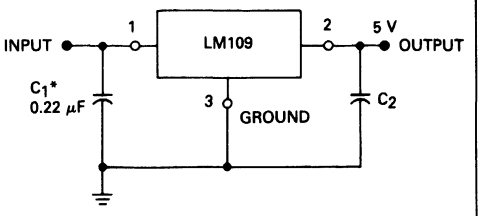
Device	Tested Operating Temperature Range	Package
LM109H	T_J = −55°C to +150°C	Metal Can
LM109K	T_J = −55°C to +150°C	Metal Power
LM209H	T_J = −25°C to +150°C	Metal Can
LM209K	T_J = −25°C to +150°C	Metal Power
LM309H	T_J = 0°C to +125°C	Metal Can
LM309K	T_J = 0°C to +125°C	Metal Power

CIRCUIT SCHEMATIC



TYPICAL APPLICATION

FIXED 5.0 V REGULATOR



*Required if regulator is located an appreciable distance from power supply filter.
Although no output capacitor is needed for stability, it does improve transient response.

LM109, LM209, LM309

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Input Voltage	V_{in}	35	Vdc
Power Dissipation	P_D	Internally Limited	
Junction Temperature Range LM109 LM209 LM309	T_J	 −55 to +150 −25 to +150 0 to +150	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C
Lead Temperature (soldering, t = 60 s)	T_S	300	°C

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	LM109/LM209[1] Min	LM109/LM209[1] Typ	LM109/LM209[1] Max	LM309[2] Min	LM309[2] Typ	LM309[2] Max	Unit
Output Voltage (T_J = +25°C)	V_O	4.7	5.05	5.3	4.8	5.05	5.2	Vdc
Input Regulation (T_J = +25°C) 7.0 ≤ V_{in} ≤ 25 V	Reg_{line}	—	4.0	50	—	4.0	50	mV
Load Regulation (T_J = +25°C) Case 1-03 5.0 mA ≤ I_O ≤ 1.5 A Case 79-03 5.0 mA ≤ I_O ≤ 0.5 A	Reg_{load}	 — —	 50 20	 100 50	 — —	 50 20	 100 50	mV
Output Voltage Range 7.0 V ≤ V_{in} ≤ 25 V 5.0 mA ≤ I_O ≤ I_{max}, P ≤ P_{max}	V_O	4.6	—	5.4	4.75	—	5.25	Vdc
Quiescent Current (7.0 V ≤ V_{in} ≤ 25 V) Quiescent Current Change (7.0 V ≤ V_{in} ≤ 25 V) 5.0 mA ≤ I_O ≤ I_{max}	I_B ΔI_B	— — —	5.2 — —	10 0.5 0.8	— — —	5.2 — —	10 0.5 0.8	mAdc
Output Noise Voltage (T_A = +25°C) 10 Hz ≤ f ≤ 100 kHz	V_N	—	40	—	—	40	—	μV
Long Term Stability	S	—	—	10	—	—	20	mV
Thermal Resistance, Junction to Case[3] Case 1-03 Case 79-03	θJC	 — —	 3.0 15	 — —	 — —	 3.0 15	 — —	°C/W

NOTES:
1. Unless otherwise specified, these specifications apply for −55°C ≤ T_J ≤ +150° (−25°C ≤ T_J ≤ +150°C for the LM209). For Case 79-03 V_{in} = 10 V, I_O = 0.1 A, I_{max} = 0.2 A and P_{max} = 2.0 W. For Case 1-03 V_{in} = 10 V, I_O = 0.5 A, I_{max} = 1.0 A and P_{max} = 20 W.
2. Unless otherwise specified, these specifications apply for 0°C ≤ T_J ≤ +125°C, V_{in} = 10 V. For Case 79-03 I_O = 0.1 A, I_{max} = 0.2 A and P_{max} = 2.0 W. For Case 1-03 I_O = 0.5 A, I_{max} = 1.0 A and P_{max} = 20 W.
3. Without a heat sink, the thermal resistance of the Case 79-03 package is about 150°C/W, while that of the Case 1-03 package is approximately 35°C/W. With a heat sink, the effective thermal resistance can only approach the values specified, depending on the efficiency of the heat sink.

TYPICAL CHARACTERISTICS

(V_{in} = 10 V, T_A = +25°C unless otherwise noted.)

FIGURE 1 – MAXIMUM AVERAGE POWER DISSIPATION (LM109K, LM209K)

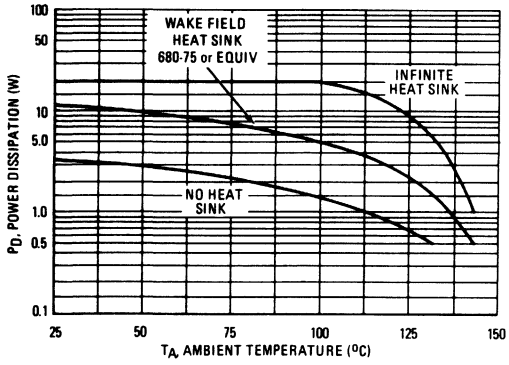
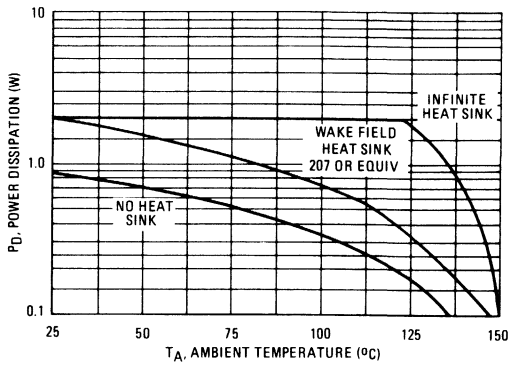


FIGURE 2 – MAXIMUM AVERAGE POWER DISSIPATION (LM109H, LM209H)



TYPICAL CHARACTERISTICS (continued)

(V_{in} = 10 V, T_A = +25°C unless otherwise noted.)

FIGURE 3 – MAXIMUM AVERAGE POWER DISSIPATION (LM309K)

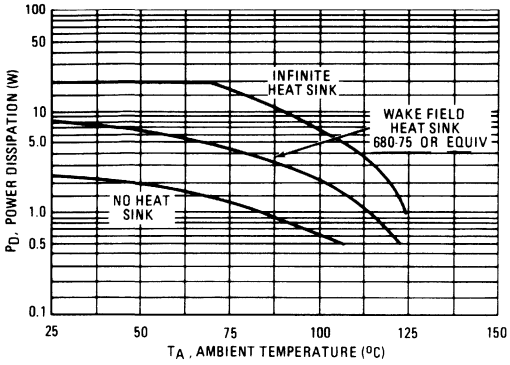


FIGURE 4 – MAXIMUM AVERAGE POWER DISSIPATION (LM309H)

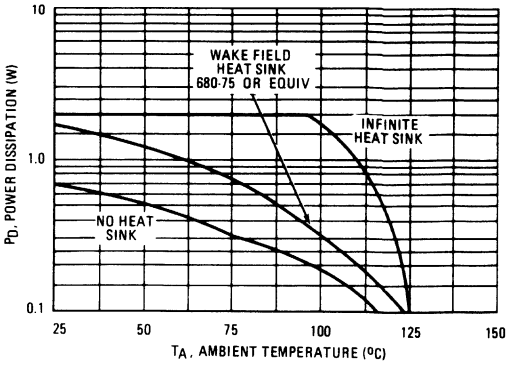


FIGURE 5 - OUTPUT IMPEDANCE versus FREQUENCY

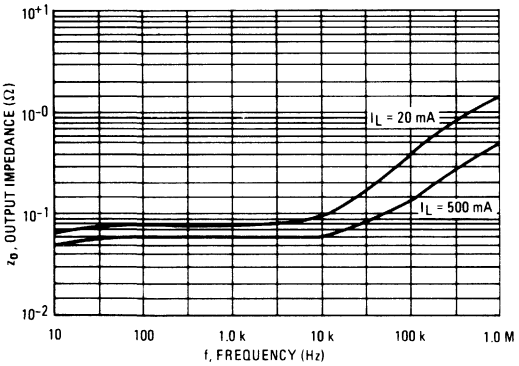


FIGURE 6 – PEAK OUTPUT CURRENT (K PACKAGE)

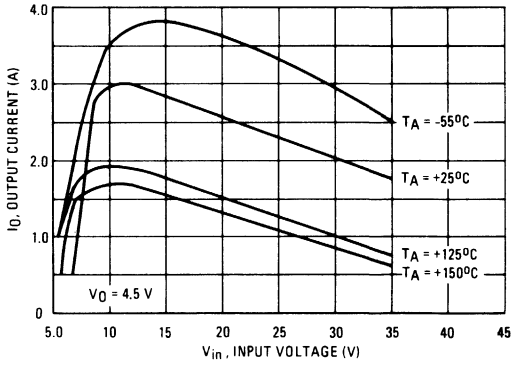


FIGURE 7 – PEAK OUTPUT CURRENT (H PACKAGE)

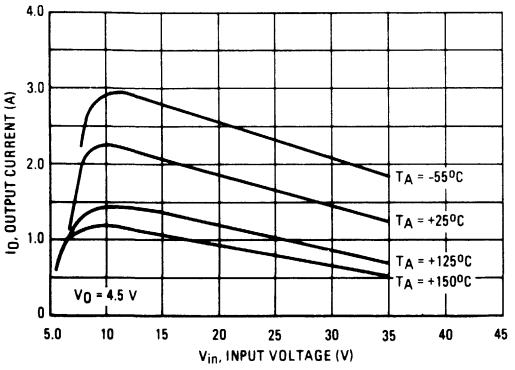
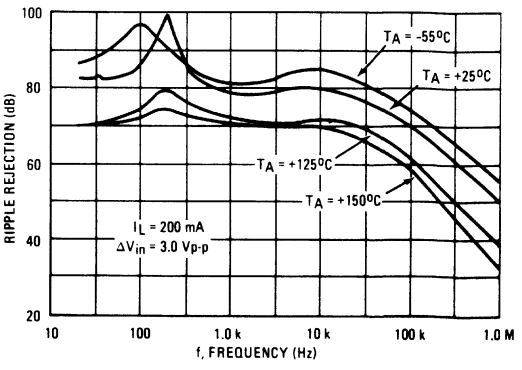


FIGURE 8 – RIPPLE REJECTION



TYPICAL CHARACTERISTICS (continued)

FIGURE 9 – DROPOUT VOLTAGE

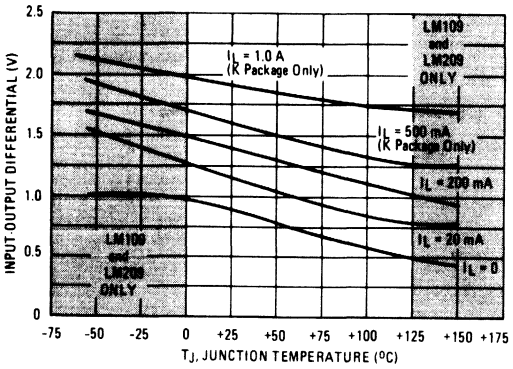


FIGURE 10 – DROPOUT CHARACTERISTIC (K PACKAGE)

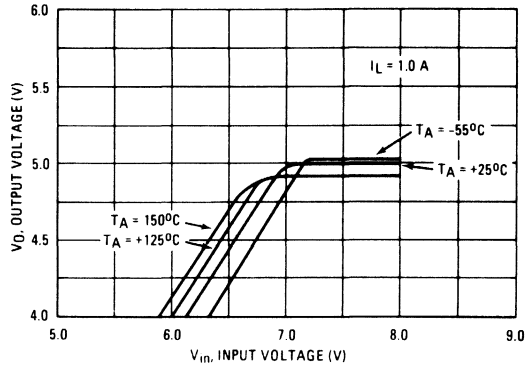


FIGURE 11 – OUTPUT VOLTAGE

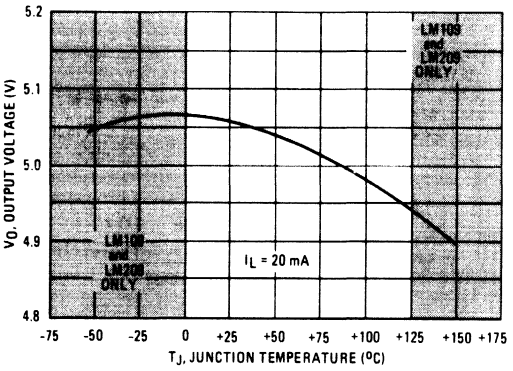


FIGURE 12 – OUTPUT NOISE VOLTAGE

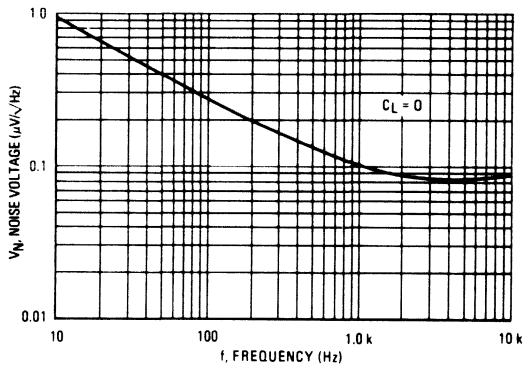


FIGURE 13 – QUIESCENT CURRENT

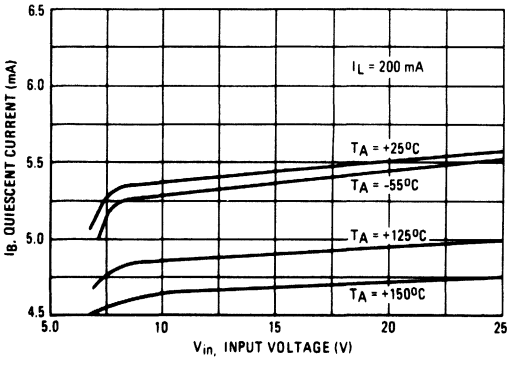
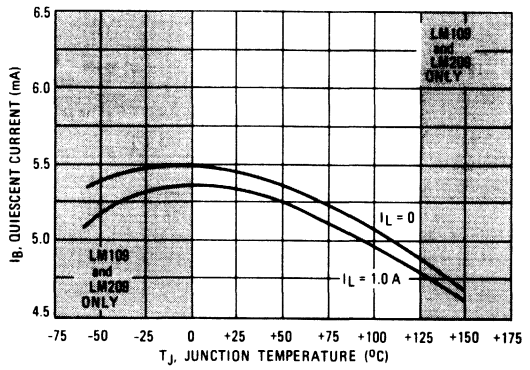


FIGURE 14 – QUIESCENT CURRENT



TYPICAL APPLICATIONS

FIGURE 15 – ADJUSTABLE OUTPUT REGULATOR

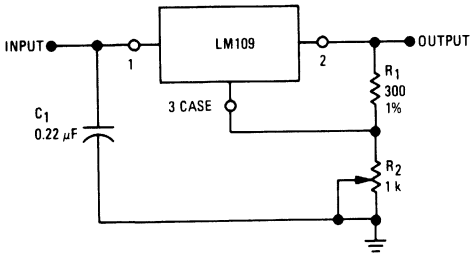
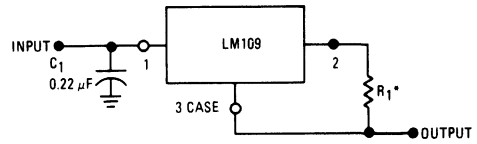


FIGURE 16 – CURRENT REGULATOR



*DETERMINES OUTPUT CURRENT.

FIGURE 17 – 5.0-VOLT, 3.0-AMPERE REGULATOR
(with plastic boost transistor)

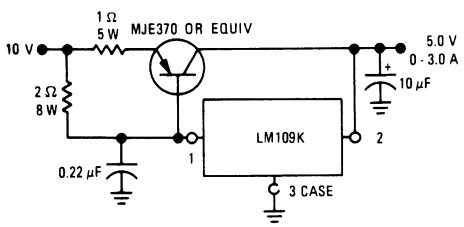


FIGURE 18 – 5.0 VOLT, 4.0-AMPERE TRANSISTOR
(with plastic Darlington boost transistor)

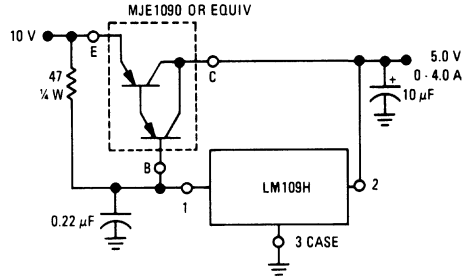


FIGURE 19 – 5.0-VOLT, 10-AMPERE REGULATOR

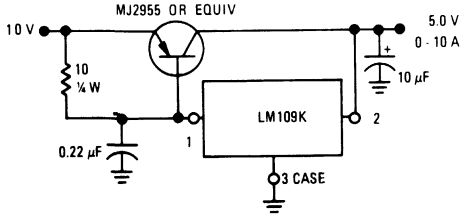
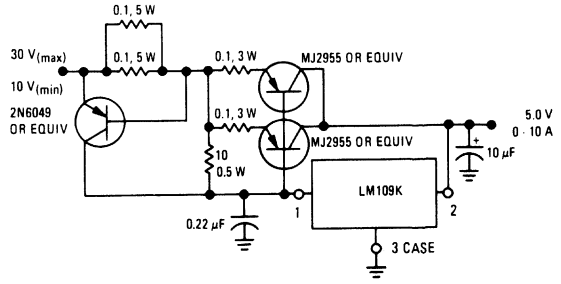


FIGURE 20 – 5.0-VOLT, 10-AMPERE REGULATOR
(with Short-Circuit Current Limiting for
Safe-Area Protection of pass transistors)



MOTOROLA

LM117
LM217
LM317

Specifications and Applications Information

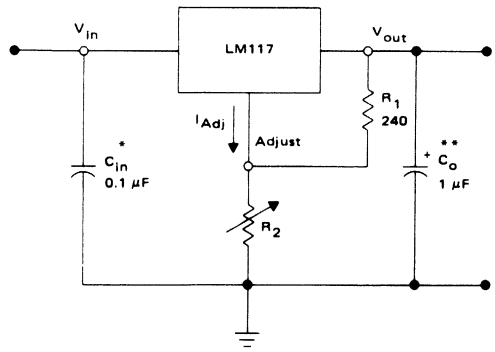
THREE-TERMINAL ADJUSTABLE OUTPUT POSITIVE VOLTAGE REGULATORS

The LM117/217/317 are adjustable 3-terminal positive voltage regulators capable of supplying in excess of 1.5 A over an output voltage range of 1.2 V to 37 V. These voltage regulators are exceptionally easy to use and require only two external resistors to set the output voltage. Further, they employ internal current limiting, thermal shutdown and safe area compensation, making them essentially blow-out proof.

The LM117 series serve a wide variety of applications including local, on card regulation. This device can also be used to make a programmable output regulator, or by connecting a fixed resistor between the adjustment and output, the LM117 series can be used as a precision current regulator.

- Output Current in Excess of 1.5 Ampere in K and T Suffix Packages
- Output Current in Excess of 0.5 Ampere in H Suffix Package
- Output Adjustable between 1.2 V and 37 V
- Internal Thermal Overload Protectiion
- Internal Short-Circuit Current Limiting Constant with Temperature
- Output Transistor Safe-Area Compensation
- Floating Operation for High Voltage Applications
- Standard 3-lead Transistor Packages
- Eliminates Stocking Many Fixed Voltages

STANDARD APPLICATION



* = C_{in} is required if regulator is located an appreciable distance from power supply filter.

** = C_o is not needed for stability, however it does improve transient response.

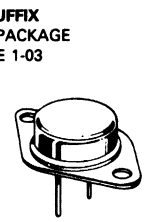
$$V_{out} = 1.25\ V\ (1 + \frac{R_2}{R_1}) + I_{Adj}\ R_2$$

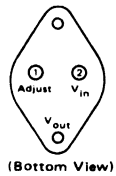
Since I_{Adj} is controlled to less than 100 μA, the error associated with this term is negligible in most applications

THREE-TERMINAL ADJUSTABLE POSITIVE VOLTAGE REGULATORS

SILICON MONOLITHIC INTEGRATED CIRCUIT

K SUFFIX
METAL PACKAGE
CASE 1-03



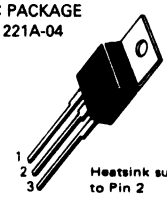


(Bottom View)

CASE IS OUTPUT

Pins 1 and 2 electrically isolated from case. Case is third electrical connection.

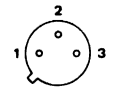
T SUFFIX
PLASTIC PACKAGE
CASE 221A-04



PIN 1. ADJUST
2. V_{out}
3. V_{in}

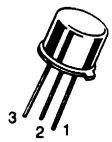
Heatsink surface connected to Pin 2

H SUFFIX
METAL PACKAGE
CASE 79-05



(Bottom View)

CASE IS OUTPUT



PIN 1. V_{in}
2. ADJUST
3. V_{out}

ORDERING INFORMATION

Device	Tested Operating Temperature Range	Package
LM117H	T_J = −55°C to +150°C	Metal Can
LM117K	T_J = −55°C to +150°C	Metal Power
LM217H	T_J = −25°C to +150°C	Metal Can
LM217K	T_J = −25°C to +150°C	Metal Power
LM317H	T_J = 0°C to +125°C	Metal Can
LM317K	T_J = 0°C to +125°C	Metal Power
LM317T	T_J = 0°C to +125°C	Plastic Power
LM317BT#	T_J = −40°C to +125°C	Plastic Power

#Automotive temperature range selections are available with special test conditions and additional tests. Contact your local Motorola sales office for information.

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Input-Output Voltage Differential	V_I-V_O	40	Vdc
Power Dissipation	P_D	Internally Limited	
Operating Junction Temperature Range LM117 LM217 LM317	T_J	 −55 to +150 −25 to +150 0 to +150	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C

ELECTRICAL CHARACTERISTICS (V_I-V_O = 5.0 V; I_O = 0.5 A for K and T packages; I_O = 0.1 A for H package; T_J = T_{low} to T_{high} [see Note 1]; I_{max} and P_{max} per Note 2; unless otherwise specified.)

Characteristic	Figure	Symbol	LM117/217 Min	LM117/217 Typ	LM117/217 Max	LM317 Min	LM317 Typ	LM317 Max	Unit
Line Regulation (Note 3) T_A = 25°C, 3.0 V ≤ V_I-V_O ≤ 40 V	1	Reg_{line}	—	0.01	0.02	—	0.01	0.04	%/V
Load Regulation (Note 3) T_A = 25°C, 10 mA ≤ I_O ≤ I_{max} V_O ≤ 5.0 V V_O ≥ 5.0 V	2	Reg_{load}	 — —	 5.0 0.1	 15 0.3	 — —	 5.0 0.1	 25 0.5	 mV % V_O
Thermal Regulation (T_A = +25°C) 20 ms Pulse		—	—	0.02	0.07	—	0.03	0.07	%/W
Adjustment Pin Current	3	I_{Adj}	—	50	100	—	50	100	μA
Adjustment Pin Current Change 2.5 V ≤ V_I-V_O ≤ 40 V 10 mA ≤ I_L ≤ I_{max}, P_D ≤ P_{max}	1,2	ΔI_{Adj}	—	0.2	5.0	—	0.2	5.0	μA
Reference Voltage (Note 4) 3.0 V ≤ V_I-V_O ≤ 40 V 10 mA ≤ I_O ≤ I_{max}, P_D ≤ P_{max}	3	V_{ref}	1.20	1.25	1.30	1.20	1.25	1.30	V
Line Regulation (Note 3) 3.0 V ≤ V_I-V_O ≤ 40 V	1	Reg_{line}	—	0.02	0.05	—	0.02	0.07	%/V
Load Regulation (Note 3) 10 mA ≤ I_O ≤ I_{max} V_O ≤ 5.0 V V_O ≥ 5.0 V	2	Reg_{load}	 — —	 20 0.3	 50 1.0	 — —	 20 0.3	 70 1.5	 mV % V_O
Temperature Stability (T_{low} ≤ T_J ≤ T_{high})	3	T_S	—	0.7	—	—	0.7	—	% V_O
Minimum Load Current to Maintain Regulation (V_I-V_O = 40 V)	3	I_{Lmin}	—	3.5	5.0	—	3.5	10	mA
Maximum Output Current V_I-V_O ≤ 15 V, P_D ≤ P_{max} K and T Packages H Package V_I-V_O = 40 V, P_D ≤ P_{max}, T_A = 25°C K and T Packages H Package	3	I_{max}	 1.5 0.5 0.25 —	 2.2 0.8 0.4 0.07	 — — — —	 1.5 0.5 0.15 —	 2.2 0.8 0.4 0.07	 — — — —	A
RMS Noise, % of V_O T_A = 25°C, 10 Hz ≤ f ≤ 10 kHz	—	N	—	0.003	—	—	0.003	—	% V_O
Ripple Rejection, V_O = 10 V, f = 120 Hz (Note 5) Without C_{Adj} C_{Adj} = 10 μF	4	RR	 — 66	 65 80	 — —	 — 66	 65 80	 — —	dB
Long-Term Stability, T_J = T_{high} (Note 6) T_A = 25°C for Endpoint Measurements	3	S	—	0.3	1.0	—	0.3	1.0	%/1.0 k Hrs.
Thermal Resistance Junction to Case H Package K Package T Package	—	$R_{\theta JC}$	 — — —	 12 2.3 —	 15 3.0 —	 — — —	 12 2.3 5.0	 15 3.0 —	°C/W

NOTES: (1) T_{low} = −55°C for LM117 T_{high} = +150°C for LM117
= −25°C for LM217 = +150°C for LM217
= 0°C for LM317 = +125°C for LM317

(2) I_{max} = 1.5 A for K and T Packages
= 0.5 A for H Package
P_{max} = 20 W for K Package
= 20 W for T Package
= 2.0 W for H Package

(3) Load and line regulation are specified at constant junction temperature. Changes in V_O due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

(4) Selected devices with tightened tolerance reference voltage available.

(5) C_{ADJ}, when used, is connected between the adjustment pin and ground.

(6) Since Long-Term Stability cannot be measured on each device before shipment, this specification is an engineering estimate of average stability from lot to lot.

SCHEMATIC DIAGRAM

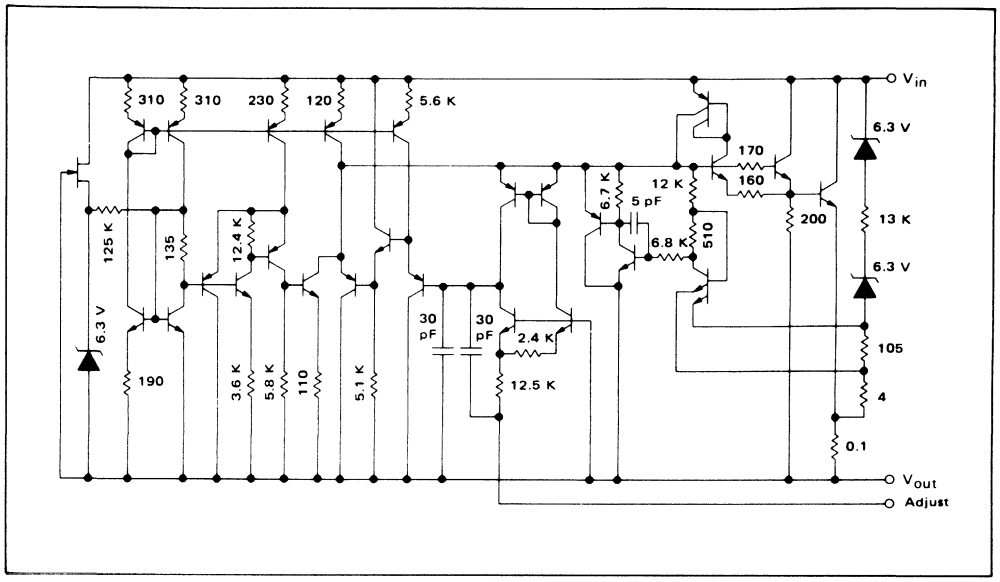


FIGURE 1 – LINE REGULATION AND ΔI_{Adj}/LINE TEST CIRCUIT

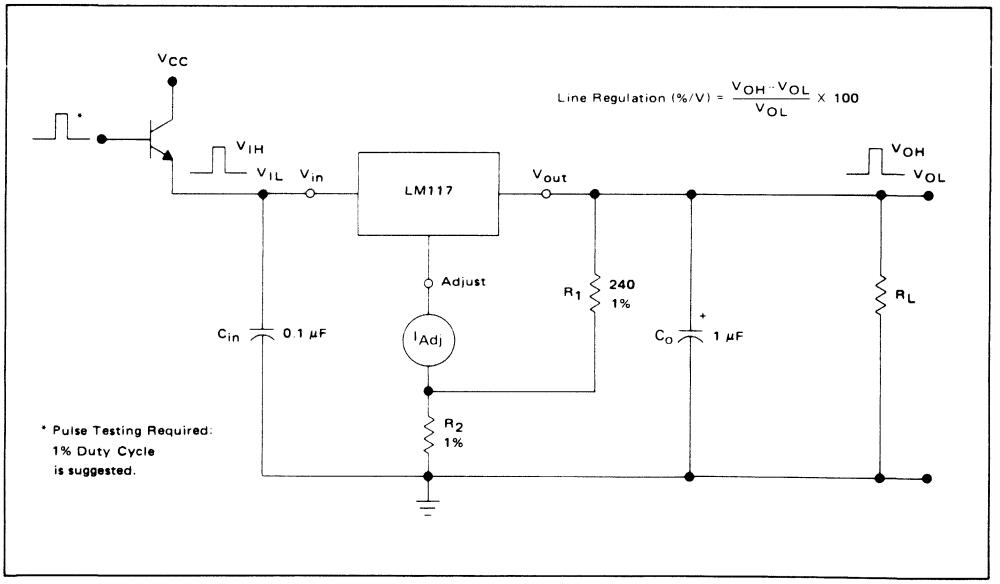


FIGURE 2 – LOAD REGULATION AND ΔI_{Adj}/LOAD TEST CIRCUIT

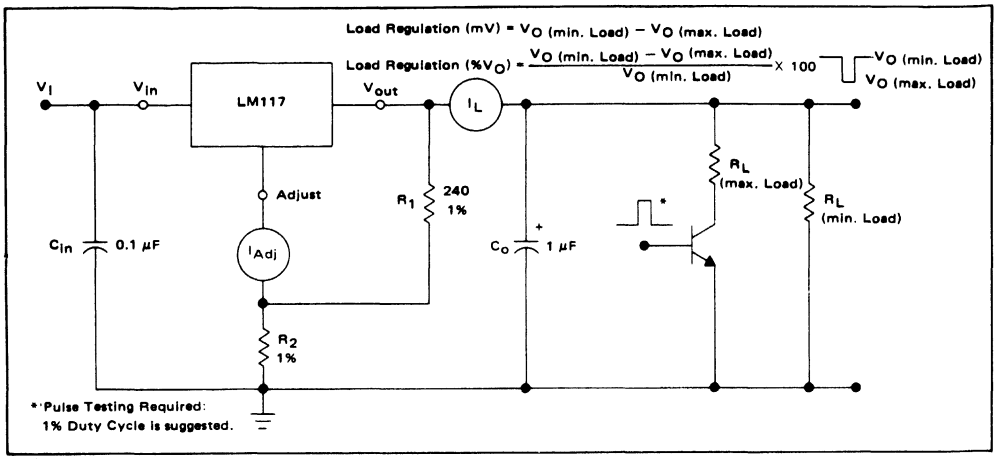


FIGURE 3 – STANDARD TEST CIRCUIT

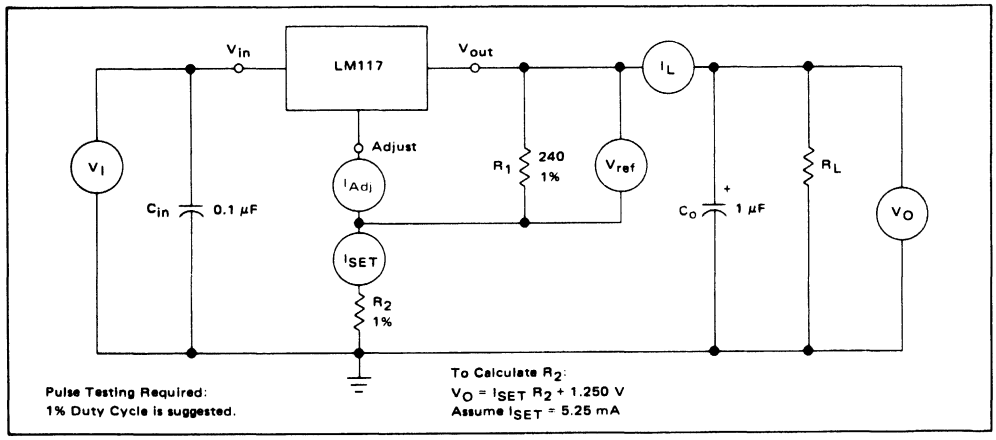


FIGURE 4 – RIPPLE REJECTION TEST CIRCUIT

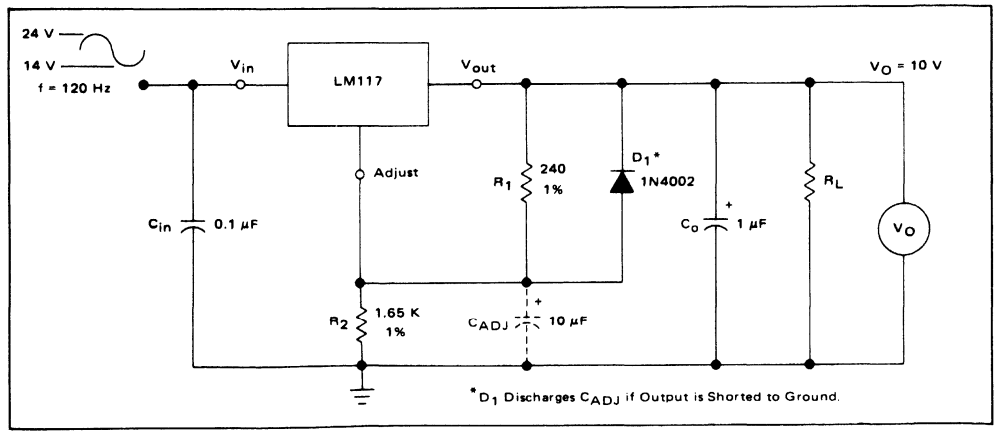


FIGURE 5 – LOAD REGULATION

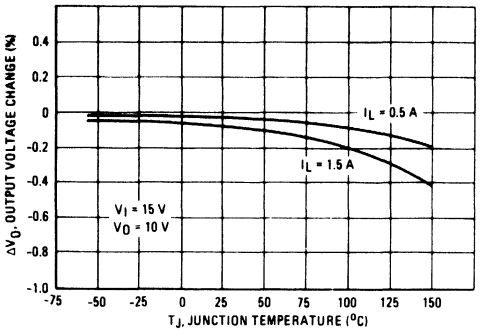


FIGURE 6 – CURRENT LIMIT

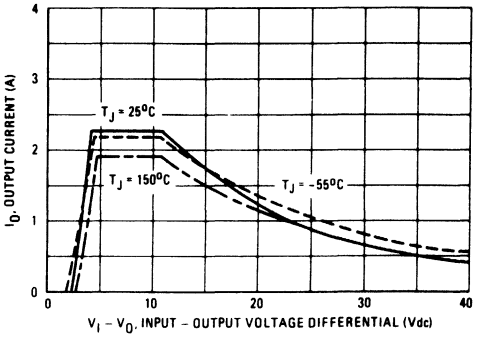


FIGURE 7 – ADJUSTMENT PIN CURRENT

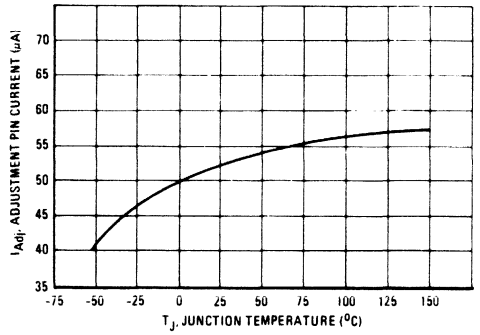


FIGURE 8 – DROPOUT VOLTAGE

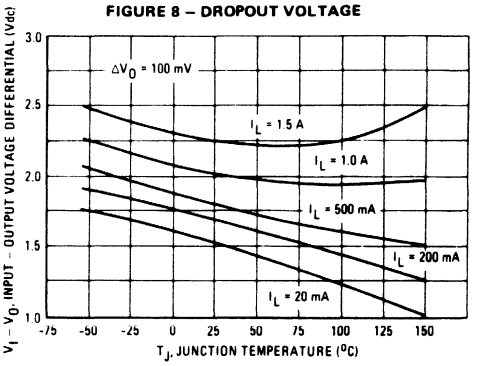


FIGURE 9 – TEMPERATURE STABILITY

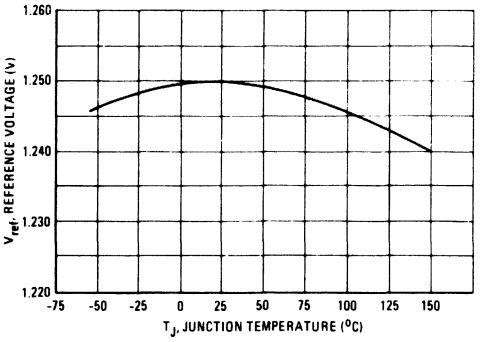


FIGURE 10 – MINIMUM OPERATING CURRENT

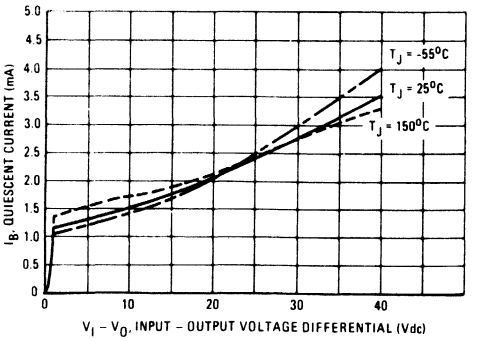


FIGURE 11 — RIPPLE REJECTION versus OUTPUT VOLTAGE

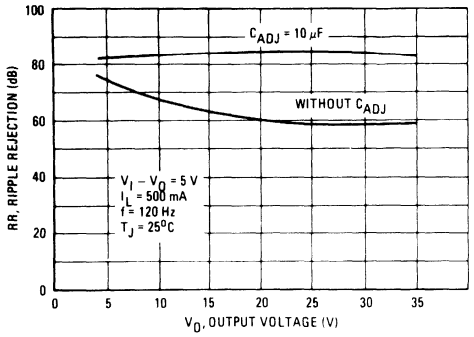


FIGURE 12 — RIPPLE REJECTION versus OUTPUT CURRENT

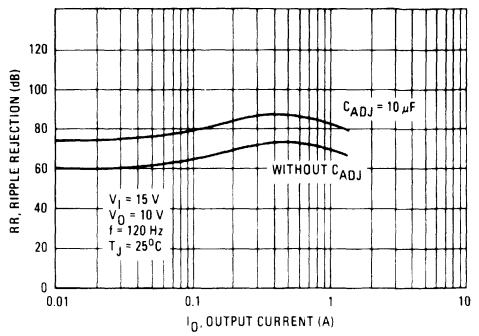


FIGURE 13 — RIPPLE REJECTION versus FREQUENCY

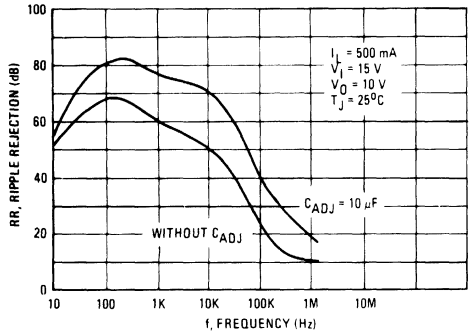


FIGURE 14 – OUTPUT IMPEDANCE

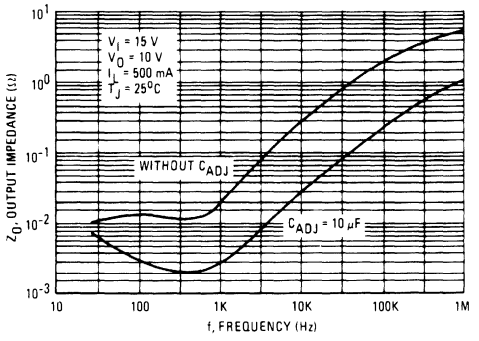


FIGURE 15 – LINE TRANSIENT RESPONSE

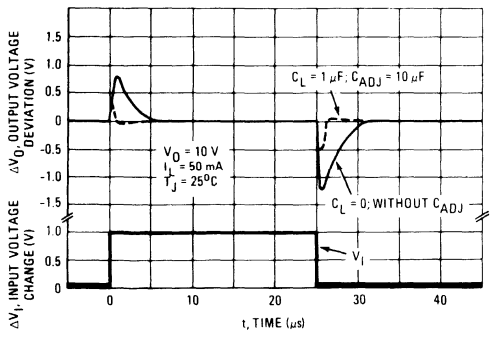
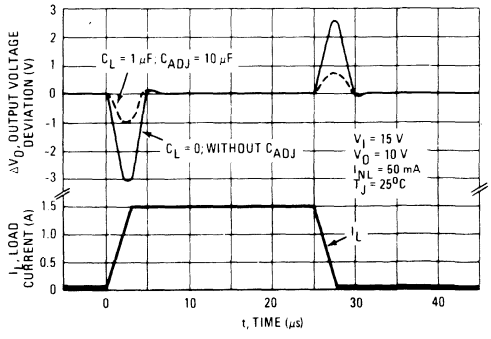


FIGURE 16 – LOAD TRANSIENT RESPONSE



APPLICATIONS INFORMATION

BASIC CIRCUIT OPERATION

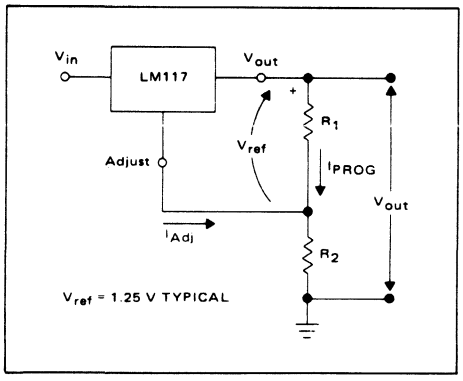
The LM117 is a 3-terminal floating regulator. In operation, the LM117 develops and maintains a nominal 1.25 volt reference (V_{ref}) between its output and adjustment terminals. This reference voltage is converted to a programming current (I_{PROG}) by R1 (see Figure 17), and this constant current flows through R2 to ground. The regulated output voltage is given by:

$$V_{out} = V_{ref}\left(1 + \frac{R2}{R1}\right) + I_{Adj}\,R2$$

Since the current from the adjustment terminal (I_{Adj}) represents an error term in the equation, the LM117 was designed to control I_{Adj} to less than 100 μA and keep it constant. To do this, all quiescent operating current is returned to the output terminal. This imposes the requirement for a minimum load current. If the load current is less than this minimum, the output voltage will rise.

Since the LM117 is a floating regulator, it is only the voltage differential across the circuit which is important to performance, and operation at high voltages with respect to ground is possible.

FIGURE 17 – BASIC CIRCUIT CONFIGURATION



LOAD REGULATION

The LM117 is capable of providing extremely good load regulation, but a few precautions are needed to obtain maximum performance. For best performance, the programming resistor (R1) should be connected as close to the regulator as possible to minimize line drops which effectively appear in series with the reference, thereby degrading regulation. The ground end of R2 can be returned near the load ground to provide remote ground sensing and improve load regulation.

EXTERNAL CAPACITORS

A 0.1 μF disc or 1 μF tantalum input bypass capacitor (C_{in}) is recommended to reduce the sensitivity to input line impedance.

The adjustment terminal may be bypassed to ground to improve ripple rejection. This capacitor (C_{ADJ}) prevents ripple from being amplified as the output voltage is increased. A 10 μF capacitor should improve ripple rejection about 15dB at 120 Hz in a 10 volt application.

Although the LM117 is stable with no output capacitance, like any feedback circuit, certain values of external capacitance can cause excessive ringing. An output capacitance (C_O) in the form of a 1 μF tantalum or 25 μF aluminum electrolytic capacitor on the output swamps this effect and insures stability.

PROTECTION DIODES

When external capacitors are used with any I.C. regulator it is sometimes necessary to add protection diodes to prevent the capacitors from discharging through low current points into the regulator.

Figure 18 shows the LM117 with the recommended protection diodes for output voltages in excess of 25 V or high capacitance values ($C_O > 25\ \mu F$, $C_{ADJ} > 10\ \mu F$). Diode D_1 prevents C_O from discharging thru the I.C. during an input short circuit. Diode D_2 protects against capacitor C_{ADJ} discharging through the I.C. during an output short circuit. The combination of diodes D1 and D2 prevents C_{ADJ} from discharging through the I.C. during an input short circuit.

FIGURE 18 – VOLTAGE REGULATOR WITH PROTECTION DIODES

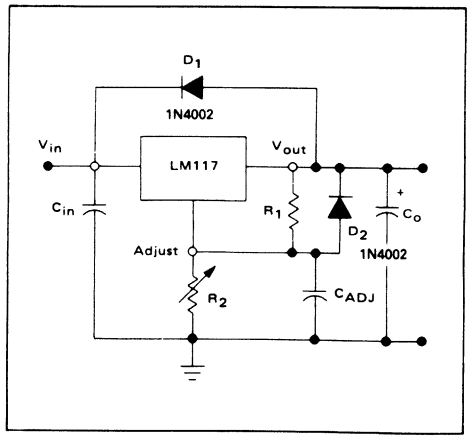


FIGURE 19 – "LABORATORY" POWER SUPPLY WITH ADJUSTABLE CURRENT LIMIT AND OUTPUT VOLTAGE

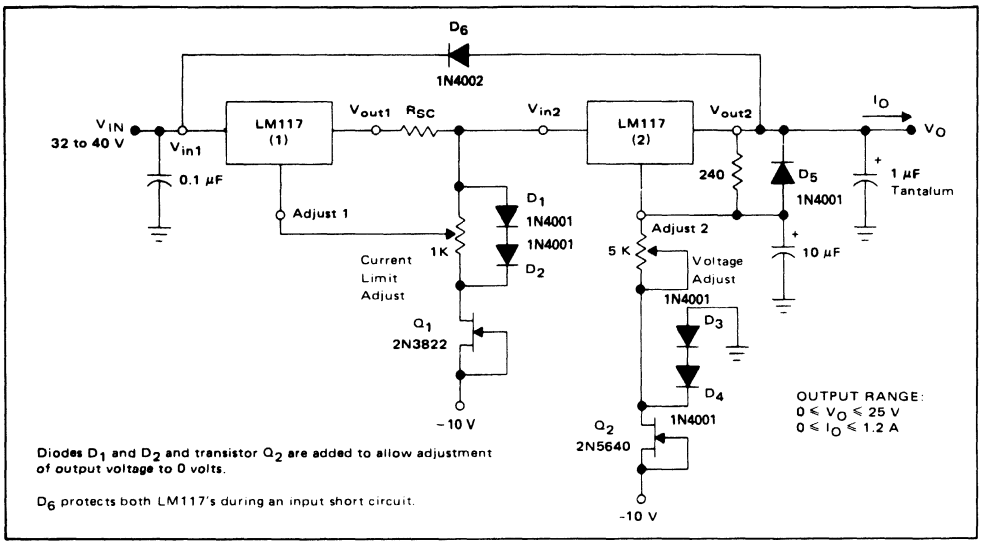


FIGURE 20 – ADJUSTABLE CURRENT LIMITER

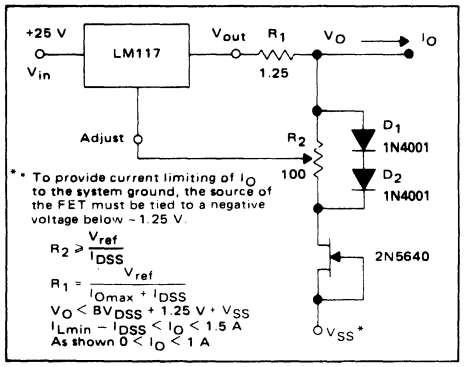


FIGURE 21 – 5 V ELECTRONIC SHUT DOWN REGULATOR

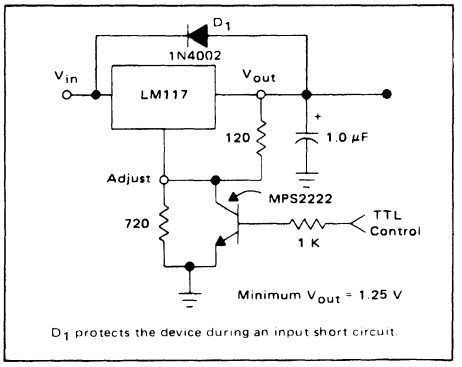


FIGURE 22 – SLOW TURN-ON REGULATOR

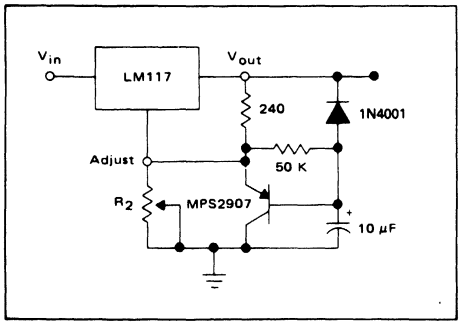
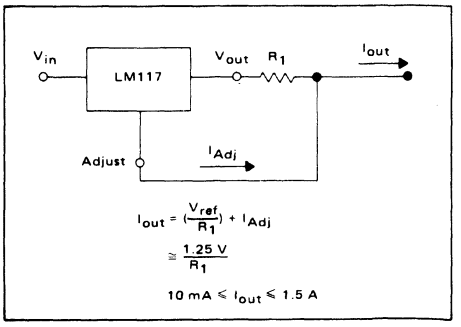


FIGURE 23 – CURRENT REGULATOR



MOTOROLA

LM117L
LM217L
LM317L

Specifications and Applications Information

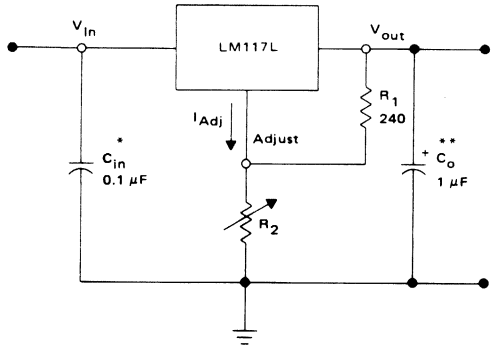
THREE-TERMINAL ADJUSTABLE OUTPUT POSITIVE VOLTAGE REGULATORS

The LM117L/217L/317L are adjustable 3-terminal positive voltage regulators capable of supplying in excess of 100 mA over an output voltage range of 1.2 V to 37 V. These voltage regulators are exceptionally easy to use and require only two external resistors to set the output voltage. Further, they employ internal current limiting, thermal shutdown and safe area compensation, making them essentially blow-out proof.

The LM117L series serves a wide variety of applications including local, on card regulation. This device can also be used to make a programmable output regulator, or by connecting a fixed resistor between the adjustment and output, the LM117L series can be used as a precision current regulator.

- Output Current in Excess of 100 mA
- Output Adjustable Between 1.2 V and 37 V
- Internal Thermal Overload Protection
- Internal Short-Circuit Current Limiting
- Output Transistor Safe-Area Compensation
- Floating Operation for High Voltage Applications
- Standard 3-Lead Transistor Packages
- Eliminates Stocking Many Fixed Voltages

STANDARD APPLICATION



* = C_{in} is required if regulator is located an appreciable distance from power supply filter.

** = C_o is not needed for stability, however it does improve transient response.

$$V_{out} = 1.25\ V\ (1 + \frac{R_2}{R_1}) + I_{Adj}\ R_2$$

Since I_{Adj} is controlled to less than 100 μA, the error associated with this term is negligible in most applications

LOW-CURRENT THREE-TERMINAL ADJUSTABLE POSITIVE VOLTAGE REGULATORS

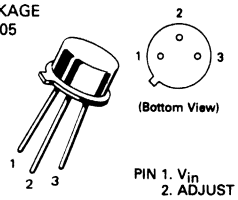
SILICON MONOLITHIC INTEGRATED CIRCUIT

Z SUFFIX
PLASTIC PACKAGE
CASE 29-04
(LM317 only)

PIN 1. ADJUST
2. V_{out}
3. V_{in}

D SUFFIX
PLASTIC PACKAGE
CASE 751-03
(SOP-8)

H SUFFIX
METAL PACKAGE
CASE 79-05



PIN 1. V_{in}
2. ADJUST
3. V_{out}

CASE
IS OUTPUT

ORDERING INFORMATION

Device	Tested Operating Temperature Range	Package
LM117LH	T_J = −55°C to +150°C	Metal Can
LM217LH	T_J = −25°C to +150°C	Metal Can
LM317LH	T_J = 0°C to +125°C	Metal Can
LM317LZ		Plastic

LM117L, LM217L, LM317L

MAXIMUM RATINGS

Rating		Symbol	Value	Unit
Input-Output Voltage Differential		V_I-V_O	40	Vdc
Power Dissipation		P_D	Internally Limited	
Operating Junction Temperature Range	LM117L LM217L LM317L	T_J	−55 to +150 −25 to +150 0 to +150	°C
Storage Temperature Range		T_{stg}	−65 to +150	°C

ELECTRICAL CHARACTERISTICS

($V_I - V_O$ = 5.0 V; I_O = 40 mA; $T_J = T_{low}$ to T_{high} [see Note 1]; I_{max} and P_{max} per Note 2; unless otherwise specified.)

Characteristic	Figure	Symbol	LM117L/217L Min	LM117L/217L Typ	LM117L/217L Max	LM317L Min	LM317L Typ	LM317L Max	Unit
Line Regulation (Note 3) T_A = 25°C, 3.0 V ≤ $V_I - V_O$ ≤ 40 V	1	Reg_{line}	—	0.01	0.02	—	0.01	0.04	%/V
Load Regulation (Note 3), T_A = 25°C 5.0 mA ≤ I_O ≤ I_{max} — LM117L/217L 10 mA ≤ I_O ≤ I_{max} — LM317L	2	Reg_{load}							
V_O ≤ 5.0 V			—	5.0	15	—	5.0	25	mV
V_O ≥ 5.0 V			—	0.1	0.3	—	0.1	0.5	% V_O
Adjustment Pin Current	3	I_{Adj}	—	50	100	—	50	100	μA
Adjustment Pin Current Change 2.5 V ≤ $V_I - V_O$ ≤ 40 V, P_D ≤ P_{max} 5.0 mA ≤ I_O ≤ I_{max} — LM117L/217L 10 mA ≤ I_O ≤ I_{max} — LM317L	1,2	ΔI_{Adj}	—	0.2	5.0	—	0.2	5.0	μA
Reference Voltage (Note 4) 3.0 V ≤ $V_I - V_O$ ≤ 40 V, P_D ≤ P_{max} 5.0 mA ≤ I_O ≤ I_{max} — LM117L/217L 10 mA ≤ I_O ≤ I_{max} — LM317L	3	V_{ref}	1.20	1.25	1.30	1.20	1.25	1.30	V
Line Regulation (Note 3) 3.0 V ≤ $V_I - V_O$ ≤ 40 V	1	Reg_{line}	—	0.02	0.05	—	0.02	0.07	%/V
Load Regulation (Note 3) 5.0 mA ≤ I_O ≤ I_{max} — LM117L/217L 10 mA ≤ I_O ≤ I_{max} — LM317L	2	Reg_{load}							
V_O ≤ 5.0 V			—	20	50	—	20	70	mV
V_O ≥ 5.0 V			—	0.3	1.0	—	0.3	1.5	% V_O
Temperature Stability (T_{low} ≤ T_J ≤ T_{high})	3	T_S	—	0.7	—	—	0.7	—	% V_O
Minimum Load Current to Maintain Regulation ($V_I - V_O$ = 40 V)	3	I_{Lmin}	—	3.5	5.0	—	3.5	10	mA
Maximum Output Current	3	I_{max}							mA
$V_I - V_O$ ≤ 20 V, P_D ≤ P_{max}, H Package			100	200	—	100	200	—	
$V_I - V_O$ ≤ 6.25 V, P_D ≤ P_{max}, Z Package			100	200	—	100	200	—	
$V_I - V_O$ = 40 V, P_D ≤ P_{max}, T_A = 25°C									
H Package			—	50	—	—	50	—	
Z Package			—	20	—	—	20	—	
RMS Noise, % of V_O T_A = 25°C, 10 Hz ≤ f ≤ 10 kHz	—	N	—	0.003	—	—	0.003	—	% V_O
Ripple Rejection (Note 5)	4	RR							dB
V_O = 1.25 V, f = 120 Hz			66	80	—	60	80	—	
C_{ADJ} = 10 μF V_O = 10.0 V			—	80	—	—	80	—	
Long Term Stability, $T_J = T_{high}$ (Note 6) T_A = 25°C for Endpoint Measurements	3	S	—	0.3	1.0	—	0.3	1.0	%/1.0 k Hrs.
Thermal Resistance Junction to Case	—	$R_{\theta JC}$							°C/W
H Package			—	40	—	—	40	—	
Z Package			—	—	—	—	83	—	
Thermal Resistance Junction to Air	—	$R_{\theta JA}$							°C/W
H Package			—	185	—	—	185	—	
Z Package			—	—	—	—	160	—	

NOTES:

(1) T_{low} = −55°C for LM117L
−25°C for LM217L
0°C for LM317L

T_{high} = +150°C for LM117L
= +150°C for LM217L
= +125°C for LM317L

(2) I_{max} = 100 mA
P_{max} = 2 W for H Package
= 625 mW for Z Package

(3) Load and line regulation are specified at constant junction temperature. Changes in V_O due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

(4) Selected devices with tightened tolerance reference voltage available.

(5) C_{ADJ}, when used, is connected between the adjustment pin and ground.

(6) Since Long Term Stability cannot be measured on each device before shipment, this specification is an engineering estimate of average stability from lot to lot.

SCHEMATIC DIAGRAM

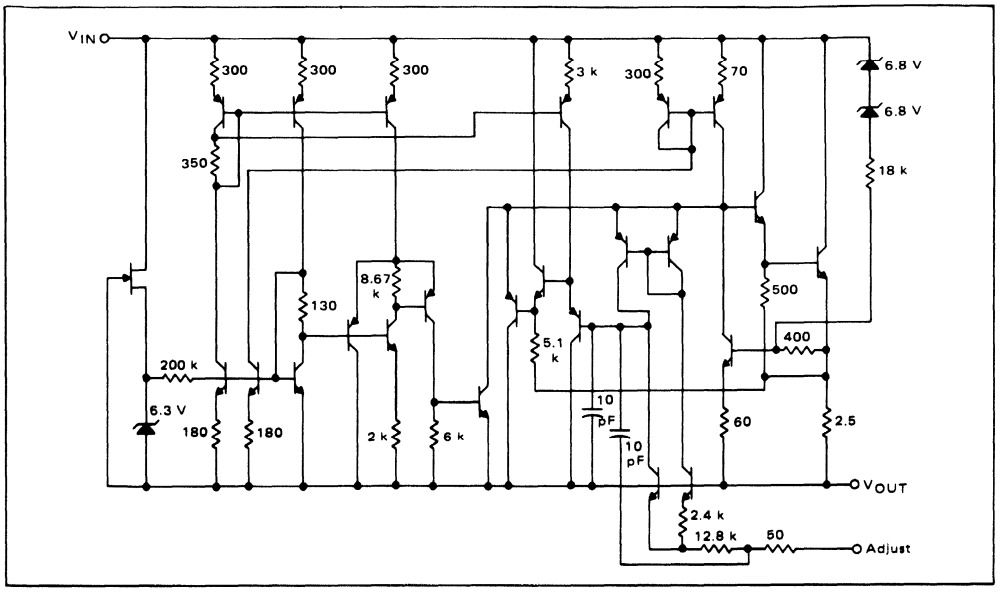


FIGURE 1 – LINE REGULATION AND ΔI_{Adj}/LINE TEST CIRCUIT

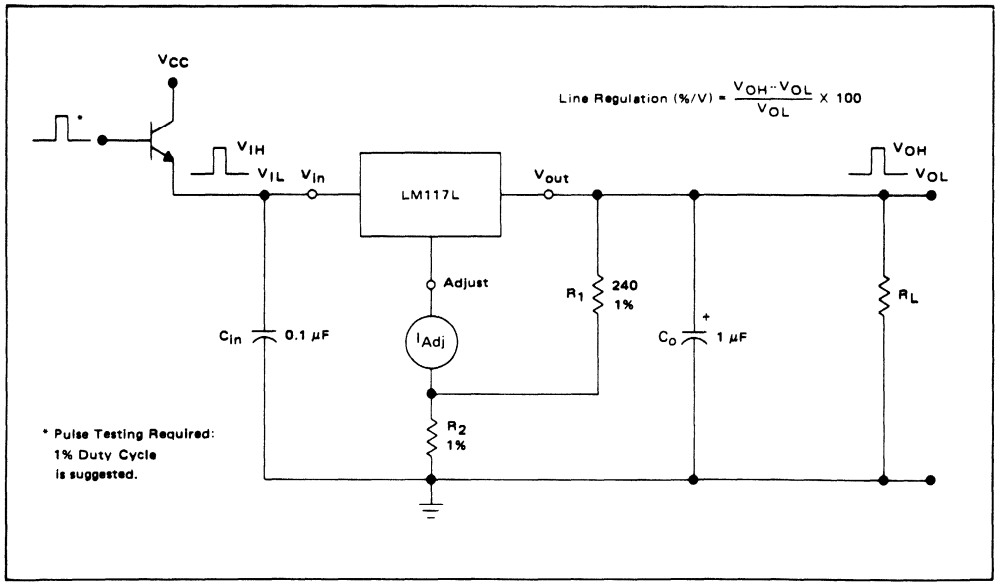


FIGURE 2 – LOAD REGULATION AND ΔI_{Adj}/LOAD TEST CIRCUIT

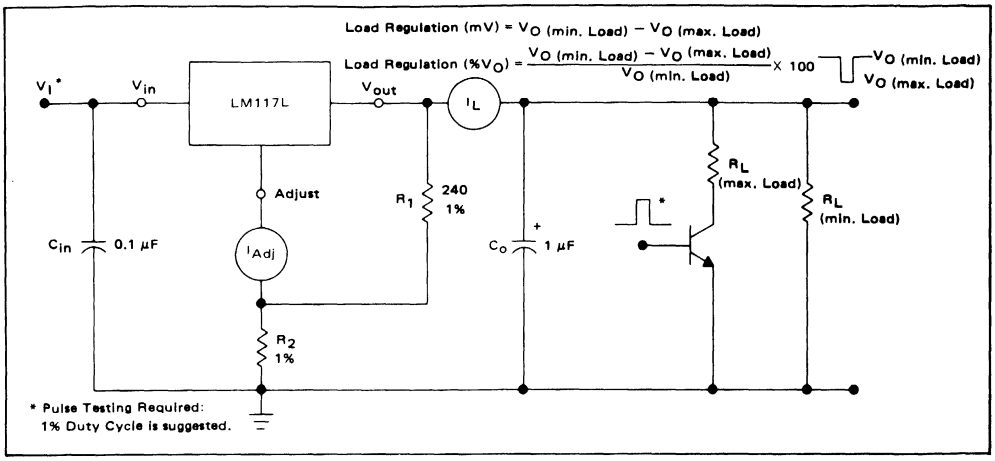


FIGURE 3 – STANDARD TEST CIRCUIT

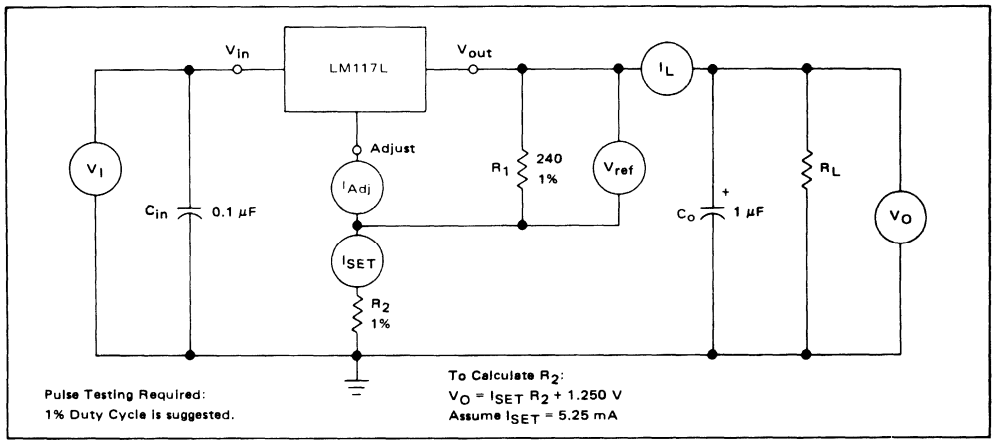


FIGURE 4 – RIPPLE REJECTION TEST CIRCUIT

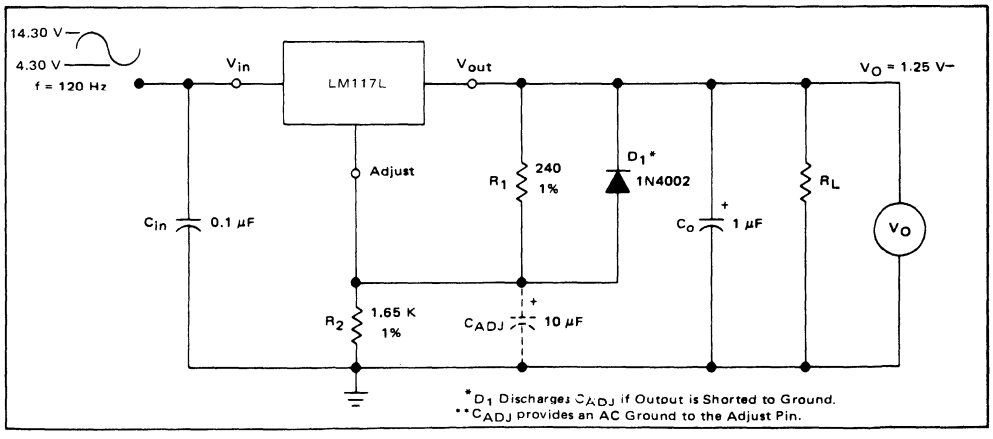


FIGURE 5 – LOAD REGULATION

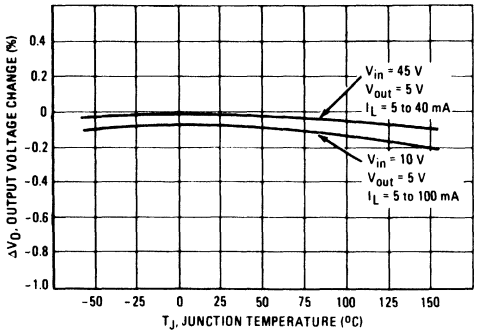


FIGURE 6 – RIPPLE REJECTION

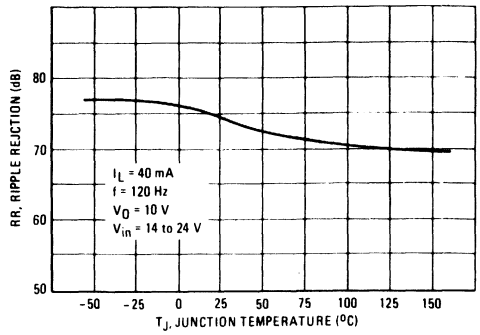


FIGURE 7 – CURRENT LIMIT

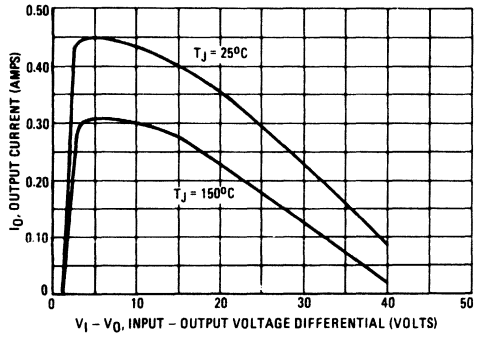


FIGURE 8 – DROPOUT VOLTAGE

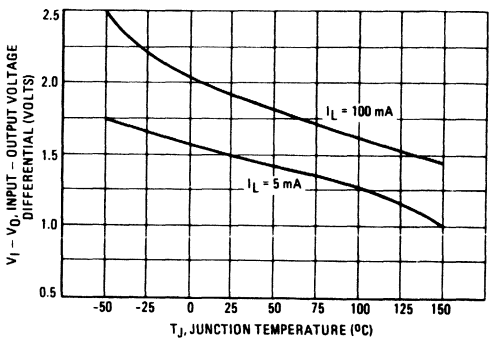


FIGURE 9 – MINIMUM OPERATING CURRENT

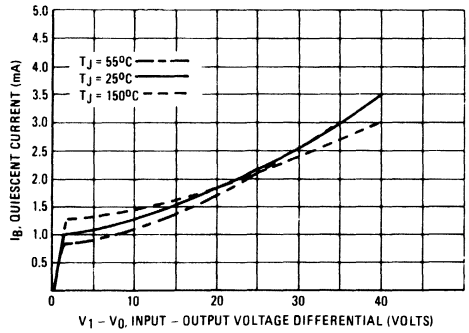


FIGURE 10 – RIPPLE REJECTION versus FREQUENCY

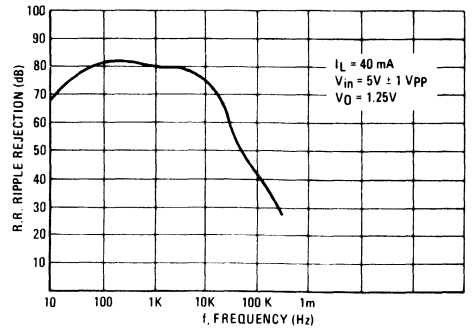


FIGURE 11 – TEMPERATURE STABILITY

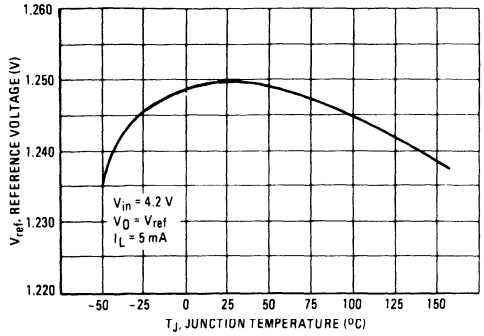


FIGURE 12 – ADJUSTMENT PIN CURRENT

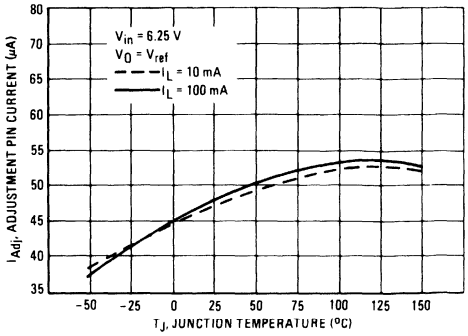


FIGURE 13 – LINE REGULATION

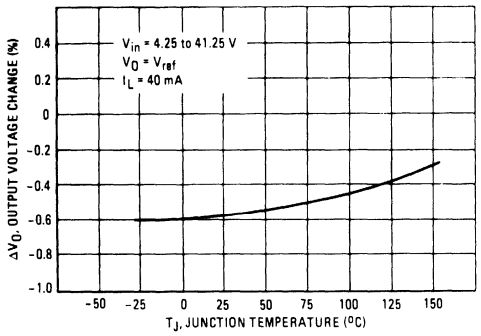


FIGURE 14 – OUTPUT NOISE

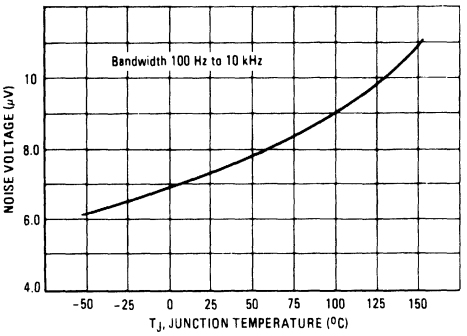


FIGURE 15 – LINE TRANSIENT RESPONSE

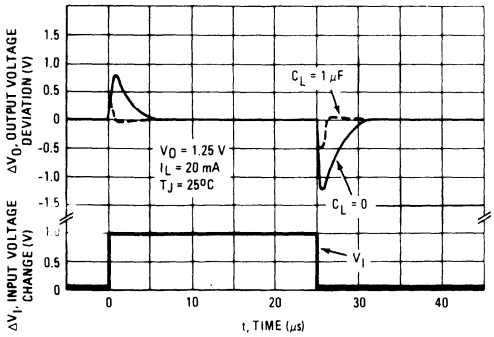
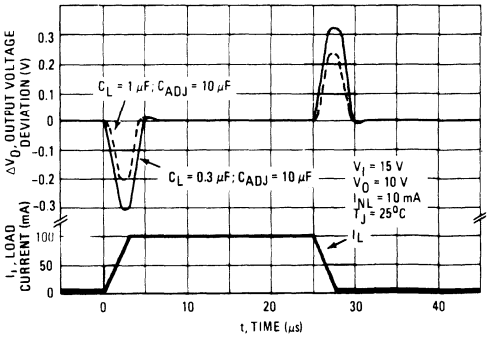


FIGURE 16 – LOAD TRANSIENT RESPONSE



APPLICATIONS INFORMATION

BASIC CIRCUIT OPERATION

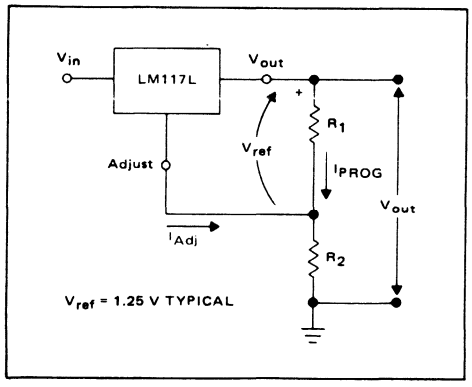
The LM117L is a 3-terminal floating regulator. In operation, the LM117L develops and maintains a nominal 1.25 volt reference (V_{ref}) between its output and adjustment terminals. This reference voltage is converted to a programming current (I_{PROG}) by R1 (see Figure 13), and this constant current flows through R2 to ground. The regulated output voltage is given by:

$$V_{out} = V_{ref}\left(1 + \frac{R2}{R1}\right) + I_{Adj}\,R2$$

Since the current from the adjustment terminal (I_{Adj}) represents an error term in the equation, the LM117L was designed to control I_{Adj} to less than 100 μA and keep it constant. To do this, all quiescent operating current is returned to the output terminal. This imposes the requirement for a minimum load current. If the load current is less than this minimum, the output voltage will rise.

Since the LM117L is a floating regulator, it is only the voltage differential across the circuit which is important to performance, and operation at high voltages with respect to ground is possible.

FIGURE 17 – BASIC CIRCUIT CONFIGURATION



LOAD REGULATION

The LM117L is capable of providing extremely good load regulation, but a few precautions are needed to obtain maximum performance. For best performance, the programming resistor (R1) should be connected as close to the regulator as possible to minimize line drops which effectively appear in series with the reference, thereby degrading regulation. The ground end of R2 can be returned near the load ground to provide remote ground sensing and improve load regulation.

EXTERNAL CAPACITORS

A 0.1 μF disc or 1 μF tantalum input bypass capacitor (C_{in}) is recommended to reduce the sensitivity to input line impedance.

The adjustment terminal may be bypassed to ground to improve ripple rejection. This capacitor (C_{ADJ}) prevents ripple from being amplified as the output voltage is increased. A 10 μF capacitor should improve ripple rejection about 15dB at 120 Hz in a 10 volt application.

Although the LM117L is stable with no output capacitance, like any feedback circuit, certain values of external capacitance can cause excessive ringing. An output capacitance (C_O) in the form of a 1 μF tantalum or 25 μF aluminum electrolytic capacitor on the output swamps this effect and insures stability.

PROTECTION DIODES

When external capacitors are used with any I.C. regulator it is sometimes necessary to add protection diodes to prevent the capacitors from discharging through low current points into the regulator.

Figure 14 shows the LM117L with the recommended protection diodes for output voltages in excess of 25 V or high capacitance values ($C_O > 10$ μF, $C_{ADJ} > 5$ μF). Diode D_1 prevents C_O from discharging thru the I.C. during an input short circuit. Diode D_2 protects against capacitor C_{ADJ} discharging through the I.C. during an output short circuit. The combination of diodes D1 and D2 prevents C_{ADJ} from discharging through the I.C. during an input short circuit.

FIGURE 18 – VOLTAGE REGULATOR WITH PROTECTION DIODES

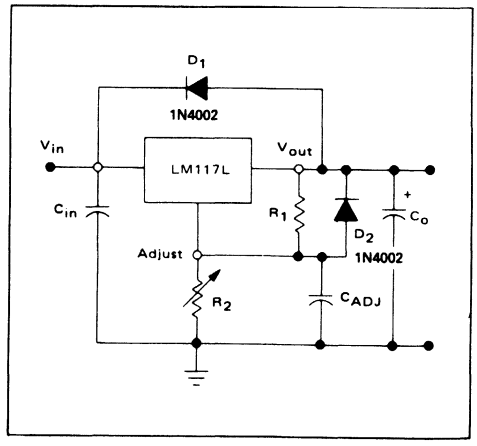


FIGURE 19 – ADJUSTABLE CURRENT LIMITER

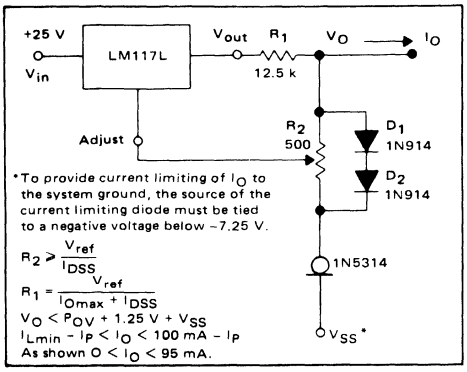


FIGURE 20 – 5 V ELECTRONIC SHUTDOWN REGULATOR

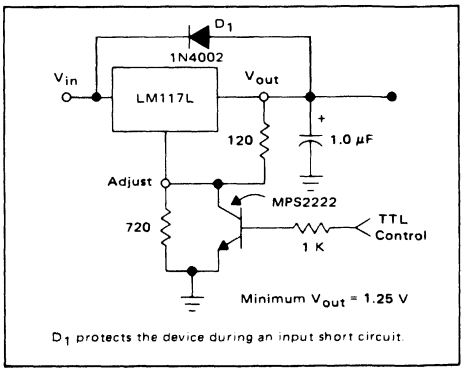


FIGURE 21 – SLOW TURN-ON REGULATOR

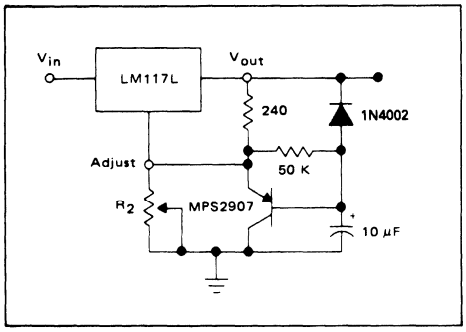
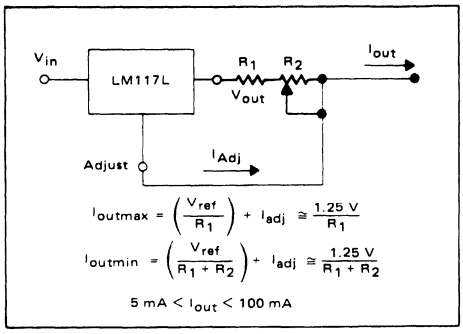


FIGURE 22 – CURRENT REGULATOR



MOTOROLA

LM123, LM123A
LM223, LM223A
LM323, LM323A

Specifications and Applications Information

3-AMPERE, 5 VOLT POSITIVE VOLTAGE REGULATORS

SILICON MONOLITHIC INTEGRATED CIRCUIT

POSITIVE VOLTAGE REGULATORS

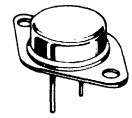
The LM123,A/LM223,A/LM323,A are a family of monolithic integrated circuits which supply a fixed positive 5.0 volt output with a load driving capability in excess of 3.0 amperes. These three-terminal regulators employ internal current limiting, thermal shutdown, and safe-area compensation. An improved series with superior electrical characteristics and a 2% output voltage tolerance is available as A-suffix (LM123A/LM223A/LM323A) device types.

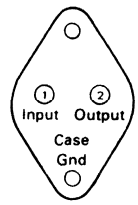
These regulators are offered in a hermetic metal power package in three operating temperature ranges. A 0°C to +125°C temperature range version is also available in a low cost plastic power package.

Although designed primarily as a fixed voltage regulator, these devices can be used with external components to obtain adjustable voltages and currents. This series of devices can be used with a series pass transistor to supply up to 15 amperes at 5.0 volts.

- Output Current in Excess of 3.0 Amperes
- Available with 2% Output Voltage Tolerance
- No external Components Required
- Internal Thermal Overload Protection
- Internal Short-Circuit Current Limiting
- Output Transistor Safe-Area Compensation
- Thermal Regulation and Ripple Rejection Have Specified Limits

K SUFFIX
METAL PACKAGE
CASE 1-03

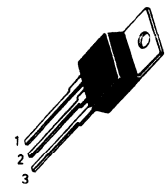




PIN 1. INPUT
2. OUTPUT
CASE GROUND

(Bottom View)

T SUFFIX
PLASTIC PACKAGE
CASE 221A-04



PIN 1. INPUT
2. GROUND
3. OUTPUT

(Heatsink surface connected to Pin 2)

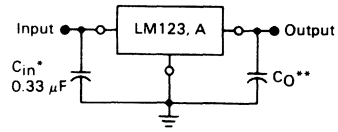
MAXIMUM RATINGS

Rating		Symbol	Value	Unit
Input Voltage		V_{in}	20	Vdc
Power Dissipation		P_D	Internally Limited	
Operating Junction Temperature Range	LM123, A LM223, A LM323, A	T_J	−55 to +150 −25 to +150 0 to +150	°C
Storage Temperature Range		T_{stg}	-65 to +150	°C
Lead Temperature (Soldering, 10 s)		T_{solder}	300	°C

ORDERING INFORMATION

Device	Output Voltage Tolerance	Tested Operating Junction Temp. Range	Package
LM123K LM123AK	6% 2%	-55 to +150°C	Metal Power
LM223K LM223AK	6% 2%	-25 to +150°C	
LM323K LM323AK	4% 2%	0 to +125°C	
LM323T LM323AT	4% 2%		Plastic Power

STANDARD APPLICATION



A common ground is required between the input and the output voltages. The input voltage must remain typically 2.5 V above the output voltage even during the low point on the input ripple voltage.

* = C_{in} is required if regulator is located an appreciable distance from power supply filter. (See Applications Information for details.)

** = C_O is not needed for stability; however, it does improve transient response.

ELECTRICAL CHARACTERISTICS ($T_J = T_{low}$ to T_{high} [see Note 1] unless otherwise specified.)

Characteristic	Symbol	LM123A/LM223A/LM323A			LM123/LM223			LM323			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Output Voltage (V_{in} = 7.5 V, 0 ≤ I_{out} ≤ 3.0 A, T_J = 25°C)	V_O	4.9	5.0	5.1	4.7	5.0	5.3	4.8	5.0	5.2	V
Output Voltage (7.5 V ≤ V_{in} ≤ 15 V, 0 ≤ I_{out} ≤ 3.0 A, P ≤ P_{max} [Note 2])	V_O	4.8	5.0	5.2	4.6	5.0	5.4	4.75	5.0	5.25	V
Line Regulation (7.5 V ≤ V_{in} ≤ 15 V, T_J = 25°C) (Note 3)	Reg_{line}	—	1.0	15	—	1.0	25	—	1.0	25	mV
Load Regulation (V_{in} = 7.5 V, 0 ≤ I_{out} ≤ 3.0 A, T_J = 25°C) (Note 3)	Reg_{load}	—	10	50	—	10	100	—	10	100	mV
Thermal Regulation (Pulse = 10 ms, P = 20 W, T_A = 25°C)	Reg_{therm}	—	0.001	0.01	—	0.002	0.03	—	0.002	0.03	%V_O/W
Quiescent Current (7.5 V ≤ V_{in} ≤ 15 V, 0 ≤ I_{out} ≤ 3.0 A)	I_B	—	3.5	10	—	3.5	20	—	3.5	20	mA
Output Noise Voltage (10 Hz ≤ f ≤ 100 kHz, T_J = 25°C)	V_N	—	40	—	—	40	—	—	40	—	μV_{rms}
Ripple Rejection (8.0 V ≤ V_{in} ≤ 18 V, I_{out} = 2.0 A, f = 120 Hz, T_J = 25°C)	RR	66	75	—	62	75	—	62	75	—	dB
Short Circuit Current Limit (V_{in} = 15 V, T_J = 25°C)	I_{SC}	—	4.5	—	—	4.5	—	—	4.5	—	A
(V_{in} = 7.5 V, T_J = 25°C)		—	5.5	—	—	5.5	—	—	5.5	—	
Long Term Stability	S	—	—	35	—	—	35	—	—	35	mV
Thermal Resistance Junction to Case (Note 4)	$R_{\theta JC}$	—	2.0	—	—	2.0	—	—	2.0	—	°C/W

Note 1. T_{low} = -55°C for LM123, A; = -25°C for LM223, A; = 0°C for LM323, A
T_{high} = +150°C for LM123, A; = +150°C for LM223, A; = +125°C for LM323, A

Note 2. Although power dissipation is internally limited, specifications apply only for P ≤ P_{max}
P_{max} = 30 W for K package
P_{max} = 25 W for T package

Note 3. Load and line regulation are specified at constant junction temperature. Pulse testing is required with a pulse width ≤ 1.0 ms and a duty cycle ≤ 5%.

Note 4. Without a heat sink, the thermal resistance ($R_{\theta JA}$ is 35°C/W for the K package, and 65°C/W for the T package. With a heat sink, the effective thermal resistance can approach the specified values of 2.0°C/W, depending on the efficiency of the heat sink.

VOLTAGE REGULATOR PERFORMANCE

The performance of a voltage regulator is specified by its immunity to changes in load, input voltage, power dissipation, and temperature. Line and load regulation are tested with a pulse of short duration (< 100 μs) and are strictly a function of electrical gain. However, pulse widths of longer duration (> 1.0 ms) are sufficient to affect temperature gradients across the die. These temperature gradients can cause a change in the output voltage, in addition to changes caused by line and load regulation. Longer pulse widths and thermal gradients make it desirable to specify thermal regulation.

Thermal regulation is defined as the change in output voltage caused by a change in dissipated power for a specified time, and is expressed as a percentage output voltage change per watt. The change in dissipated power can be caused by a change in either the input voltage or the load current. Thermal regulation is a function of I.C. layout and die attach techniques, and usually occurs within 10 ms of a change in power dissipation. After 10 ms, additional changes in the output voltage are due to the temperature coefficient of the device.

Figure 1 shows the line and thermal regulation response of a typical LM123A to a 20 watt input pulse. The variation of the output voltage due to line regulation is labeled ①. and the thermal regulation component is labeled ②. Figure 2 shows the load and thermal regulation response of a typical LM123A to a 20 watt load pulse. The output voltage variation due to load regulation is labeled ① and the thermal regulation component is labeled ②.

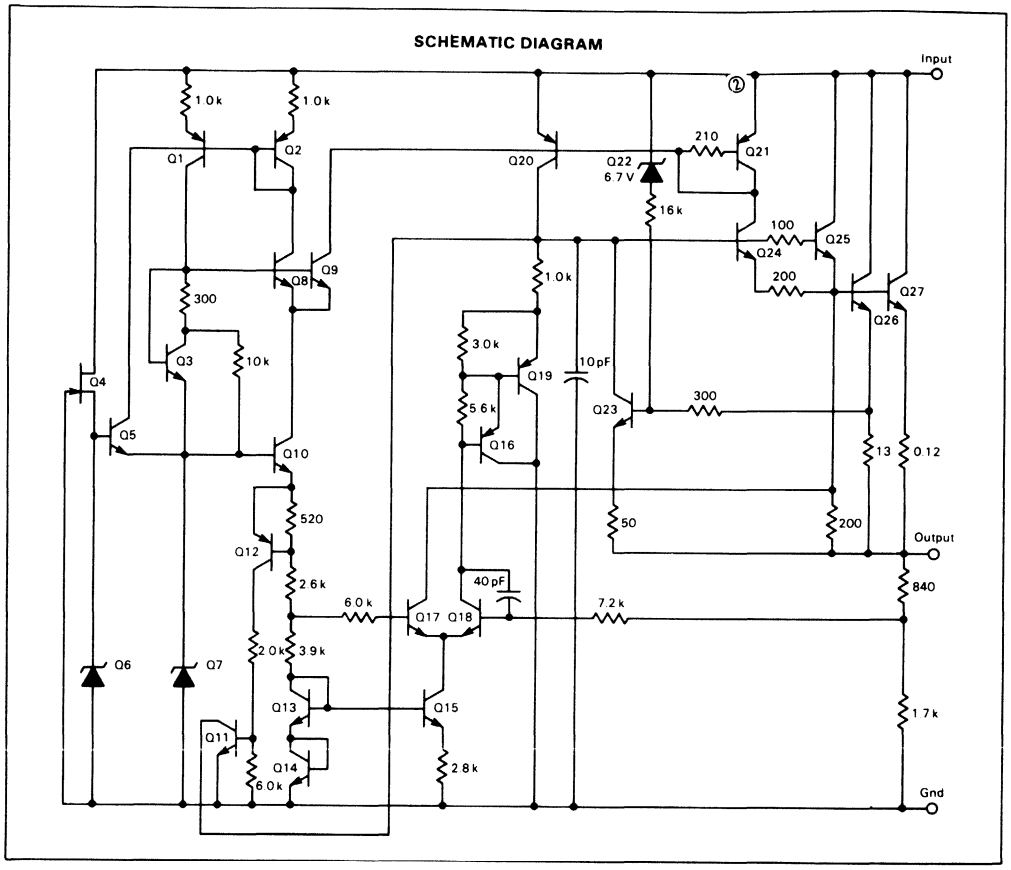
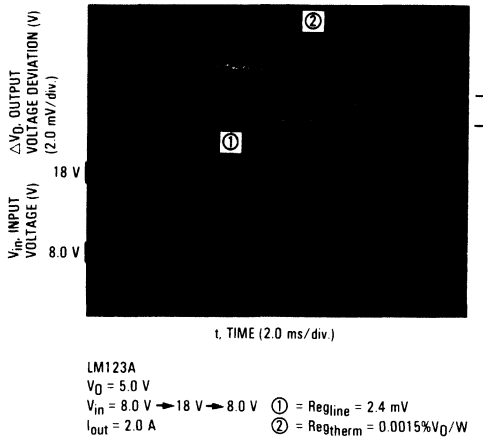
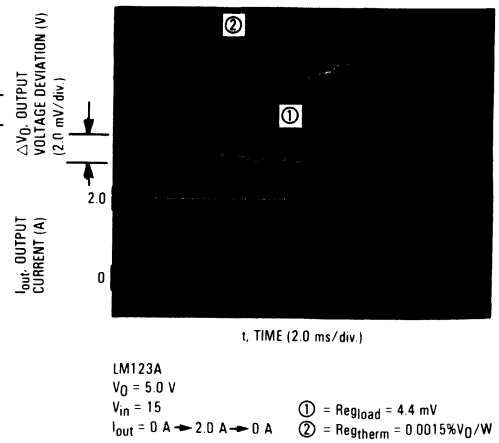


FIGURE 1 — LINE AND THERMAL REGULATION



LM123A
V_O = 5.0 V
V_{in} = 8.0 V → 18 V → 8.0 V
I_{out} = 2.0 A
① = Reg_{line} = 2.4 mV
② = Reg_{therm} = 0.0015%V_O/W

FIGURE 2 — LOAD AND THERMAL REGULATION



LM123A
V_O = 5.0 V
V_{in} = 15
I_{out} = 0 A → 2.0 A → 0 A
① = Reg_{load} = 4.4 mV
② = Reg_{therm} = 0.0015%V_O/W

FIGURE 3 — TEMPERATURE STABILITY

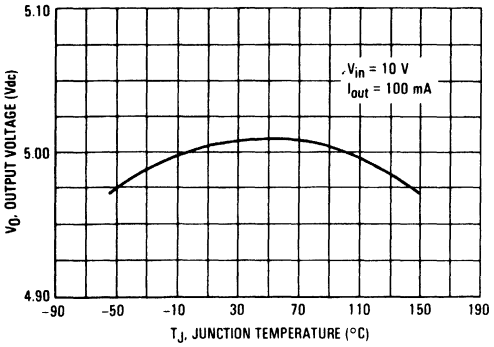


FIGURE 4 — OUTPUT IMPEDANCE

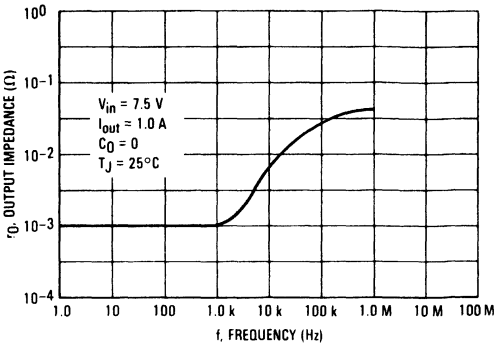


FIGURE 5 — RIPPLE REJECTION versus FREQUENCY

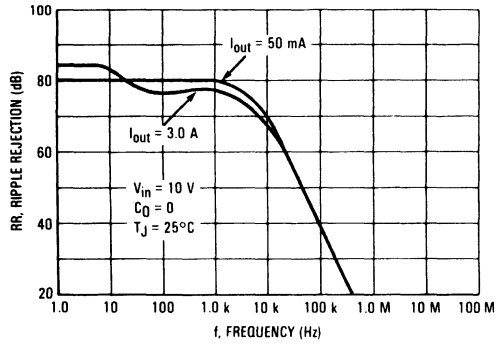


FIGURE 6 — RIPPLE REJECTION versus OUTPUT CURRENT

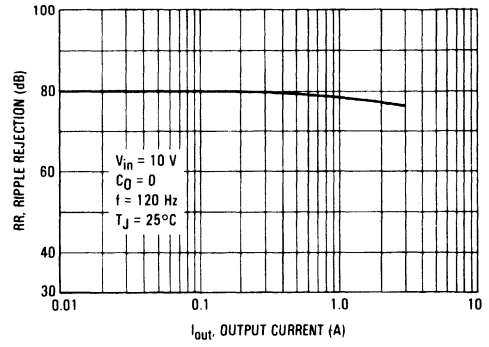


FIGURE 7 — QUIESCENT CURRENT versus INPUT VOLTAGE

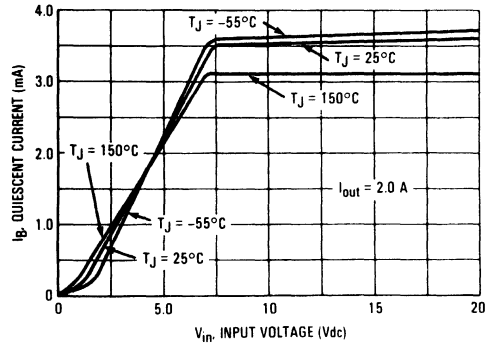


FIGURE 8 — QUIESCENT CURRENT versus OUTPUT CURRENT

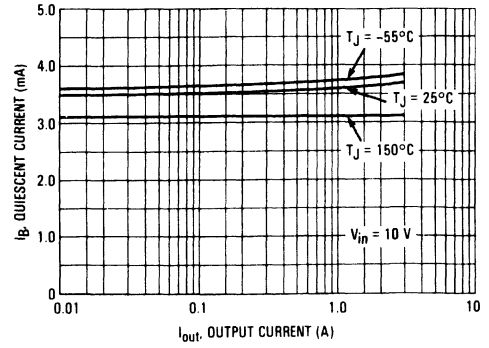


FIGURE 9 — DROPOUT VOLTAGE

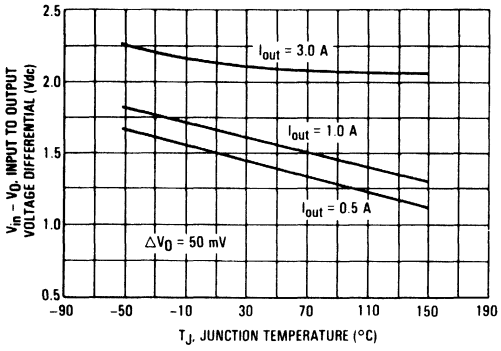


FIGURE 10 — SHORT CIRCUIT CURRENT

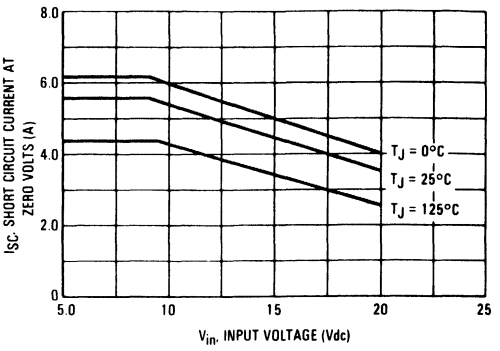


FIGURE 11 — LINE TRANSIENT RESPONSE

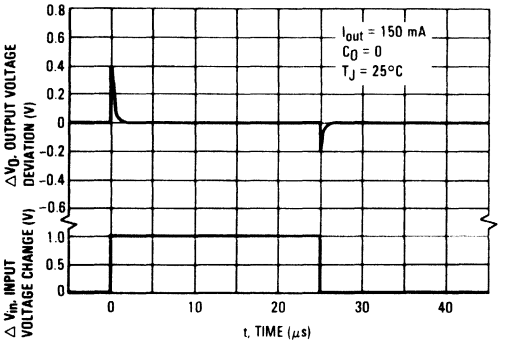


FIGURE 12 — LOAD TRANSIENT RESPONSE

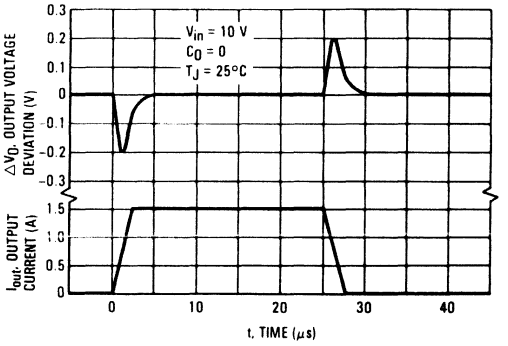


FIGURE 13 — MAXIMUM AVERAGE POWER DISSIPATION FOR LM123K and LM223K

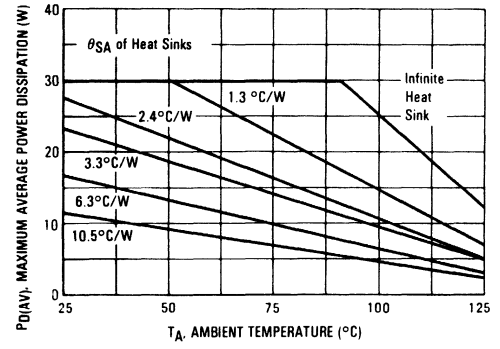
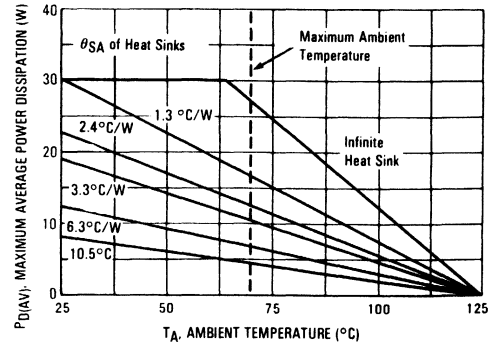


FIGURE 14 — MAXIMUM AVERAGE POWER DISSIPATION FOR LM323K



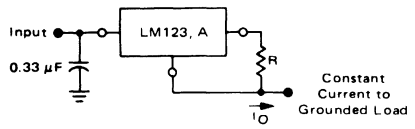
APPLICATIONS INFORMATION

Design Considerations

The LM123,A Series of fixed voltage regulators are designed with Thermal Overload Protection that shuts down the circuit when subjected to an excessive power overload condition, Internal Short-Circuit Protection that limits the maximum current the circuit will pass, and Output Transistor *Safe-Area Compensation* that reduces the output short-circuit current as the voltage across the pass transistor is increased.

In many low current applications, compensation capacitors are not required. However, it is recommended that the regulator input be bypassed with a capacitor if the regulator is connected to the power supply filter with long wire lengths, or if the output load capacitance is large. An input bypass capacitor should be selected to provide good high-frequency characteristics to insure stable operation under all load conditions. A 0.33 μF or larger tantalum, mylar, or other capacitor having low internal impedance at high frequencies should be chosen. The bypass capacitor should be mounted with the shortest possible leads directly across the regulator's input terminals. Normally good construction techniques should be used to minimize ground loops and lead resistance drops since the regulator has no external sense lead.

FIGURE 15 — CURRENT REGULATOR



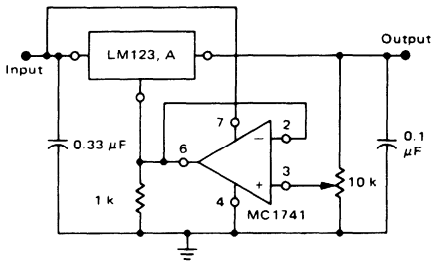
The LM123,A regulator can also be used as a current source when connected as above. Resistor R determines the current as follows:

$$I_O = \frac{5.0\ V}{R} + I_B$$

$\Delta I_B \cong 0.7$ mA over line, load and temperature changes
$I_B \cong 3.5$ mA

For example, a 2-ampere current source would require R to be a 2.5 ohm, 15 W resistor and the output voltage compliance would be the input voltage less 7.5 volts.

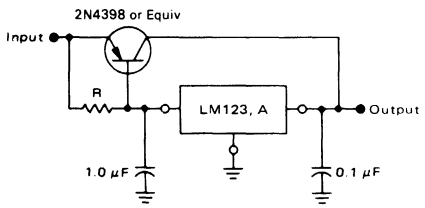
FIGURE 16 — ADJUSTABLE OUTPUT REGULATOR



V_O, 8.0 V to 20 V
$V_{in} - V_O \geq 2.5$ V

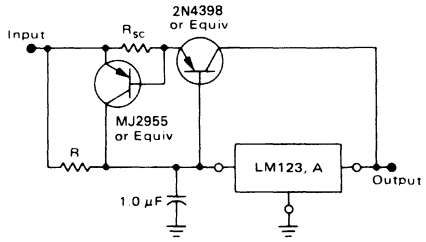
The addition of an operational amplifier allows adjustment to higher or intermediate values while retaining regulation characteristics. The minimum voltage obtainable with this arrangement is 3.0 volts greater than the regulator voltage.

FIGURE 17 — CURRENT BOOST REGULATOR



The LM123,A series can be current boosted with a PNP transistor. The 2N4398 provides current to 15 amperes. Resistor R in conjunction with the V_{BE} of the PNP determines when the pass transistor begins conducting; this circuit is not short-circuit proof. Input-output differential voltage minimum is increased by the V_{BE} of the pass transistor.

FIGURE 18 — CURRENT BOOST WITH SHORT-CIRCUIT PROTECTION



The circuit of Figure 17 can be modified to provide supply protection against short circuits by adding a short-circuit sense resistor, R_{SC}, and an additional PNP transistor. The current sensing PNP must be able to handle the short-circuit current of the three-terminal regulator. Therefore, an eight-ampere power transistor is specified.

MOTOROLA

LM137
LM237
LM337

Specifications and Applications Information

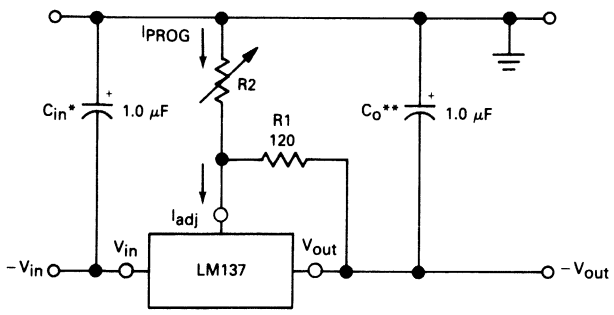
THREE-TERMINAL ADJUSTABLE OUTPUT NEGATIVE VOLTAGE REGULATORS

The LM137/237/337 are adjustable 3-terminal negative voltage regulators capable of supplying in excess of 1.5 A over an output voltage range of −1.2 V to −37 V. These voltage regulators are exceptionally easy to use and require only two external resistors to set the output voltage. Further, they employ internal current limiting, thermal shutdown and safe area compensation, making them essentially blow-out proof.

The LM137 series serve a wide variety of applications including local, on-card regulation. This device can also be used to make a programmable output regulator; or, by connecting a fixed resistor between the adjustment and output, the LM137 series can be used as a precision current regulator.

- Output Current in Excess of 1.5 Ampere in K and T Suffix Packages
- Output Current in Excess of 0.5 Ampere in H Suffix Package
- Output Adjustable Between −1.2 V and −37 V
- Internal Thermal Overload Protection
- Internal Short-Circuit-Current Limiting, Constant with Temperature
- Output Transistor Safe-Area Compensation
- Floating Operation for High Voltage Applications
- Standard 3-Lead Transistor Packages
- Eliminates Stocking Many Fixed Voltages

STANDARD APPLICATION



*C_{in} is required if regulator is located more than 4 inches from power supply filter. A 1 μF solid tantalum or 10 μF aluminum electrolytic is recommended.

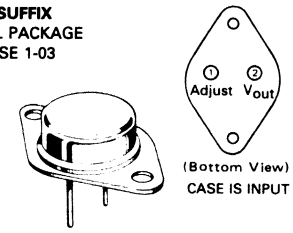
**C_O is necessary for stability. A 1 μF solid tantalum or 10 μF aluminum electrolytic is recommended.

$$V_{out} = -1.25\ V\left(1 + \frac{R2}{R1}\right)$$

THREE-TERMINAL ADJUSTABLE NEGATIVE VOLTAGE REGULATORS

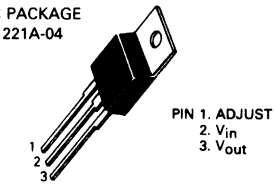
SILICON MONOLITHIC INTEGRATED CIRCUIT

K SUFFIX
METAL PACKAGE
CASE 1-03



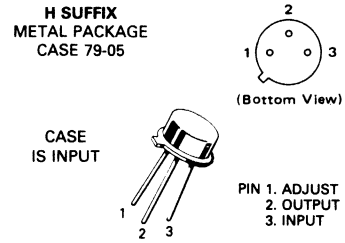
Pins 1 and 2 electrically isolated from case. Case is third electrical connection.

T SUFFIX
PLASTIC PACKAGE
CASE 221A-04



Heatsink surface connected to Pin 2

H SUFFIX
METAL PACKAGE
CASE 79-05



ORDERING INFORMATION

Device	Tested Operating Temperature Range	Package
LM137H	T_J = −55°C to +150°C	Metal Can
LM137K	T_J = −55°C to +150°C	Metal Power
LM237H	T_J = −25°C to +150°C	Metal Can
LM237K	T_J = −25°C to +150°C	Metal Power
LM337H	T_J = 0°C to +125°C	Metal Can
LM337K	T_J = 0°C to +125°C	Metal Power
LM337T	T_J = 0°C to +125°C	Plastic Power

MAXIMUM RATINGS

Rating		Symbol	Value	Unit
Input-Output Voltage Differential		V_I-V_O	40	Vdc
Power Dissipation		P_D	Internally Limited	
Operating Junction Temperature Range	LM137 LM237 LM337	T_J	−55 to +150 −25 to +150 0 to +150	°C
Storage Temperature Range		T_{stg}	−65 to +150	°C

ELECTRICAL CHARACTERISTICS ($|V_I - V_O| = 5$ V, $I_O = 0.5$ A for K and T packages; $I_O = 0.1$ A for H package; $T_J = T_{low}$ to T_{high} [see Note 1], I_{max} and P_{max} per Note 2, unless otherwise specified.)

Characteristic	Figure	Symbol	LM137/237 Min	LM137/237 Typ	LM137/237 Max	LM337 Min	LM337 Typ	LM337 Max	Unit
Line Regulation (Note 3) T_A = 25°C, 3.0 V ≤ $\|V_I-V_O\|$ ≤ 40 V	1	Reg_{line}	—	0.01	0.02	—	0.01	0.04	%/V
Load Regulation (Note 3) T_A = 25°C, 10 mA ≤ I_O ≤ I_{max}	2	Reg_{load}							
$\|V_O\|$ ≤ 5.0 V			—	15	25	—	15	50	mV
$\|V_O\|$ ≥ 5.0 V			—	0.3	0.5	—	0.3	1.0	% V_O
Thermal Regulation 10 mS Pulse, T_A = 25°C	—	Reg_{therm}	—	0.002	0.02	—	0.003	0.04	% V_O/W
Adjustment Pin Current	3	I_{Adj}	—	65	100	—	65	100	μA
Adjustment Pin Current Change 2.5 V ≤ $\|V_I-V_O\|$ ≤ 40 V 10 mA ≤ I_L ≤ I_{max}, P_D ≤ P_{max}, T_A = 25°C	1,2	ΔI_{Adj}	—	2.0	5.0	—	2.0	5.0	μA
Reference Voltage (Note 4) T_A = +25°C 3.0 V ≤ $\|V_I-V_O\|$ ≤ 40 V, 10 mA ≤ I_O ≤ I_{max}, P_D ≤ P_{max}, T_J = T_{low} to T_{high}	3	V_{ref}	−1.225 −1.20	−1.250 −1.25	−1.275 −1.30	−1.213 −1.20	−1.250 −1.25	−1.287 −1.30	V
Line Regulation (Note 3) 3.0 V ≤ $\|V_I-V_O\|$ ≤ 40 V	1	Reg_{line}	—	0.02	0.05	—	0.02	0.07	%/V
Load Regulation (Note 3) 10 mA ≤ I_O ≤ I_{max}	2	Reg_{load}							
$\|V_O\|$ ≤ 5.0 V			—	20	50	—	20	70	mV
$\|V_O\|$ ≥ 5.0 V			—	0.3	1.0	—	0.3	1.5	% V_O
Temperature Stability (T_{low} ≤ T_J ≤ T_{high})	3	T_S	—	0.6	—	—	0.6	—	% V_O
Minimum Load Current to Maintain Regulation ($\|V_I-V_O\|$ ≤ 10 V)	3	I_{Lmin}	—	1.2	3.0	—	1.5	6.0	mA
($\|V_I-V_O\|$ ≤ 40 V)			—	2.5	5.0	—	2.5	10	
Maximum Output Current $\|V_I-V_O\|$ ≤ 15 V, P_D ≤ P_{max}	3	I_{max}							A
K and T Packages			1.5	2.2	—	1.5	2.2	—	
H Package			0.5	0.8	—	0.5	0.8	—	
$\|V_I-V_O\|$ = 40 V, P_D ≤ P_{max}, T_J = 25°C									
K and T Packages			0.24	0.4	—	0.15	0.4	—	
H Package			0.15	0.20	—	0.10	0.20	—	
RMS Noise, % of V_O T_A = 25°C, 10 Hz ≤ f ≤ 10 kHz	—	N	—	0.003	—	—	0.003	—	% V_O
Ripple Rejection, V_O = −10 V, f = 120 Hz (Note 5)	4	RR							dB
Without C_{Adj}			—	60	—	—	60	—	
C_{Adj} = 10 μF			66	77	—	66	77	—	
Long-Term Stability, T_J = T_{high} (Note 6) T_A = 25°C for Endpoint Measurements	3	S	—	0.3	1.0	—	0.3	1.0	%/1.0 k Hrs.
Thermal Resistance Junction to Case	—	$R_{\theta JC}$							°C/W
H Package			—	12	15	—	12	15	
K Package			—	2.3	3.0	—	2.3	3.0	
T Package			—	—	—	—	4.0	—	

NOTES:

(1) T_{low} = −55°C for LM137 = −25°C for LM237 = 0°C for LM337
T_{high} = +150°C for LM137 = +150°C for LM237 = +125°C for LM337

(2) I_{max} = 1.5 A for K and T Packages = 0.5 A for H Package
P_{max} = 20 W for K and T Packages = 2 W for H Package

(3) Load and line regulation are specified at a constant junction temperature. Pulse testing with a low duty cycle is used. Change in V_O because of heating effects is covered under the Thermal Regulation specification.

(4) Selected devices with tightened tolerance reference voltage available.

(5) C_{adj}, when used, is connected between the adjustment pin and ground.

(6) Since Long Term Stability cannot be measured on each device before shipment, this specification is an engineering estimate of average stability from lot to lot.

(7) Power dissipation within an I.C. voltage regulator produces a temperature gradient on the die, affecting individual I.C. components on the die. These effects can be minimized by proper integrated circuit design and layout techniques. Thermal Regulation is the effect of these temperature gradients on the output voltage and is expressed in percentage of output change per watt of power change in a specified time.

SCHEMATIC DIAGRAM

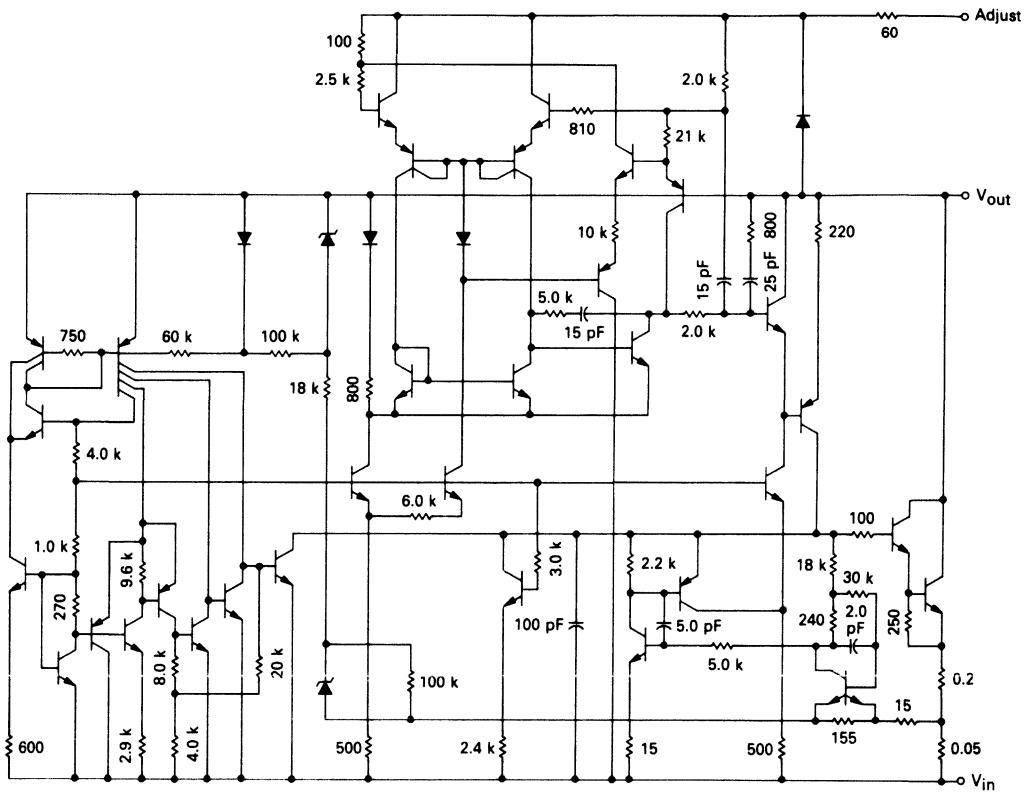


FIGURE 1 — LINE REGULATION AND ΔI_{Adj}/LINE TEST CIRCUIT

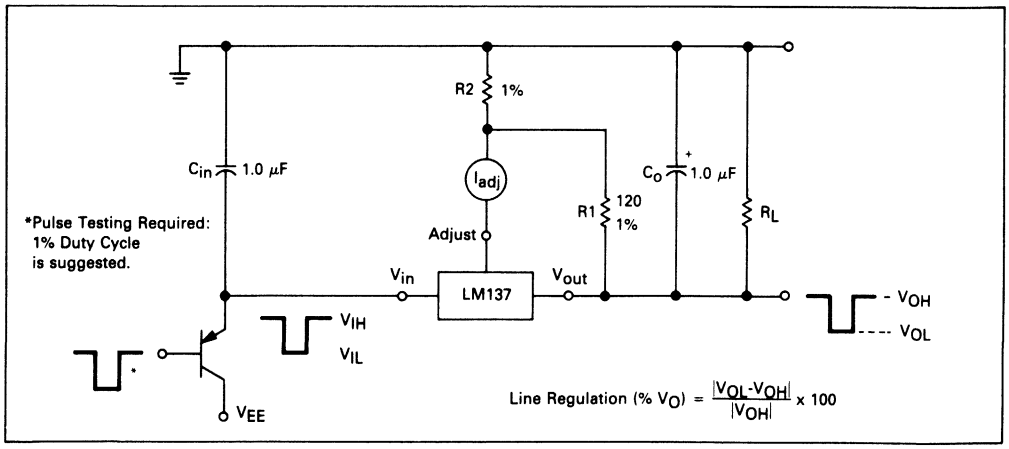


FIGURE 2 — LOAD REGULATION AND ΔI_{Adj}/LOAD TEST CIRCUIT

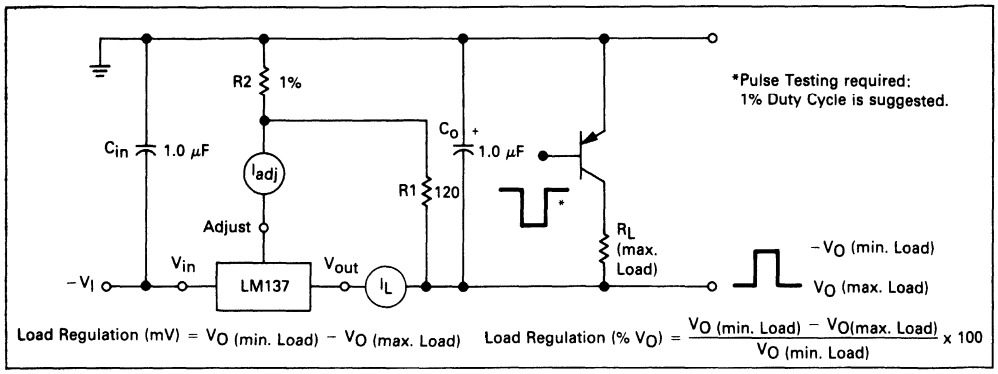


FIGURE 3 — STANDARD TEST CIRCUIT

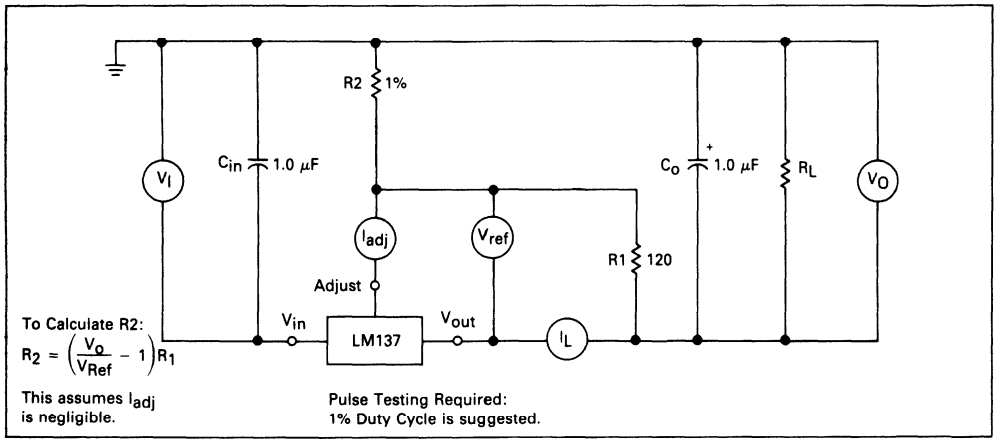


FIGURE 4 — RIPPLE REJECTION TEST CIRCUIT

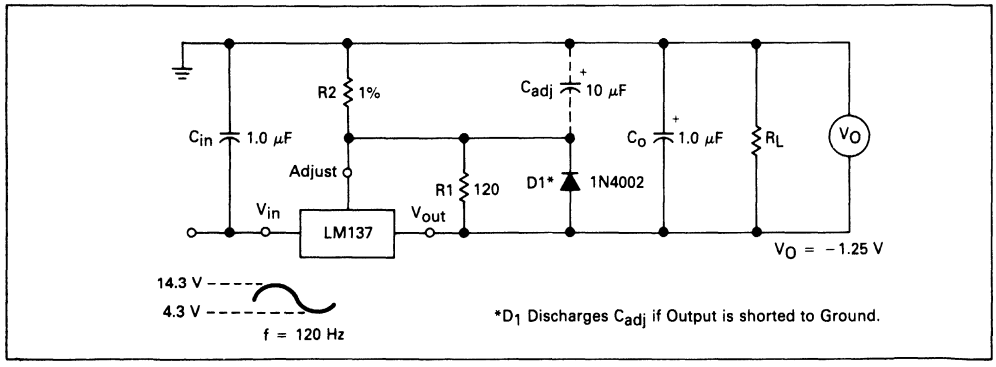


FIGURE 5 – LOAD REGULATION

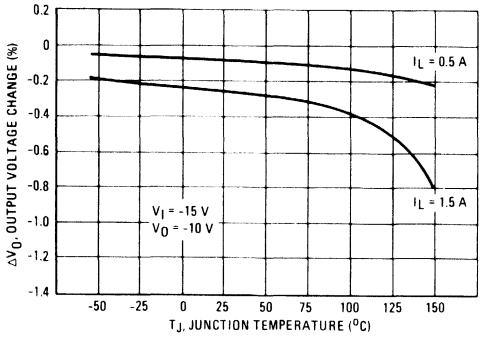


FIGURE 6 – CURRENT LIMIT

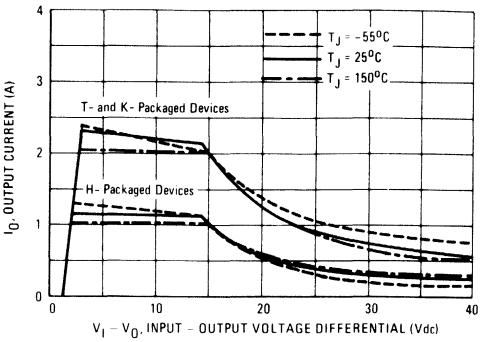


FIGURE 7 – ADJUSTMENT PIN CURRENT

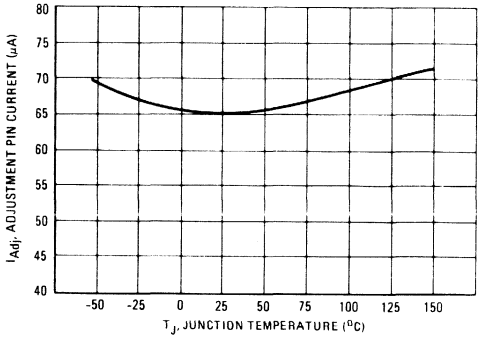


FIGURE 8 – DROPOUT VOLTAGE

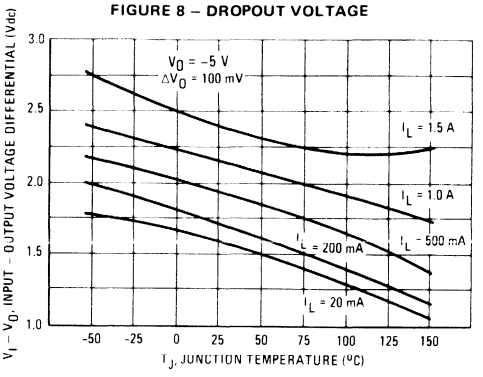


FIGURE 9 – TEMPERATURE STABILITY

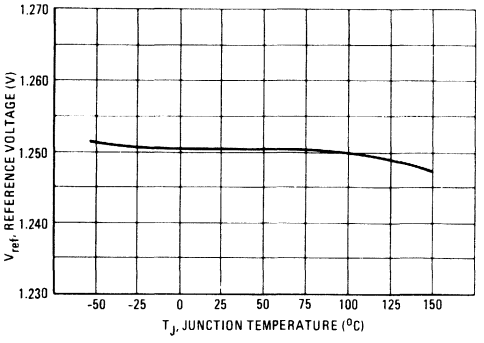


FIGURE 10 – MINIMUM OPERATING CURRENT

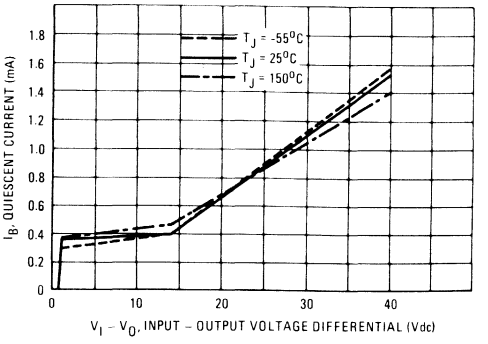


FIGURE 11 — RIPPLE REJECTION versus OUTPUT VOLTAGE

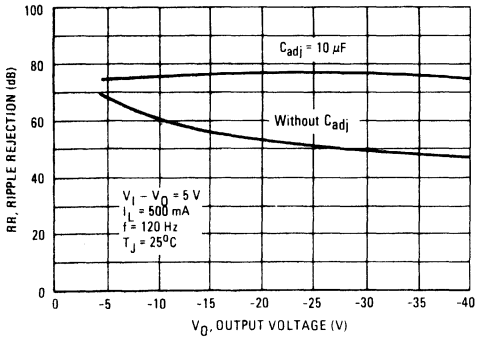


FIGURE 12 — RIPPLE REJECTION versus OUTPUT CURRENT

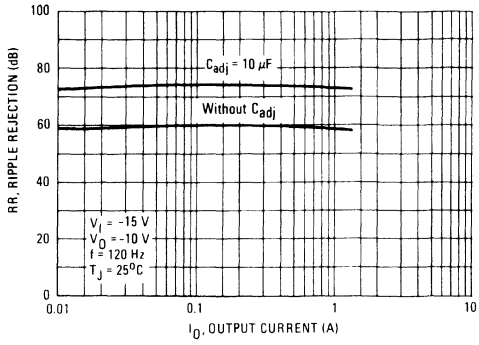


FIGURE 13 — RIPPLE REJECTION versus FREQUENCY

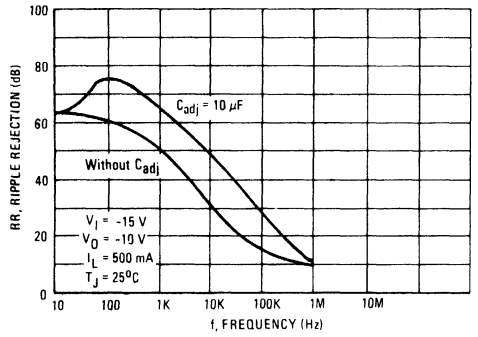


FIGURE 14 — OUTPUT IMPEDANCE

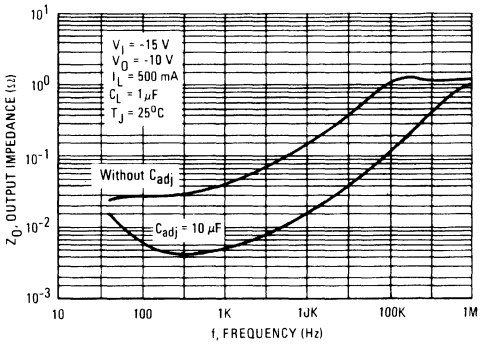


FIGURE 15 — LINE TRANSIENT RESPONSE

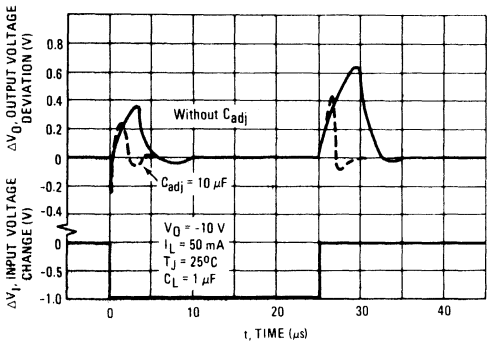
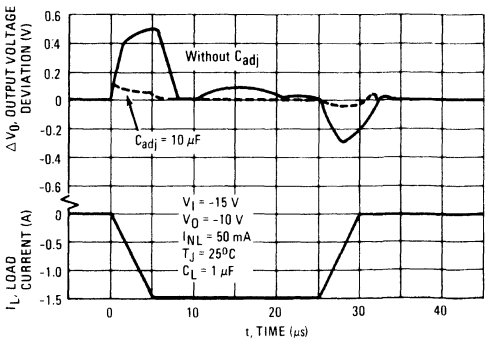


FIGURE 16 — LOAD TRANSIENT RESPONSE



APPLICATIONS INFORMATION

BASIC CIRCUIT OPERATION

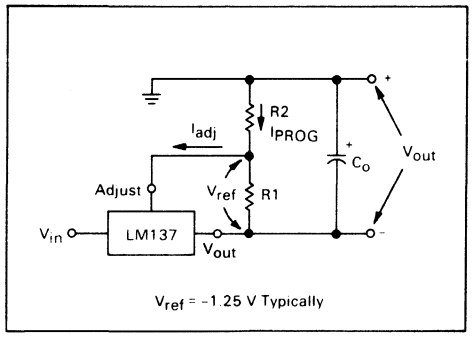
The LM137 is a 3-terminal floating regulator. In operation, the LM137 develops and maintains a nominal −1.25 volt reference (V_{ref}) between its output and adjustment terminals. This reference voltage is converted to a programming current (I_{PROG}) by R1 (see Figure 17), and this constant current flows through R2 from ground. The regulated output voltage is given by:

$$V_{out} = V_{ref}\left(1 + \frac{R2}{R1}\right) + I_{adj}\,R2$$

Since the current into the adjustment terminal (I_{adj}) represents an error term in the equation, the LM137 was designed to control I_{adj} to less than 100 μA and keep it constant. To do this, all quiescent operating current is returned to the output terminal. This imposes the requirement for a minimum load current. If the load current is less than this minimum, the output voltage will increase.

Since the LM137 is a floating regulator, it is only the voltage differential across the circuit that is important to performance, and operation at high voltages with respect to ground is possible.

FIGURE 17 – BASIC CIRCUIT CONFIGURATION



LOAD REGULATION

The LM137 is capable of providing extremely good load regulation, but a few precautions are needed to obtain maximum performance. For best performance, the programming resistor (R1) should be connected as close to the regulator as possible to minimize line drops which effectively appear in series with the reference, thereby degrading regulation. The ground end of R2 can be returned near the load ground to provide remote ground sensing and improve load regulation.

EXTERNAL CAPACITORS

A 1 μF tantalum input bypass capacitor (C_{in}) is recommended to reduce the sensitivity to input line impedance.

The adjustment terminal may be bypassed to ground to improve ripple rejection. This capacitor (C_{adj}) prevents ripple from being amplified as the output voltage is increased. A 10 μF capacitor should improve ripple rejection about 15 dB at 120 Hz in a 10 volt application.

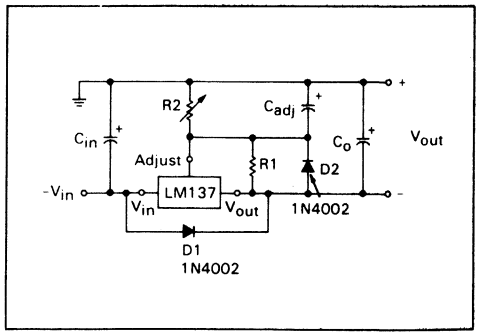
An output capacitor (C_o) in the form of a 1 μF tantalum or 10 μF aluminum electrolytic capacitor is required for stability.

PROTECTION DIODES

When external capacitors are used with any I.C. regulator it is sometimes necessary to add protection diodes to prevent the capacitors from discharging through low current points into the regulator.

Figure 18 shows the LM137 with the recommended protection diodes for output voltages in excess of −25 V or high capacitance values (C_o > 25 μF, C_{adj} > 10 μF). Diode D_1 prevents C_o from discharging thru the I.C. during an input short circuit. Diode D_2 protects against capacitor C_{adj} discharging through the I.C. during an output short circuit. The combination of diodes D1 and D2 prevents C_{adj} from discharging through the I.C. during an input short circuit.

FIGURE 18 – VOLTAGE REGULATOR WITH PROTECTION DIODES



MOTOROLA

LM140,A Series
LM340,A Series

Specifications and Applications Information

THREE-TERMINAL POSITIVE VOLTAGE REGULATORS

This family of fixed voltage regulators are monolithic integrated circuits capable of driving loads in excess of 1.0 ampere. These three-terminal regulators employ internal current limiting, thermal shutdown, and safe-area compensation. Devices are available with improved specifications, including a 2% output voltage tolerance, on A-suffix 5.0, 12 and 15 volt device types.

Although designed primarily as a fixed voltage regulator, these devices can be used with external components to obtain adjustable voltages and currents. This series of devices can be used with a series-pass transistor to boost output current capability at the nominal output voltage.

- Output Current in Excess of 1.0 Ampere
- No External Components Required
- Output Voltage Offered in 2% and 4% Tolerance*
- Internal Thermal Overload Protection
- Internal Short-Circuit Current Limiting
- Output Transistor Safe-Area Compensation

ORDERING INFORMATION

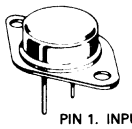
Device	Output Voltage and Tolerance	Tested Operating Junction Temp. Range	Package
LM140K-5.0	5.0 V ± 4%	−55°C to +150°C	Metal Power
LM140AK-5.0	5.0 V ± 2%	−55°C to +150°C	Metal Power
LM140K-8.0	8.0 V ± 4%	−55°C to +150°C	Metal Power
LM140K-12	12 V ± 4%	−55°C to +150°C	Metal Power
LM140AK-12	12 V ± 2%	−55°C to +150°C	Metal Power
LM140K-15	15 V ± 4%	−55°C to +150°C	Metal Power
LM140AK-15	15 V ± 2%	−55°C to +150°C	Metal Power
LM340K-5.0	5.0 V ± 4%	0°C to +125°C	Metal Power
LM340AK-5.0	5.0 V ± 2%	0°C to +125°C	
LM340T-5.0	5.0 V ± 4%	0°C to +125°C	Plastic Power
LM340AT-5.0	5.0 V ± 2%	0°C to +125°C	
LM340T-6.0	6.0 V ± 4%	0°C to +125°C	Plastic Power
LM340K-8.0	8.0 V ± 4%	0°C to +125°C	Metal Power
LM340T-8.0	8.0 V ± 4%	0°C to +125°C	Plastic Power
LM340K-12	12 V ± 4%	0°C to +125°C	Metal Power
LM340AK-12	12 V ± 2%	0°C to +125°C	
LM340T-12	12 V ± 4%	0°C to +125°C	Plastic Power
LM340AT-12	12 V ± 2%	0°C to +125°C	
LM340K-15	15 V ± 4%	0°C to +125°C	Metal Power
LM340AK-15	15 V ± 2%	0°C to +125°C	
LM340T-15	15 V ± 4%	0°C to +125°C	Plastic Power
LM340AT-15	15 V ± 2%	0°C to +125°C	
LM340T-18	18 V ± 4%	0°C to +125°C	Plastic Power
LM340T-24	24 V ± 4%	0°C to +125°C	Plastic Power

*2% regulators are available in 5, 12 and 15 volt devices

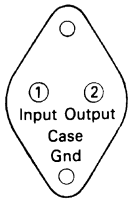
THREE-TERMINAL POSITIVE FIXED VOLTAGE REGULATORS

SILICON MONOLITHIC INTEGRATED CIRCUIT

K SUFFIX
METAL PACKAGE
CASE 1-03

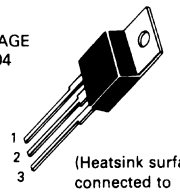


PIN 1. INPUT
2. OUTPUT
CASE GROUND



(Bottom View)

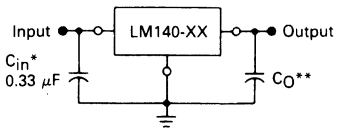
T SUFFIX
PLASTIC PACKAGE
CASE 221A-04



PIN 1. INPUT
2. GROUND
3. OUTPUT

(Heatsink surface connected to Pin 2)

STANDARD APPLICATION



A common ground is required between the input and the output voltages. The input voltage must remain typically 1.7 V above the output voltage even during the low point on the input ripple voltage.

XX = these two digits of the type number indicate voltage.

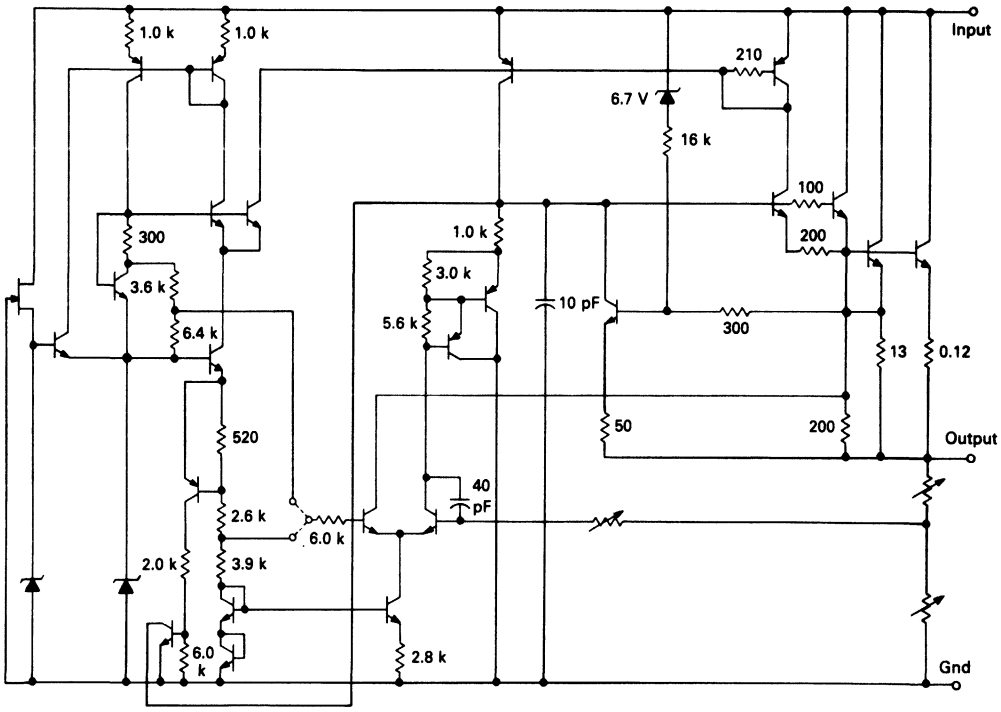
* = C_{in} is required if regulator is located an appreciable distance from power supply filter.

** = C_O is not needed for stability; however, it does improve transient response. If needed, use a 0.1 μF ceramic disc.

MAXIMUM RATINGS (T_A = +25°C unless otherwise noted.)

Rating	Symbol	Value	Unit
Input Voltage (5.0 V – 18 V) (24 V)	V_{in}	35 40	Vdc
Power Dissipation and Thermal Characteristics Plastic Package T_A = +25°C Derate above T_A = +25°C Thermal Resistance, Junction to Air T_C = +25°C Derate above T_C = +75°C (See Figure 1) Thermal Resistance, Junction to Case Metal Package T_C = +25°C Derate above T_A = +25°C Thermal Resistance, Junction to Air T_C = +25°C Derate above T_C = +65°C (See Figure 2) Thermal Resistance, Junction to Case	 P_D $1/\theta_{JA}$ θ_{JA} P_D $1/\theta_{JC}$ θ_{JC} P_D $1/\theta_{JA}$ θ_{JA} P_D $1/\theta_{JC}$ θ_{JC}	 Internally Limited 15.4 65 Internally Limited 200 5.0 Internally Limited 22.5 45 Internally Limited 182 5.5	 Watts mW/°C °C/W Watts mW/°C °C/W Watts mW/°C °C/W Watts mW/°C °C/W
Storage Junction Temperature Range	T_{stg}	–65 to +150	°C
Operating Junction Temperature Range LM140,A LM340,A	T_J	 –55 to +150 0 to +150	°C

EQUIVALENT SCHEMATIC DIAGRAM



DEFINITIONS

Line Regulation — The change in output voltage for a change in the input voltage. The measurement is made under conditions of low dissipation or by using pulse techniques such that the average chip temperature is not significantly affected.

Load Regulation — The change in output voltage for a change in load current at constant chip temperature.

Maximum Power Dissipation — The maximum total device dissipation for which the regulator will operate within specifications.

Quiescent Current — That part of the input current that is not delivered to the load.

Output Noise Voltage — The rms ac voltage at the output, with constant load and no input ripple, measured over a specified frequency range.

LM140/340 — 5.0

ELECTRICAL CHARACTERISTICS (V_{in} = 10 V, I_O = 500 mA, T_J = T_{low} to T_{high} (Note 1), unless otherwise noted).

Characteristic	Symbol	Min	Typ	Max	Unit
Output Voltage (T_J = +25°C) I_O = 5.0 mA to 1.0 A	V_O	4.8	5.0	5.2	Vdc
Line Regulation (Note 2)	Reg_{line}				mV
8.0 to 20 Vdc		—	—	50	
7.0 to 25 Vdc (T_J = +25°C)		—	—	50	
8.0 to 12 Vdc, I_O = 1.0 A		—	—	25	
7.3 to 20 Vdc, I_O = 1.0 A (T_J = +25°C)		—	—	50	
Load Regulation (Note 2)	Reg_{load}				mV
5.0 mA ≤ I_O ≤ 1.0 A		—	—	50	
5.0 mA ≤ I_O ≤ 1.5 A (T_J = +25°C)		—	—	50	
250 mA ≤ I_O ≤ 750 mA (T_J = +25°C)		—	—	25	
Output Voltage	V_O				Vdc
LM140					
8.0 ≤ V_{in} ≤ 20 Vdc, 5.0 mA ≤ I_O ≤ 1.0 A, P_D ≤ 15 W		4.75	—	5.25	
LM340					
7.0 ≤ V_{in} ≤ 20 Vdc, 5.0 mA ≤ I_O ≤ 1.0 A, P_D ≤ 15 W		4.75	—	5.25	
Quiescent Current	I_B				mA
I_O = 1.0 A					
LM140		—	—	7.0	
LM340		—	—	8.5	
LM140 (T_J = +25°C)		—	4.0	6.0	
LM340 (T_J = +25°C)		—	4.0	8.0	
Quiescent Current Change	ΔI_B				mA
8.0 ≤ V_{in} ≤ 25 Vdc, I_O = 500 mA LM140		—	—	0.8	
7.0 ≤ V_{in} ≤ 25 Vdc, I_O = 500 mA LM340		—	—	1.0	
5.0 mA ≤ I_O ≤ 1.0 A, V_{in} = 10 V LM140, LM340		—	—	0.5	
8.0 ≤ V_{in} ≤ 20 Vdc, I_O = 1.0 A LM140		—	—	0.8	
7.5 ≤ V_{in} ≤ 20 Vdc, I_O = 1.0 A LM340		—	—	1.0	
Ripple Rejection	RR				dB
LM140		68	—	—	
LM340		62	—	—	
I_O = 1.0 A (T_J = +25°C)					
LM140		68	80	—	
LM340		62	80	—	
Dropout Voltage	$V_{in} - V_O$	—	1.7	—	Vdc
Output Resistance (f = 1.0 kHz)	r_O	—	2.0	—	mΩ
Short-Circuit Current Limit (T_J = +25°C)	I_{sc}	—	2.0	—	mA
Output Noise Voltage (T_A = +25°C) 10 Hz ≤ f ≤ 100 kHz	V_n	—	40	—	μV
Average Temperature Coefficient of Output Voltage I_O = 5.0 mA	TCV_O	—	±0.6	—	mV/°C
Peak Output Current (T_J = +25°C)	I_O	—	2.4	—	A
Input Voltage to Maintain Line Regulation (T_J = +25°C) I_O = 1.0 A		7.3	—	—	Vdc

NOTES: 1. T_{low} = −55°C for LM140 T_{high} = +150°C for LM140
= 0°C for LM340 = +125°C for LM340

2. Load and line regulation are specified at constant junction temperature. Changes in V_O due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

LM140A/340A — 5.0

ELECTRICAL CHARACTERISTICS (V_{in} = 10 V, I_O = 1.0 A, T_J = T_{low} to T_{high} (Note 1), unless otherwise noted).

Characteristic	Symbol	Min	Typ	Max	Unit
Output Voltage (T_J = +25°C) I_O = 5.0 mA to 1.0 A	V_O	4.9	5.0	5.1	Vdc
Line Regulation (Note 2) 7.5 to 20 Vdc, I_O = 500 mA 7.3 to 20 Vdc (T_J = +25°C) 8.0 to 12 Vdc 8.0 to 12 Vdc (T_J = +25°C)	Reg_{line}	 — — — —	 — 3.0 — —	 10 10 12 4.0	mV
Load Regulation (Note 2) 5.0 mA ≤ I_O ≤ 1.0 A 5.0 mA ≤ I_O ≤ 1.5 A (T_J = +25°C) 250 mA ≤ I_O ≤ 750 mA (T_J = +25°C)	Reg_{load}	 — — —	 — — —	 25 25 15	mV
Output Voltage 7.5 ≤ V_{in} ≤ 20 Vdc, 5.0 mA ≤ I_O ≤ 1.0 A, P_D ≤ 15 W	V_O	4.8	—	5.2	Vdc
Quiescent Current (T_J = +25°C)	I_B	— —	— 3.5	6.5 6.0	mA
Quiescent Current Change 5.0 mA ≤ I_O ≤ 1.0 A, V_{in} = 10 V 8.0 ≤ V_{in} ≤ 25 Vdc, I_O = 500 mA 7.5 ≤ V_{in} ≤ 20 Vdc, I_O = 1.0 A (T_J = +25°C)	ΔI_B	 — — —	 — — —	 0.5 0.8 0.8	mA
Ripple Rejection 8.0 ≤ V_{in} ≤ 18 Vdc, f = 120 Hz I_O = 500 mA I_O = 1.0 A (T_J = +25°C)	RR	 68 68	 — 80	 — —	dB
Dropout Voltage	$V_{in} - V_O$	—	1.7	—	Vdc
Output Resistance (f = 1.0 kHz)	r_O	—	2.0	—	mΩ
Short-Circuit Current Limit (T_J = +25°C)	I_{sc}	—	2.0	—	mA
Output Noise Voltage (T_A = +25°C) 10 Hz ≤ f ≤ 100 kHz	V_n	—	40	—	μV
Average Temperature Coefficient of Output Voltage I_O = 5.0 mA	TCV_O	—	±0.6	—	mV/°C
Peak Output Current (T_J = +25°C)	I_O	—	2.4	—	A
Input Voltage to Maintain Line Regulation (T_J = +25°C)		7.3	—	—	Vdc

NOTES:

1. T_{low} = −55°C for LM140A T_{high} = +150°C for LM140A
   = 0°C for LM340A = +125°C for LM340A
2. Load and line regulation are specified at constant junction temperature. Changes in V_O due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

LM140/340 — 6.0

ELECTRICAL CHARACTERISTICS (V_{in} = 11 V, I_O = 500 mA, T_J = T_{low} to T_{high} (Note 1), unless otherwise noted).

Characteristic	Symbol	Min	Typ	Max	Unit
Output Voltage (T_J = +25°C) I_O = 5.0 mA to 1.0 A	V_O	5.75	6.0	6.25	Vdc
Line Regulation (Note 2)	Reg_{line}				mV
9.0 to 21 Vdc		—	—	60	
8.0 to 25 Vdc (T_J = +25°C)		—	—	60	
9.0 to 13 Vdc, I_O = 1.0 A		—	—	30	
8.3 to 21 Vdc, I_O = 1.0 A (T_J = +25°C)		—	—	60	
Load Regulation (Note 2)	Reg_{load}				mV
5.0 mA ≤ I_O ≤ 1.0 A		—	—	60	
5.0 mA ≤ I_O ≤ 1.5 A (T_J = +25°C)		—	—	60	
250 mA ≤ I_O ≤ 750 mA (T_J = +25°C)		—	—	30	
Output Voltage	V_O				Vdc
LM140					
9.0 ≤ V_{in} ≤ 21 Vdc, 5.0 mA ≤ I_O ≤ 1.0 A, P_D ≤ 15 W		5.7	—	6.3	
LM340					
8.0 ≤ V_{in} ≤ 21 Vdc, 6.0 mA ≤ I_O ≤ 1.0 A, P_D ≤ 15 W		5.7	—	6.3	
Quiescent Current	I_B				mA
I_O = 1.0 A					
LM140		—	—	7.0	
LM340		—	—	8.5	
LM140 (T_J = +25°C)		—	4.0	6.0	
LM340 (T_J = +25°C)		—	4.0	8.0	
Quiescent Current Change	ΔI_B				mA
9.0 ≤ V_{in} ≤ 25 Vdc, I_O = 500 mA LM140		—	—	0.8	
8.0 ≤ V_{in} ≤ 25 Vdc, I_O = 500 mA LM340		—	—	1.0	
5.0 mA ≤ I_O ≤ 1.0 A, V_{in} = 11 V LM140, LM340		—	—	0.5	
9.0 ≤ V_{in} ≤ 21 Vdc, I_O = 1.0 A LM140		—	—	0.8	
8.6 ≤ V_{in} ≤ 21 Vdc, I_O = 1.0 A LM340		—	—	1.0	
Ripple Rejection	RR				dB
LM140		65	—	—	
LM340		59	—	—	
I_O = 1.0 A (T_J = +25°C)					
LM140		65	78	—	
LM340		59	78	—	
Dropout Voltage	$V_{in} - V_O$	—	1.7	—	Vdc
Output Resistance (f = 1.0 kHz)	r_O	—	2.0	—	mΩ
Short-Circuit Current Limit (T_J = +25°C)	I_{sc}	—	1.9	—	mA
Output Noise Voltage (T_A = +25°C) 10 Hz ≤ f ≤ 100 kHz	V_n	—	45	—	μV
Average Temperature Coefficient of Output Voltage I_O = 5.0 mA	TCV_O	—	±0.7	—	mV/°C
Peak Output Current (T_J = +25°C)	I_O	—	2.4	—	A
Input Voltage to Maintain Line Regulation (T_J = +25°C) I_O = 1.0 A		8.3	—	—	Vdc

NOTES:

1. T_{low} = −55°C for LM140 T_{high} = +150°C for LM140
   = 0°C for LM340 = +125°C for LM340
2. Load and line regulation are specified at constant junction temperature. Changes in V_O due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

LM140/340 — 8.0

ELECTRICAL CHARACTERISTICS (V_{in} = 14 V, I_O = 500 mA, T_J = T_{low} to T_{high} (Note 1), unless otherwise noted).

Characteristic	Symbol	Min	Typ	Max	Unit
Output Voltage (T_J = +25°C) I_O = 5.0 mA to 1.0 A	V_O	7.7	8.0	8.3	Vdc
Line Regulation (Note 2)	Reg_{line}				mV
11 to 23 Vdc		—	—	80	
10.5 to 25 Vdc (T_J = +25°C)		—	—	80	
11 to 17 Vdc, I_O = 1.0 A		—	—	40	
10.5 to 23 Vdc, I_O = 1.0 A (T_J = +25°C)		—	—	80	
Load Regulation (Note 2)	Reg_{load}				mV
5.0 mA ≤ I_O ≤ 1.0 A		—	—	80	
5.0 mA ≤ I_O ≤ 1.5 A (T_J = +25°C)		—	—	80	
250 mA ≤ I_O ≤ 750 mA (T_J = +25°C)		—	—	40	
Output Voltage	V_O				Vdc
LM140					
11.5 ≤ V_{in} ≤ 23 Vdc, 5.0 mA ≤ I_O ≤ 1.0 A, P_D ≤ 15 W		7.6	—	8.4	
LM340					
10.5 ≤ V_{in} ≤ 23 Vdc, 5.0 mA ≤ I_O ≤ 1.0 A, P_D ≤ 15 W		7.6	—	8.4	
Quiescent Current	I_B				mA
I_O = 1.0 A					
LM140		—	—	7.0	
LM340		—	—	8.5	
LM140 (T_J = +25°C)		—	4.0	6.0	
LM340 (T_J = +25°C)		—	4.0	8.0	
Quiescent Current Change	ΔI_B				mA
11.5 ≤ V_{in} ≤ 25 Vdc, I_O = 500 mA LM140		—	—	0.8	
10.5 ≤ V_{in} ≤ 25 Vdc, I_O = 500 mA LM340		—	—	1.0	
5.0 mA ≤ I_O ≤ 1.0 A, V_{in} = 14 V LM140, LM340		—	—	0.5	
11.5 ≤ V_{in} ≤ 23 Vdc, I_O = 1.0 A LM140		—	—	0.8	
10.6 ≤ V_{in} ≤ 23 Vdc, I_O = 1.0 A LM340		—	—	1.0	
Ripple Rejection	RR				dB
LM140		62	—	—	
LM340		56	—	—	
I_O = 1.0 A (T_J = +25°C)					
LM140		62	76	—	
LM340		56	76	—	
Dropout Voltage	$V_{in} - V_O$	—	1.7	—	Vdc
Output Resistance (f = 1.0 kHz)	r_O	—	2.0	—	mΩ
Short-Circuit Current Limit (T_J = +25°C)	I_{sc}	—	1.5	—	mA
Output Noise Voltage (T_A = +25°C) 10 Hz ≤ f ≤ 100 kHz	V_n	—	52	—	μV
Average Temperature Coefficient of Output Voltage I_O = 5.0 mA	TCV_O	—	±1.0	—	mV/°C
Peak Output Current (T_J = +25°C)	I_O	—	2.4	—	A
Input Voltage to Maintain Line Regulation (T_J = +25°C) I_O = 1.0 A		10.5	—	—	Vdc

NOTES:

1. T_{low} = −55°C for LM140 T_{high} = +150°C for LM140
   = 0°C for LM340 = +125°C for LM340
2. Load and line regulation are specified at constant junction temperature. Changes in V_O due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

LM140/340 — 12

ELECTRICAL CHARACTERISTICS (V_{in} = 19 V, I_O = 500 mA, T_J = T_{low} to T_{high} (Note 1), unless otherwise noted).

Characteristic	Symbol	Min	Typ	Max	Unit
Output Voltage (T_J = +25°C) I_O = 5.0 mA to 1.0 A	V_O	11.5	12	12.5	Vdc
Line Regulation (Note 2)	Reg_{line}				mV
15 to 27 Vdc		—	—	120	
14.6 to 30 Vdc (T_J = +25°C)		—	—	120	
16 to 22 Vdc, I_O = 1.0 A		—	—	60	
14.6 to 27 Vdc, I_O = 1.0 A (T_J = +25°C)		—	—	120	
Load Regulation (Note 2)	Reg_{load}				mV
5.0 mA ≤ I_O ≤ 1.0 A		—	—	120	
5.0 mA ≤ I_O ≤ 1.5 A (T_J = +25°C)		—	—	120	
250 mA ≤ I_O ≤ 750 mA (T_J = +25°C)		—	—	60	
Output Voltage	V_O				Vdc
LM140					
15.5 ≤ V_{in} ≤ 27 Vdc, 5.0 mA ≤ I_O ≤ 1.0 A, P_D ≤ 15 W		11.4	—	12.6	
LM340					
14.5 ≤ V_{in} ≤ 27 Vdc, 5.0 mA ≤ I_O ≤ 1.0 A, P_D ≤ 15 W		11.4	—	12.6	
Quiescent Current	I_B				mA
I_O = 1.0 A					
LM140		—	—	7.0	
LM340		—	—	8.5	
LM140 (T_J = +25°C)		—	4.0	6.0	
LM340 (T_J = +25°C)		—	4.0	8.0	
Quiescent Current Change	ΔI_B				mA
15 ≤ V_{in} ≤ 30 Vdc, I_O = 500 mA LM140		—	—	0.8	
14.5 ≤ V_{in} ≤ 30 Vdc, I_O = 500 mA LM340		—	—	1.0	
5.0 mA ≤ I_O ≤ 1.0 A, V_{in} = 19 V LM140, LM340		—	—	0.5	
15 ≤ V_{in} ≤ 27 Vdc, I_O = 1.0 A LM140		—	—	0.8	
14.8 ≤ V_{in} ≤ 27 Vdc, I_O = 1.0 A LM340		—	—	1.0	
Ripple Rejection	RR				dB
LM140		61	—	—	
LM340		55	—	—	
I_O = 1.0 A (T_J = +25°C)					
LM140		61	72	—	
LM340		55	72	—	
Dropout Voltage	V_{in} – V_O	—	1.7	—	Vdc
Output Resistance (f = 1.0 kHz)	r_O	—	2.0	—	mΩ
Short-Circuit Current Limit (T_J = +25°C)	I_{sc}	—	1.1	—	mA
Output Noise Voltage (T_A = +25°C) 10 Hz ≤ f ≤ 100 kHz	V_n	—	75	—	μV
Average Temperature Coefficient of Output Voltage I_O = 5.0 mA	TCV_O	—	±1.5	—	mV/°C
Peak Output Current (T_J = +25°C)	I_O	—	2.4	—	A
Input Voltage to Maintain Line Regulation (T_J = +25°C) I_O = 1.0 A		14.6	—	—	Vdc

NOTES:

1. T_{low} = −55°C for LM140 T_{high} = +150°C for LM140
   = = +125°C for LM340
2. Load and line regulation are specified at constant junction temperature. Changes in V_O due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

LM140A/340A — 12

ELECTRICAL CHARACTERISTICS (V_{in} = 19 V, I_O = 1.0 A, T_J = T_{low} to T_{high} (Note 1), unless otherwise noted).

Characteristic	Symbol	Min	Typ	Max	Unit
Output Voltage (T_J = +25°C) I_O = 5.0 mA to 1.0 A	V_O	11.75	12	12.25	Vdc
Line Regulation (Note 2)	Reg_{line}				mV
14.8 to 27 Vdc, I_O = 500 mA		—	—	18	
14.5 to 27 Vdc (T_J = +25°C)		—	4.0	18	
16 to 22 Vdc		—	—	30	
16 to 22 Vdc (T_J = +25°C)		—	—	9.0	
Load Regulation (Note 2)	Reg_{load}				mV
5.0 mA ≤ I_O ≤ 1.0 A		—	—	60	
5.0 mA ≤ I_O ≤ 1.5 A (T_J = +25°C)		—	—	32	
250 mA ≤ I_O ≤ 750 mA (T_J = +25°C)		—	—	19	
Output Voltage 14.8 ≤ V_{in} ≤ 27 Vdc, 5.0 mA ≤ I_O ≤ 1.0 A, P_D ≤ 15 W	V_O	11.5	—	12.5	Vdc
Quiescent Current	I_B	—	—	6.5	mA
(T_J = +25°C)		—	3.5	6.0	
Quiescent Current Change	ΔI_B				mA
5.0 mA ≤ I_O ≤ 1.0 A, V_{in} = 19 V		—	—	0.5	
15 ≤ V_{in} ≤ 30 Vdc, I_O = 500 mA		—	—	0.8	
14.8 ≤ V_{in} ≤ 27 Vdc, I_O = 1.0 A (T_J = +25°C)		—	—	0.8	
Ripple Rejection	RR				dB
15 ≤ V_{in} ≤ 25 Vdc, f = 120 Hz					
I_O = 500 mA		61	—	—	
I_O = 1.0 A, (T_J = +25°C)		61	72	—	
Dropout Voltage	$V_{in} - V_O$	—	1.7	—	Vdc
Output Resistance (f = 1.0 kHz)	r_O	—	2.0	—	mΩ
Short-Circuit Current Limit (T_J = +25°C)	I_{sc}	—	1.1	—	mA
Output Noise Voltage (T_A = +25°C) 10 Hz ≤ f ≤ 100 kHz	V_n	—	75	—	μV
Average Temperature Coefficient of Output Voltage I_O = 5.0 mA	TCV_O	—	±1.5	—	mV/°C
Peak Output Current (T_J = +25°C)	I_O	—	2.4	—	A
Input Voltage to Maintain Line Regulation (T_J = +25°C)		14.5	—	—	Vdc

NOTES:

1. T_{low} = −55°C for LM140A T_{high} = +150°C for LM140A
   = 0°C for LM340A = +125°C for LM340A
2. Load and line regulation are specified at constant junction temperature. Changes in V_O due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

LM140A/340 — 15

ELECTRICAL CHARACTERISTICS (V_{in} = 23 V, I_O = 500 mA, T_J = T_{low} to T_{high} (Note 1), unless otherwise noted).

Characteristic	Symbol	Min	Typ	Max	Unit
Output Voltage (T_J = +25°C) I_O = 5.0 mA to 1.0 A	V_O	14.4	15	15.6	Vdc
Line Regulation (Note 2)	Reg_{line}				mV
18.5 to 30 Vdc		—	—	150	
17.5 to 30 Vdc (T_J = +25°C)		—	—	150	
20 to 26 Vdc, I_O = 1.0 A		—	—	75	
17.7 to 30 Vdc, I_O = 1.0 A (T_J = +25°C)		—	—	150	
Load Regulation (Note 2)	Reg_{load}				mV
5.0 mA ≤ I_O ≤ 1.0 A		—	—	150	
5.0 mA ≤ I_O ≤ 1.5 A (T_J = +25°C)		—	—	150	
250 mA ≤ I_O ≤ 750 mA (T_J = +25°C)		—	—	75	
Output Voltage	V_O				Vdc
LM140					
18.5 ≤ V_{in} ≤ 30 Vdc, 5.0 mA ≤ I_O ≤ 1.0 A, P_D ≤ 15 W		14.25	—	15.75	
LM340					
17.5 ≤ V_{in} ≤ 30 Vdc, 5.0 mA ≤ I_O ≤ 1.0 A, P_D ≤ 15 W		14.25	—	15.75	
Quiescent Current	I_B				mA
I_O = 1.0 A					
LM140		—	—	7.0	
LM340		—	—	8.5	
LM140 (T_J = +25°C)		—	4.0	6.0	
LM340 (T_J = +25°C)		—	4.0	8.0	
Quiescent Current Change	ΔI_B				mA
18.5 ≤ V_{in} ≤ 30 Vdc, I_O = 500 mA LM140		—	—	0.8	
17.5 ≤ V_{in} ≤ 30 Vdc, I_O = 500 mA LM340		—	—	1.0	
5.0 mA ≤ I_O ≤ 1.0 A, V_{in} = 23 V LM140, LM340		—	—	0.5	
18.5 ≤ V_{in} ≤ 30 Vdc, I_O = 1.0 A LM140		—	—	0.8	
17.9 ≤ V_{in} ≤ 30 Vdc, I_O = 1.0 A LM340		—	—	1.0	
Ripple Rejection	RR				dB
LM140		60	—	—	
LM340		54	—	—	
I_O = 1.0 A (T_J = +25°C)					
LM140		60	70	—	
LM340		54	70	—	
Dropout Voltage	$V_{in} - V_O$	—	1.7	—	Vdc
Output Resistance (f = 1.0 kHz)	r_O	—	2.0	—	mΩ
Short-Circuit Current Limit (T_J = +25°C)	I_{sc}	—	800	—	mA
Output Noise Voltage (T_A = +25°C) 10 Hz ≤ f ≤ 100 kHz	V_n	—	90	—	μV
Average Temperature Coefficient of Output Voltage I_O = 5.0 mA	TCV_O	—	±1.8	—	mV/°C
Peak Output Current (T_J = +25°C)	I_O	—	2.4	—	A
Input Voltage to Maintain Line Regulation (T_J = +25°C) I_O = 1.0 A		17.7	—	—	Vdc

NOTES:

1. T_{low} = −55°C for LM140 T_{high} = +150°C for LM140
   = = +125°C for LM340
2. Load and line regulation are specified at constant junction temperature. Changes in V_O due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

LM140A/340A — 15

ELECTRICAL CHARACTERISTICS (V_{in} = 23 V, I_O = 1.0 A, T_J = T_{low} to T_{high} (Note 1), unless otherwise noted).

Characteristic	Symbol	Min	Typ	Max	Unit
Output Voltage (T_J = +25°C) I_O = 5.0 mA to 1.0 A	V_O	14.7	15	15.3	Vdc
Line Regulation (Note 2) 17.9 to 30 Vdc, I_O = 500 mA 17.5 to 30 Vdc (T_J = +25°C) 20 to 26 Vdc, I_O = 1.0 A 20 to 26 Vdc, I_O = 1.0 A (T_J = +25°C)	Reg_{line}	 — — — —	 — 4.0 — —	 22 22 30 10	mV
Load Regulation (Note 2) 5.0 mA ≤ I_O ≤ 1.0 A 5.0 mA ≤ I_O ≤ 1.5 A (T_J = +25°C) 250 mA ≤ I_O ≤ 750 mA (T_J = +25°C)	Reg_{load}	 — — —	 — 12 —	 75 35 21	mV
Output Voltage 17.9 ≤ V_{in} ≤ 30 Vdc, 5.0 mA ≤ I_O ≤ 1.0 A, P_D ≤ 15 W	V_O	14.4	—	15.6	Vdc
Quiescent Current (T_J = +25°C)	I_B	— —	— 3.5	6.5 6.0	mA
Quiescent Current Change 5.0 mA ≤ I_O ≤ 1.0 A, V_{in} = 23 V 17.9 ≤ V_{in} ≤ 30 Vdc, I_O = 500 mA 17.9 ≤ V_{in} ≤ 30 Vdc, I_O = 1.0 A (T_J = +25°C)	ΔI_B	 — — —	 — — —	 0.5 0.8 0.8	mA
Ripple Rejection 18.5 ≤ V_{in} ≤ 28.5 Vdc, f = 120 Hz I_O = 500 mA I_O = 1.0 A, (T_J = +25°C)	RR	 60 60	 — 70	 — —	dB
Dropout Voltage	$V_{in} - V_O$	—	1.7	—	Vdc
Output Resistance (f = 1.0 kHz)	r_O	—	2.0	—	mΩ
Short-Circuit Current Limit (T_J = +25°C)	I_{sc}	—	800	—	mA
Output Noise Voltage (T_A = +25°C) 10 Hz ≤ f ≤ 100 kHz	V_n	—	90	—	μV
Average Temperature Coefficient of Output Voltage I_O = 5.0 mA	TCV_O	—	±1.8	—	mV/°C
Peak Output Current (T_J = +25°C)	I_O	—	2.4	—	A
Input Voltage to Maintain Line Regulation (T_J = +25°C)		17.5	—	—	Vdc

NOTES:

1. T_{low} = −55°C for LM140A T_{high} = +150°C for LM140A
   = 0°C for LM340A = +125°C for LM340A
2. Load and line regulation are specified at constant junction temperature. Changes in V_O due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

LM140/340 — 18

ELECTRICAL CHARACTERISTICS (V_{in} = 27 V, I_O = 500 mA, T_J = T_{low} to T_{high} (Note 1), unless otherwise noted).

Characteristic		Symbol	Min	Typ	Max	Unit
Output Voltage (T_J = +25°C) I_O = 5.0 mA to 1.0 A		V_O	17.3	18	18.7	Vdc
Line Regulation (Note 2)		Reg_{line}				mV
21.5 to 33 Vdc			—	—	180	
21 to 33 Vdc (T_J = +25°C)			—	—	180	
24 to 30 Vdc, I_O = 1.0 A			—	—	90	
21 to 33 Vdc, I_O = 1.0 A (T_J = +25°C)			—	—	180	
Load Regulation (Note 2)		Reg_{load}				mV
5.0 mA ≤ I_O ≤ 1.0 A			—	—	180	
5.0 mA ≤ I_O ≤ 1.5 A (T_J = +25°C)			—	—	180	
250 mA ≤ I_O ≤ 750 mA (T_J = +25°C)			—	—	90	
Output Voltage		V_O				Vdc
LM140						
22 ≤ V_{in} ≤ 33 Vdc, 5.0 mA ≤ I_O ≤ 1.0 A, P_D ≤ 15 W			17.1	—	18.9	
LM340						
21 ≤ V_{in} ≤ 33 Vdc, 5.0 mA ≤ I_O ≤ 1.0 A, P_D ≤ 15 W			17.1	—	18.9	
Quiescent Current		I_B				mA
I_O = 1.0 A						
LM140			—	—	7.0	
LM340			—	—	8.5	
LM140 (T_J = +25°C)			—	4.0	6.0	
LM340 (T_J = +25°C)			—	4.0	8.0	
Quiescent Current Change		ΔI_B				mA
22 ≤ V_{in} ≤ 33 Vdc, I_O = 500 mA	LM140		—	—	0.8	
21 ≤ V_{in} ≤ 33 Vdc, I_O = 500 mA	LM340		—	—	1.0	
5.0 mA ≤ I_O ≤ 1.0 A, V_{in} = 27 V	LM140, LM340		—	—	0.5	
22 ≤ V_{in} ≤ 33 Vdc, I_O = 1.0 A	LM140		—	—	0.8	
21 ≤ V_{in} ≤ 33 Vdc, I_O = 1.0 A	LM340		—	—	1.0	
Ripple Rejection		RR				dB
LM140			59	—	—	
LM340			53	—	—	
I_O = 1.0 A (T_J = +25°C)						
LM140			59	69	—	
LM340			53	69	—	
Dropout Voltage		$V_{in} - V_O$	—	1.7	—	Vdc
Output Resistance (f = 1.0 kHz)		r_O	—	2.0	—	mΩ
Short-Circuit Current Limit (T_J = +25°C)		I_{sc}	—	500	—	mA
Output Noise Voltage (T_A = +25°C) 10 Hz ≤ f ≤ 100 kHz		V_n	—	110	—	μV
Average Temperature Coefficient of Output Voltage I_O = 5.0 mA		TCV_O	—	±2.3	—	mV/°C
Peak Output Current (T_J = +25°C)		I_O	—	2.4	—	A
Input Voltage to Maintain Line Regulation (T_J = +25°C) I_O = 1.0 A			21	—	—	Vdc

NOTES:

1. T_{low} = −55°C for LM140 T_{high} = +150°C for LM140
   = 0°C for LM340 = +125°C for LM340
2. Load and line regulation are specified at constant junction temperature. Changes in V_O due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

LM140/340 — 24

ELECTRICAL CHARACTERISTICS (V_{in} = 33 V, I_O = 500 mA, T_J = T_{low} to T_{high} (Note 1), unless otherwise noted).

Characteristic		Symbol	Min	Typ	Max	Unit
Output Voltage (T_J = +25°C) I_O = 5.0 mA to 1.0 A		V_O	23	24	25	Vdc
Line Regulation (Note 2)		Reg_{line}				mV
28 to 38 Vdc			—	—	240	
27 to 38 Vdc (T_J = +25°C)			—	—	240	
30 to 36 Vdc, I_O = 1.0 A			—	—	120	
27.1 to 38 Vdc, I_O = 1.0 A (T_J = +25°C)			—	—	240	
Load Regulation (Note 2)		Reg_{load}				mV
5.0 mA ≤ I_O ≤ 1.0 A			—	—	240	
5.0 mA ≤ I_O ≤ 1.5 A (T_J = +25°C)			—	—	240	
250 mA ≤ I_O ≤ 750 mA (T_J = +25°C)			—	—	120	
Output Voltage		V_O				Vdc
LM140						
28 ≤ V_{in} ≤ 38 Vdc, 5.0 mA ≤ I_O ≤ 1.0 A, P_D ≤ 15 W			22.8	—	25.2	
LM340						
27 ≤ V_{in} ≤ 38 Vdc, 5.0 mA ≤ I_O ≤ 1.0 A, P_D ≤ 15 W			22.8	—	25.2	
Quiescent Current		I_B				mA
I_O = 1.0 A						
LM140			—	—	7.0	
LM340			—	—	8.5	
LM140 (T_J = +25°C)			—	4.0	6.0	
LM340 (T_J = +25°C)			—	4.0	8.0	
Quiescent Current Change		ΔI_B				mA
28 ≤ V_{in} ≤ 38 Vdc, I_O = 500 mA	LM140		—	—	0.8	
27 ≤ V_{in} ≤ 38 Vdc, I_O = 500 mA	LM340		—	—	1.0	
5.0 mA ≤ I_O ≤ 1.0 A, V_{in} = 33 V	LM140, LM340		—	—	0.5	
28 ≤ V_{in} ≤ 38 Vdc, I_O = 1.0 A	LM140		—	—	0.8	
27.3 ≤ V_{in} ≤ 38 Vdc, I_O = 1.0 A	LM340		—	—	1.0	
Ripple Rejection		RR				dB
LM140			56	—	—	
LM340			50	—	—	
I_O = 1.0 A (T_J = +25°C)						
LM140			56	66	—	
LM340			50	66	—	
Dropout Voltage		$V_{in} - V_O$	—	1.7	—	Vdc
Output Resistance (f = 1.0 kHz)		r_O	—	2.0	—	mΩ
Short-Circuit Current Limit (T_J = +25°C)		I_{sc}	—	200	—	mA
Output Noise Voltage (T_A = +25°C) 10 Hz ≤ f ≤ 100 kHz		V_n	—	170	—	μV
Average Temperature Coefficient of Output Voltage I_O = 5.0 mA		TCV_O	—	±3.0	—	mV/°C
Peak Output Current (T_J = +25°C)		I_O	—	2.4	—	A
Input Voltage to Maintain Line Regulation (T_J = +25°C) I_O = 1.0 A			27.1	—	—	Vdc

NOTES:

1. T_{low} = −55°C for LM140 T_{high} = +150°C for LM140
   = 0°C for LM340 = +125°C for LM340
2. Load and line regulation are specified at constant junction temperature. Changes in V_O due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

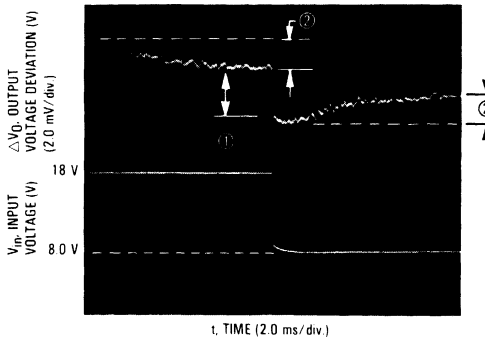
VOLTAGE REGULATOR PERFORMANCE

The performance of a voltage regulator is specified by its immunity to changes in load, input voltage, power dissipation, and temperature. Line and load regulation are tested with a pulse of short duration (< 100 μs) and are strictly a function of electrical gain. However, pulse widths of longer duration (> 1.0 ms) are sufficient to affect temperature gradients across the die. These temperature gradients can cause a change in the output voltage, in addition to changes caused by line and load regulation. Longer pulse widths and thermal gradients make it desirable to specify thermal regulation.

Thermal regulation is defined as the change in output voltage caused by a change in dissipated power for a specified time, and is expressed as a percentage output voltage change per watt. The change in dissipated power can be caused by a change in either the input voltage or the load current. Thermal regulation is a function of IC layout and die attach techniques, and usually occurs within 10 ms of a change in power dissipation. After 10 ms, additional changes in the output voltage are due to the temperature coefficient of the device.

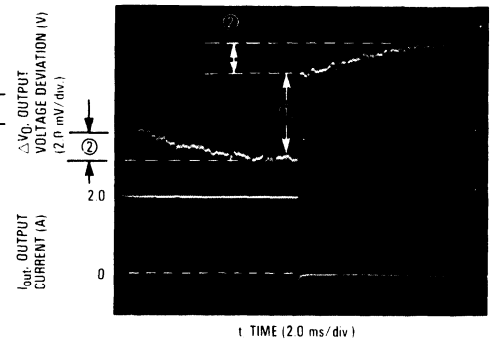
Figure 1 shows the line and thermal regulation response of a typical LM140AK-5.0 to a 10 watt input pulse. The variation of the output voltage due to line regulation is labeled ① and the thermal regulation component is labeled ②. Figure 2 shows the load and thermal regulation response of a typical LM140AK-5.0 to a 15 watt load pulse. The output voltage variation due to load regulation is labeled ① and the thermal regulation component is labeled ②.

FIGURE 1 — LINE AND THERMAL REGULATION



LM140AK-5.0
V_O = 5.0 V
V_{in} = 8.0 V → 18 V → 8.0 V ① = Reg_{line} = 2.4 mV
I_{out} = 1.0 A ② = Reg_{therm} = 0.0030%V_O/W

FIGURE 2 — LOAD AND THERMAL REGULATION



LM140AK-5.0
V_O = 5.0 V
V_{in} = 15 ① = Reg_{load} = 4.4 mV
I_{out} = 0 A → 1.5 A → 0 A ② = Reg_{therm} = 0.0020%V_O/W

FIGURE 3 — TEMPERATURE STABILITY

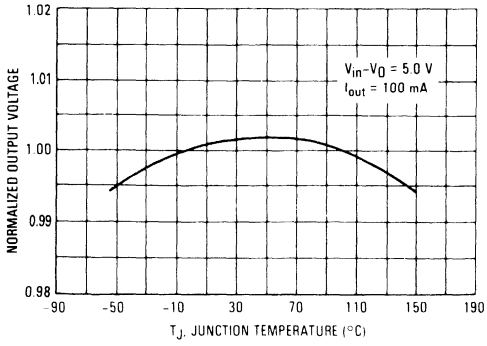


FIGURE 4 — OUTPUT IMPEDANCE

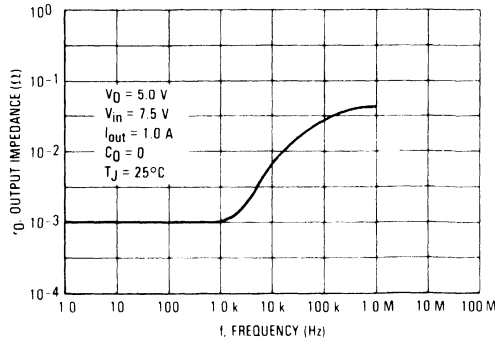


FIGURE 5 — RIPPLE REJECTION versus FREQUENCY

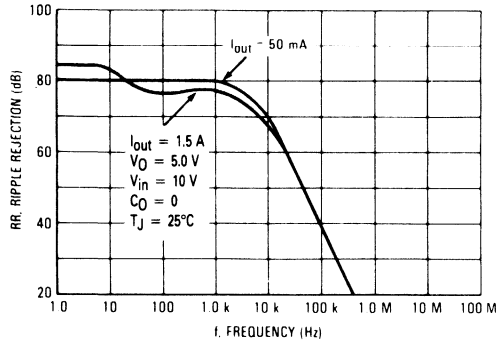


FIGURE 6 — RIPPLE REJECTION versus OUTPUT CURRENT

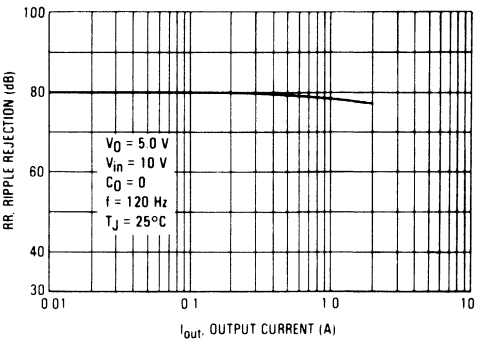


FIGURE 7 — QUIESCENT CURRENT versus INPUT VOLTAGE

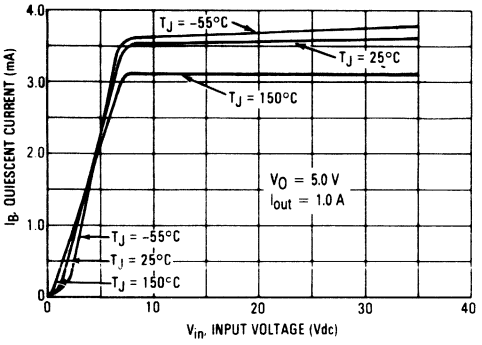


FIGURE 8 — QUIESCENT CURRENT versus OUTPUT CURRENT

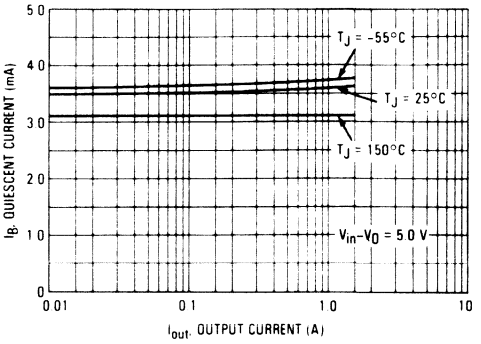


FIGURE 9 — DROPOUT VOLTAGE

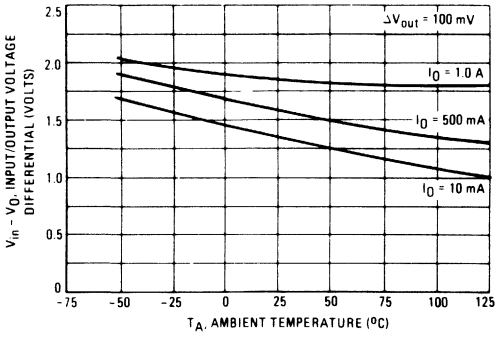


FIGURE 10 — PEAK OUTPUT CURRENT

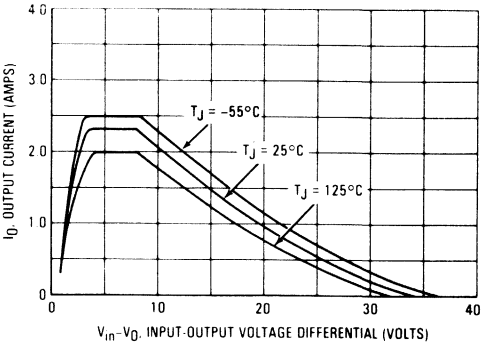


FIGURE 11 — LINE TRANSIENT RESPONSE

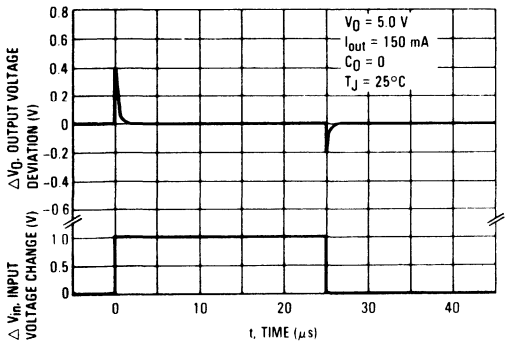


FIGURE 12 — LOAD TRANSIENT RESPONSE

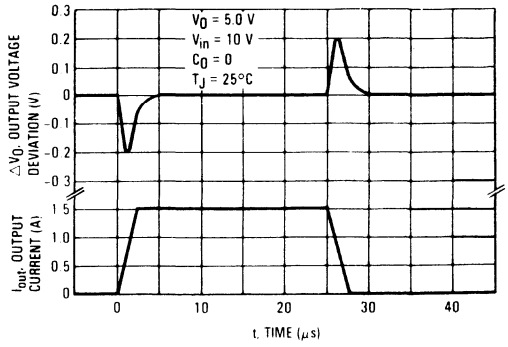


FIGURE 13 — WORST CASE POWER DISSIPATION versus AMBIENT TEMPERATURE (Case 221A)

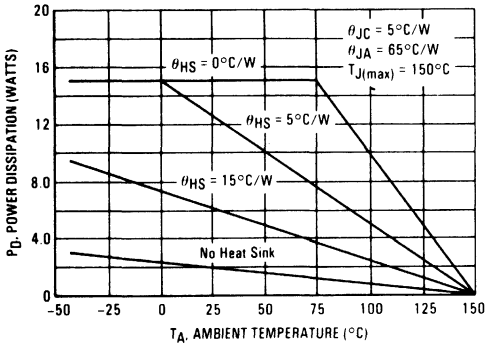
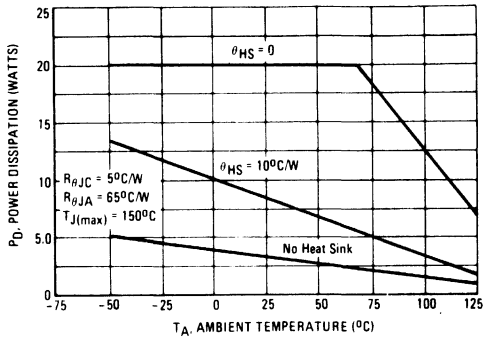


FIGURE 14 — WORST CASE POWER DISSIPATION versus AMBIENT TEMPERATURE (Case 1)



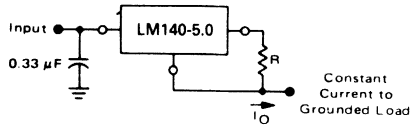
APPLICATIONS INFORMATION

Design Considerations

The LM140 Series of fixed voltage regulators are designed with Thermal Overload Protection that shuts down the circuit when subjected to an excessive power overload condition, Internal Short-Circuit Protection that limits the maximum current the circuit will pass, and Output Transistor Safe-Area Compensation that reduces the output short-circuit current as the voltage across the pass transistor is increased.

In many low current applications, compensation capacitors are not required. However, it is recommended that the regulator input be bypassed with a capacitor if the regulator is connected to the power supply filter with long wire lengths, or if the output load capacitance is large. An input bypass capacitor should be selected to provide good high-frequency characteristics to insure stable operation under all load conditions. A 0.33 μF or larger tantalum, mylar, or other capacitor having low internal impedance at high frequencies should be chosen. The bypass capacitor should be mounted with the shortest possible leads directly across the regulators input terminals. Normally good construction techniques should be used to minimize ground loops and lead resistance drops since the regulator has no external sense lead.

FIGURE 15 — CURRENT REGULATOR



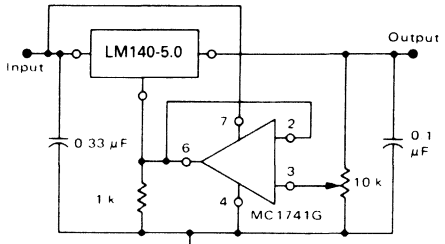
These regulators can also be used as a current source when connected as above. In order to minimize dissipation the LM140-5.0 is chosen in this application. Resistor R determines the current as follows:

$$I_O = \frac{5.0\ V}{R} + I_Q$$

$I_Q \cong 1.5$ mA over line and load changes

For example, a 1-ampere current source would require R to be a 5-ohm, 10-W resistor and the output voltage compliance would be the input voltage less 7.0 volts.

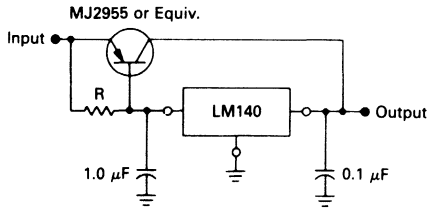
FIGURE 16 — ADJUSTABLE OUTPUT REGULATOR



V_O, 7.0 V to 20 V
$V_{IN} - V_O \geq 2.0$ V

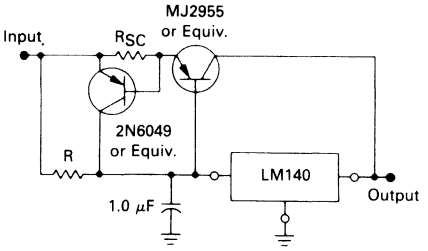
The addition of an operational amplifier allows adjustment to higher or intermediate values while retaining regulation characteristics. The minimum voltage obtainable with thi arrangement is 2.0 volts greater than the regulator voltage.

FIGURE 17 — CURRENT BOOST REGULATOR



The LM140 series can be current boosted with a PNP transistor. The MJ2955 provides current to 5.0 amperes. Resistor R in conjunction with the V_{BE} of the PNP determines when the pass transistor begins conducting; this circuit is not short-circuit proof. Input-output differential voltage minimum is increased by V_{BE} of the pass transistor.

FIGURE 18 — SHORT-CIRCUIT PROTECTION



The circuit of Figure 17 can be modified to provide supply protection against short circuits by adding a short-circuit sense resistor, P_{SC}, and an additional PNP transistor. The current sensing PNP must be able to handle the short-circuit current of the three-terminal regulator. Therefore, a four-ampere plastic power transistor is specified.

MOTOROLA

LM150
LM250
LM350

Specifications and Applications Information

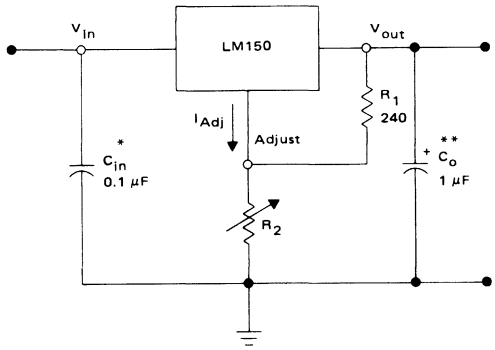
THREE-TERMINAL ADJUSTABLE OUTPUT POSITIVE VOLTAGE REGULATORS

The LM150/250/350 are adjustable 3-terminal positive voltage regulators capable of supplying in excess of 3.0 A over an output voltage range of 1.2 V to 33 V. These voltage regulators are exceptionally easy to use and require only two external resistors to set the output voltage. Further, they employ internal current limiting, thermal shutdown and safe area compensation, making them essentially blow-out proof.

The LM150 series serve a wide variety of applications including local, on card regulation. This device also makes an especially simple adjustable switching regulator, a programmable output regulator, or by connecting a fixed resistor between the adjustment and output, the LM150 series can be used as a precision current regulator.

- Guaranteed 3.0 Amps Output Current
- Output Adjustable between 1.2 V and 33 V
- Load Regulation Typically 0.1%
- Line Regulation Typically 0.005%/V
- Internal Thermal Overload Protection
- Internal Short-Circuit Current Limiting Constant with Temperature
- Output Transistor Safe-area Compensation
- Floating Operation for High Voltage Applications
- Standard 3-lead Transistor Packages
- Eliminates Stocking Many Fixed Voltages

STANDARD APPLICATION



* = C_{in} is required if regulator is located an appreciable distance from power supply filter.

** = C_o is not needed for stability, however it does improve transient response.

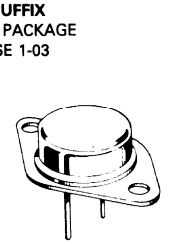
$$V_{out} = 1.25\ V\ (1 + \frac{R_2}{R_1}) + I_{Adj}\ R_2$$

Since I_{Adj} is controlled to less than 100 μA, the error associated with this term is negligible in most applications

THREE-TERMINAL ADJUSTABLE POSITIVE VOLTAGE REGULATORS

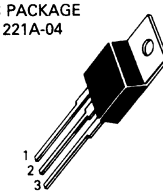
SILICON MONOLITHIC INTEGRATED CIRCUIT

K SUFFIX
METAL PACKAGE
CASE 1-03



Pins 1 and 2 electrically isolated from case.
Case is third electrical connection.

T SUFFIX
PLASTIC PACKAGE
CASE 221A-04



PIN 1. ADJUST
2. V_{out}
3. V_{in}

Heatsink surface connected to Pin 2

ORDERING INFORMATION

Device	Tested Operating Temperature Range	Package
LM150K	T_J = −55°C to +150°C	Metal Power
LM250K	T_J = −25°C to +150°C	Metal Power
LM350K	T_J = 0°C to +125°C	Metal Power
LM350T	T_J = 0°C to +125°C	Plastic Power

MAXIMUM RATINGS

Rating		Symbol	Value	Unit
Input-Output Voltage Differential		V_I-V_O	35	Vdc
Power Dissipation		P_D	Internally Limited	
Operating Junction Temperature Range	LM150 LM250 LM350	T_J	-55 to +150 -25 to +150 0 to +125	°C
Storage Temperature Range		T_{stg}	-65 to +150	°C
Soldering Lead Temperature (10 seconds)			300	°C

ELECTRICAL CHARACTERISTICS (Unless otherwise specified, V_I-V_O = 5.0 V; I_L = 1.5 A; T_J = T_{low} to T_{high}; P_{max} [see Note 1].)

Characteristic	Figure	Symbol	LM150/250 Min	LM150/250 Typ	LM150/250 Max	LM350 Min	LM350 Typ	LM350 Max	Unit
Line Regulation (Note 2) T_A = 25°C, 3.0 V ≤ V_I-V_O ≤ 35 V	1	Reg_{line}	—	0.005	0.01	—	0.005	0.03	%/V
Load Regulation (Note 2) T_A = 25°C, 10 mA ≤ I_L ≤ 3.0 A V_O ≤ 5.0 V V_O ≥ 5.0 V	2	Reg_{load}	 — —	 5.0 0.1	 15 0.3	 — —	 5.0 0.1	 25 0.5	 mV % V_O
Thermal Regulation, Pulse = 20 ms, T_A = 25°C	—	Reg_{therm}	—	0.002	—	—	0.002	—	% V_O/W
Adjustment Pin Current	3	I_{Adj}	—	50	100	—	50	100	μA
Adjustment Pin Current Change 3.0 V ≤ V_I-V_O ≤ 35 V 10 mA ≤ I_L ≤ 3.0 A, P_D ≤ P_{max}	1,2	ΔI_{Adj}	—	0.2	5.0	—	0.2	5.0	μA
Reference Voltage (Note 3) 3.0 V ≤ V_I-V_O ≤ 35 V 10 mA ≤ I_L ≤ 3.0 A, P_D ≤ P_{max}	3	V_{ref}	1.20	1.25	1.30	1.20	1.25	1.30	V
Line Regulation (Note 2) 3.0 V ≤ V_I-V_O ≤ 35 V	1	Reg_{line}	—	0.02	0.05	—	0.02	0.07	%/V
Load Regulation (Note 2) 10 mA ≤ I_L ≤ 3.0 A V_O ≤ 5.0 V V_O ≥ 5.0 V	2	Reg_{load}	 — —	 20 0.3	 50 1.0	 — —	 20 0.3	 70 1.5	 mV % V_O
Temperature Stability (T_{low} ≤ T_J ≤ T_{high})	3	T_S	—	1.0	—	—	1.0	—	% V_O
Minimum Load Current to Maintain Regulation (V_I-V_O = 35 V)	3	I_{Lmin}	—	3.5	5.0	—	3.5	10	mA
Maximum Output Current V_I-V_O ≤ 10 V, P_D ≤ P_{max} V_I-V_O = 30 V, P_D ≤ P_{max}, T_A = 25°C	3	I_{max}	 3.0 0.3	 4.5 1.0	 — —	 3.0 0.25	 4.5 1.0	 — —	A
RMS Noise, % of V_O T_A = 25°C, 10 Hz ≤ f ≤ 10 kHz	—	N	—	0.003	—	—	0.003	—	% V_O
Ripple Rejection, V_O = 10 V, f = 120 Hz (Note 4) Without C_{Adj} C_{Adj} = 10 μF	4	RR	 — 66	 65 80	 — —	 — 66	 65 80	 — —	dB
Long-Term Stability, T_J = T_{high} (Note 5) T_A = 25°C for Endpoint Measurements	3	S	—	0.3	1.0	—	0.3	1.0	%/1.0 k Hrs.
Thermal Resistance Junction to Case Peak (Note 6) K Package T Package Average (Note 7) K Package T Package	—	$R_{\theta JC}$	 — — — —	 2.3 — — —	 — — 1.5 —	 — — — —	 2.3 2.3 — —	 — — 1.5 1.5	°C/W

NOTES:

(1) T_{low} = −55°C for LM150, −25°C for LM250, 0°C for LM350; T_{high} = +150°C for LM150, +150°C for LM250, +125°C for LM350
P_{max} = 30 W for K suffix
P_{max} = 25 W for T suffix

(2) Load and line regulation are specified at constant junction temperature. Changes in V_O due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

(3) Selected devices with tightened tolerance reference voltage available.

(4) C_{Adj}, when used, is connected between the adjustment pin and ground.

(5) Since Long-Term Stability cannot be measured on each device before shipment, this specification is an engineering estimate of average stability from lot to lot.

(6) Thermal Resistance evaluated measuring the hottest temperature on the die using an infrared scanner. This method of evaluation yields very accurate thermal resistance values which are conservative when compared to other measurement techniques.

(7) The average die temperature is used to derive the value of thermal resistance junction to case (average).

SCHEMATIC DIAGRAM

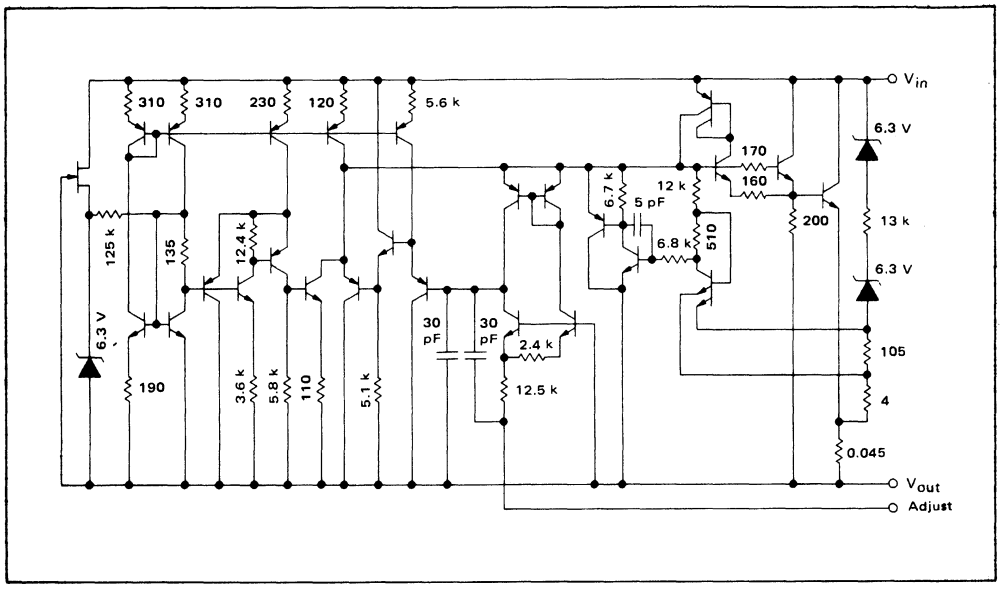


FIGURE 1 — LINE REGULATION AND ΔI_{Adj}/LINE TEST CIRCUIT

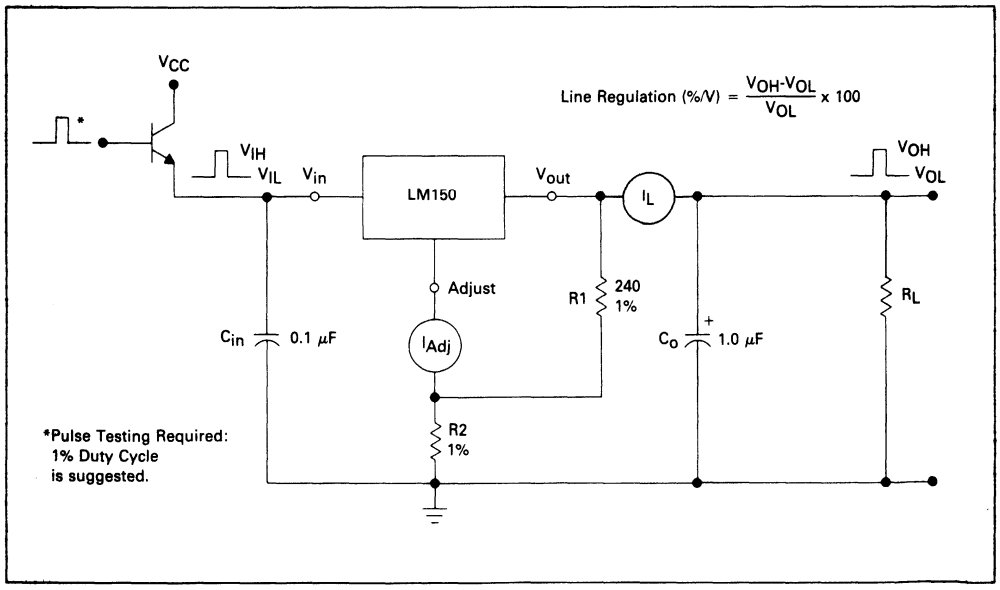


FIGURE 2 — LOAD REGULATION AND ΔI_{Adj}/LOAD TEST CIRCUIT

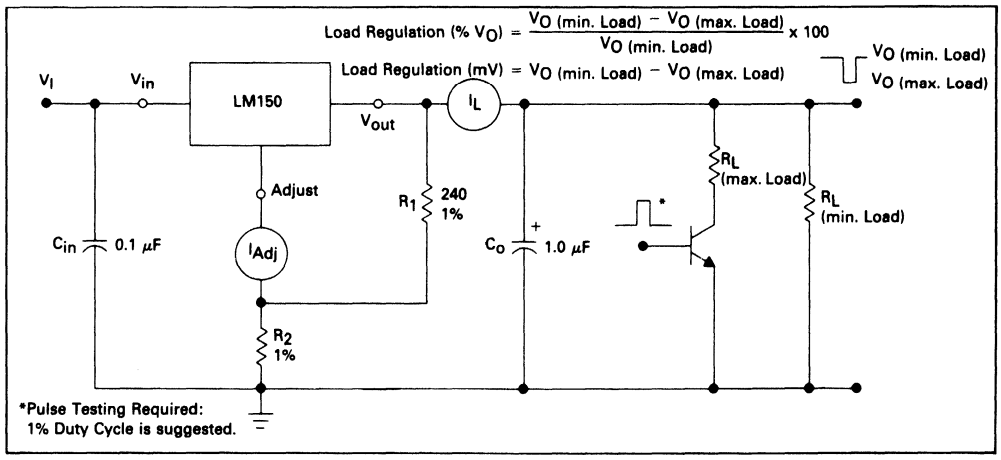


FIGURE 3 — STANDARD TEST CIRCUIT

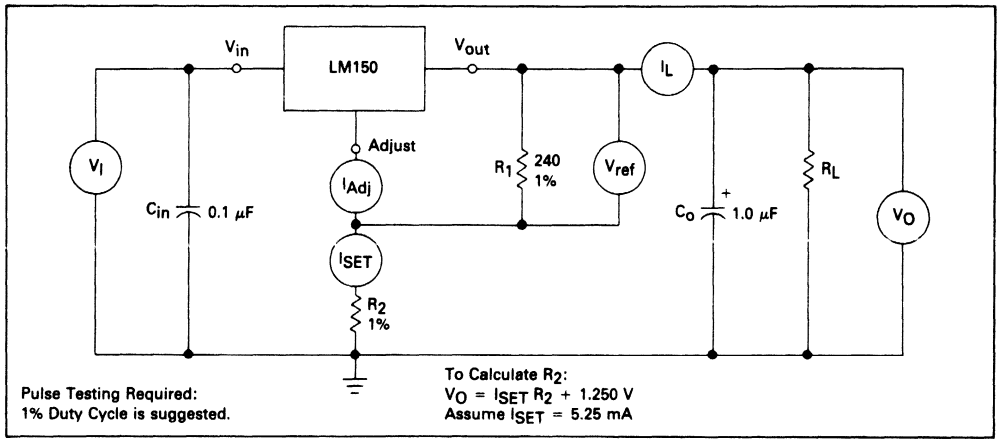


FIGURE 4 — RIPPLE REJECTION TEST CIRCUIT

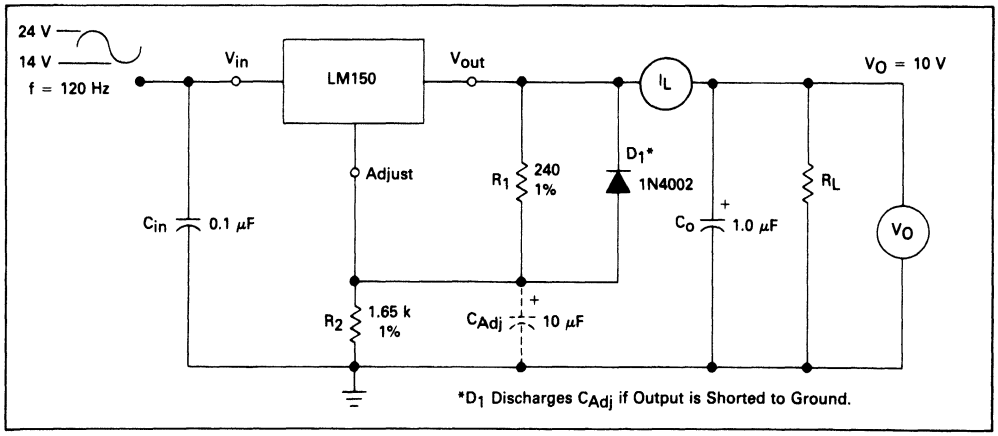


FIGURE 5 – LOAD REGULATION

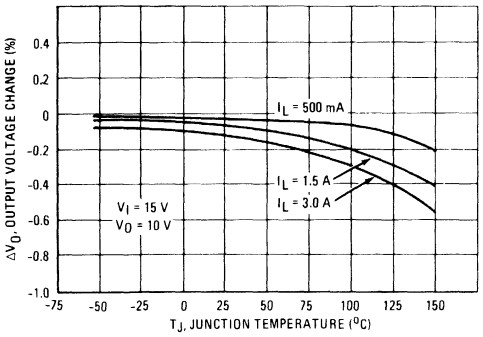


FIGURE 6 – CURRENT LIMIT

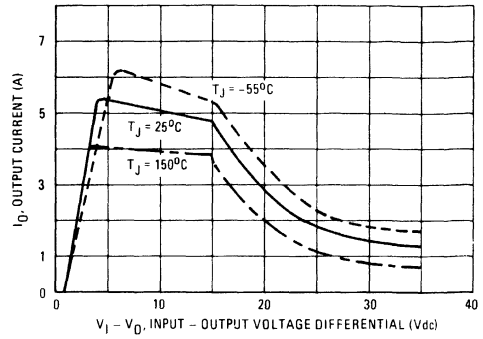


FIGURE 7 – ADJUSTMENT PIN CURRENT

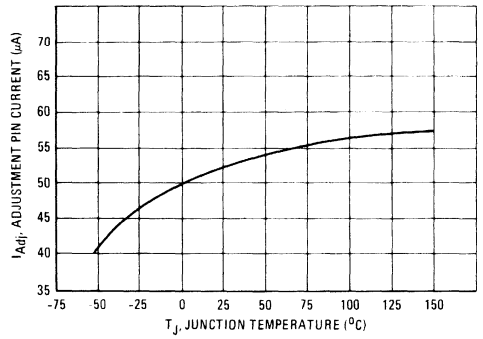


FIGURE 8 – DROPOUT VOLTAGE

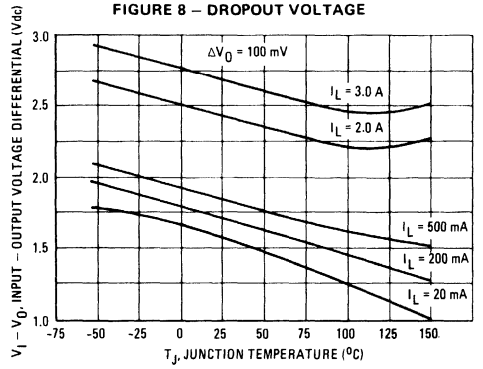


FIGURE 9 – TEMPERATURE STABILITY

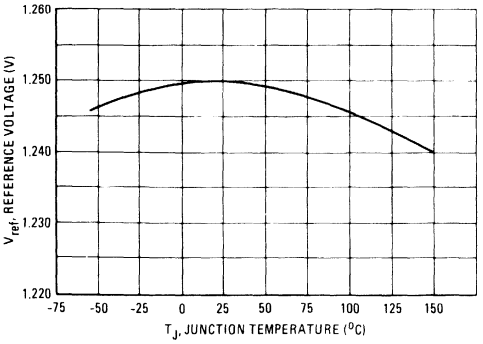


FIGURE 10 – MINIMUM OPERATING CURRENT

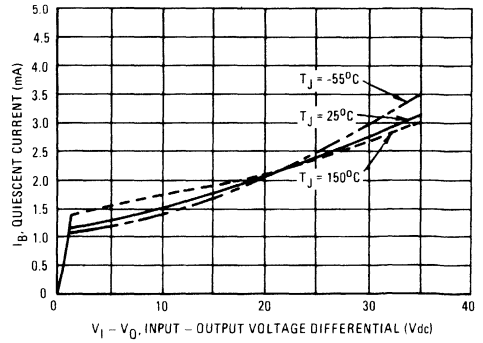


FIGURE 11 — RIPPLE REJECTION versus OUTPUT VOLTAGE

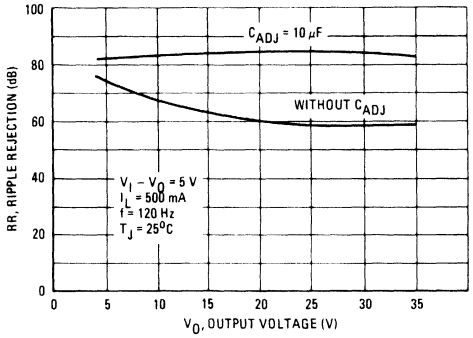


FIGURE 12 — RIPPLE REJECTION versus OUTPUT CURRENT

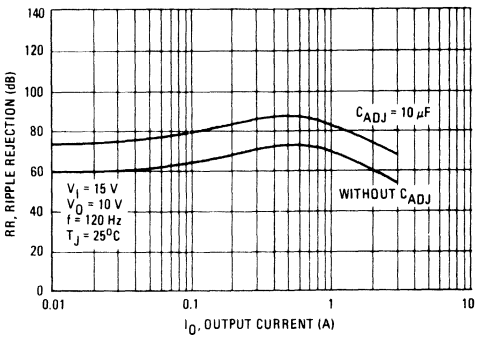


FIGURE 13 — RIPPLE REJECTION versus FREQUENCY

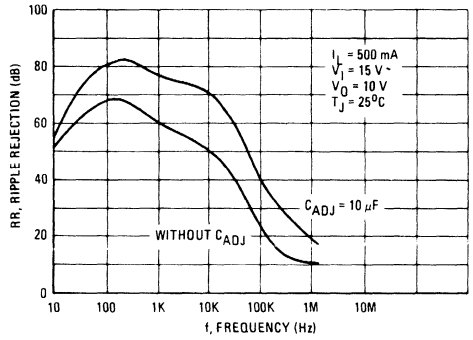


FIGURE 14 — OUTPUT IMPEDANCE

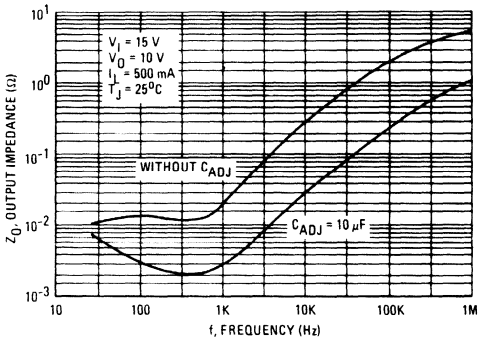


FIGURE 15 — LINE TRANSIENT RESPONSE

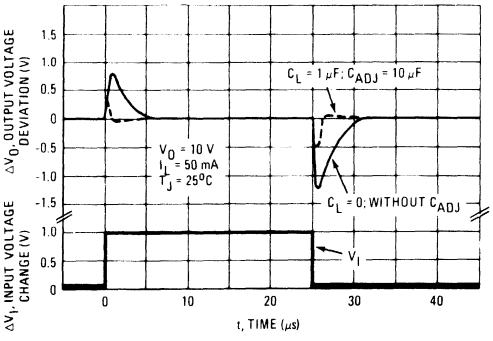
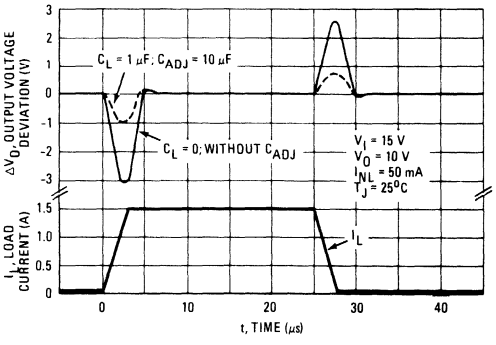


FIGURE 16 — LOAD TRANSIENT RESPONSE



APPLICATIONS INFORMATION

BASIC CIRCUIT OPERATION

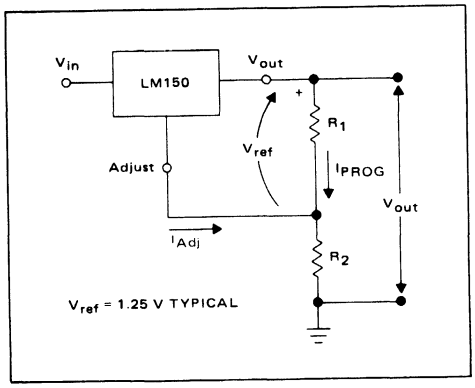
The LM150 is a 3-terminal floating regulator. In operation, the LM150 develops and maintains a nominal 1.25 volt reference (V_{ref}) between its output and adjustment terminals. This reference voltage is converted to a programming current (I_{PROG}) by R1 (see Figure 17), and this constant current flows through R2 to ground. The regulated output voltage is given by:

$$V_{out} = V_{ref}\left(1 + \frac{R2}{R1}\right) + I_{Adj}\,R2$$

Since the current from the adjustment terminal (I_{Adj}) represents an error term in the equation, the LM150 was designed to control I_{Adj} to less than 100 μA and keep it constant. To do this, all quiescent operating current is returned to the output terminal. This imposes the requirement for a minimum load current. If the load current is less than this minimum, the output voltage will rise.

Since the LM150 is a floating regulator, it is only the voltage differential across the circuit which is important to performance, and operation at high voltages with respect to ground is possible.

FIGURE 17 – BASIC CIRCUIT CONFIGURATION



LOAD REGULATION

The LM150 is capable of providing extremely good load regulation, but a few precautions are needed to obtain maximum performance. For best performance, the programming resistor (R1) should be connected as close to the regulator as possible to minimize line drops which effectively appear in series with the reference, thereby degrading regulation. The ground end of R2 can be returned near the load ground to provide remote ground sensing and improve load regulation.

EXTERNAL CAPACITORS

A 0.1 μF disc or 1 μF tantalum input bypass capacitor (C_{in}) is recommended to reduce the sensitivity to input line impedance.

The adjustment terminal may be bypassed to ground to improve ripple rejection. This capacitor (C_{ADJ}) prevents ripple from being amplified as the output voltage is increased. A 10 μF capacitor should improve ripple rejection about 15 dB at 120 Hz in a 10 volt application.

Although the LM150 is stable with no output capacitance, like any feedback circuit, certain values of external capacitance can cause excessive ringing. An output capacitance (C_O) in the form of a 1 μF tantalum or 25 μF aluminum electrolytic capacitor on the output swamps this effect and insures stability.

PROTECTION DIODES

When external capacitors are used with any I.C. regulator it is sometimes necessary to add protection diodes to prevent the capacitors from discharging through low current points into the regulator.

Figure 18 shows the LM150 with the recommended protection diodes for output voltages in excess of 25 V or high capacitance values ($C_O > 25\ \mu F$, $C_{ADJ} > 10\ \mu F$). Diode D_1 prevents C_O from discharging thru the I.C. during an input short circuit. Diode D_2 protects against capacitor C_{ADJ} discharging through the I.C. during an output short circuit. The combination of diodes D1 and D2 prevents C_{ADJ} from discharging through the I.C. during an input short circuit.

FIGURE 18 – VOLTAGE REGULATOR WITH PROTECTION DIODES

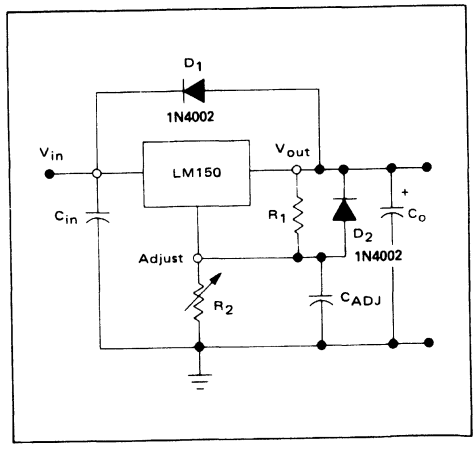


FIGURE 19 – "LABORATORY" POWER SUPPLY WITH ADJUSTABLE CURRENT LIMIT AND OUTPUT VOLTAGE

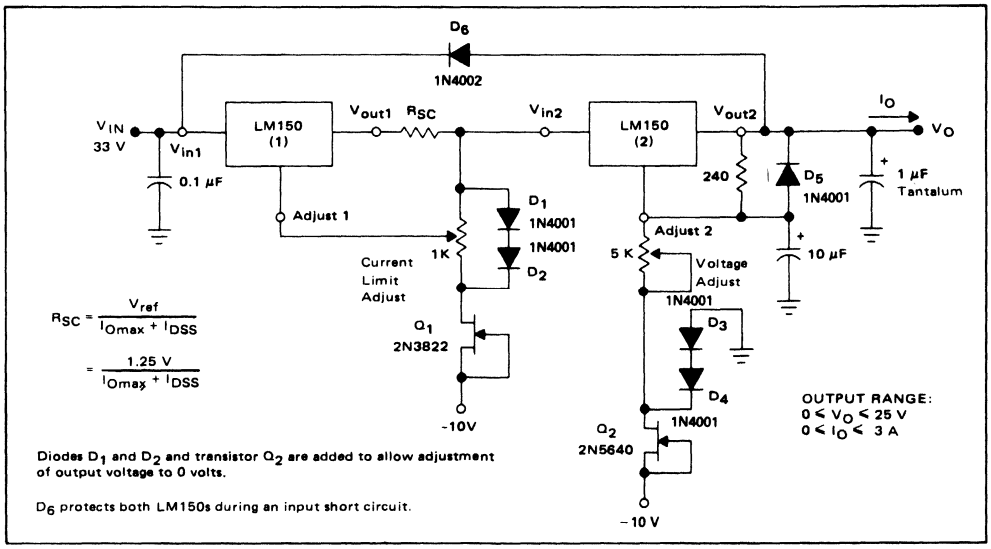


FIGURE 20 – ADJUSTABLE CURRENT LIMITER

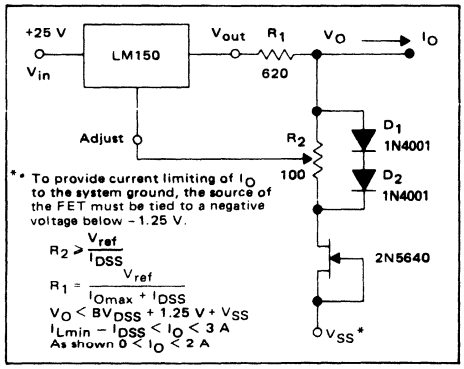


FIGURE 21 – 5 V ELECTRONIC SHUT DOWN REGULATOR

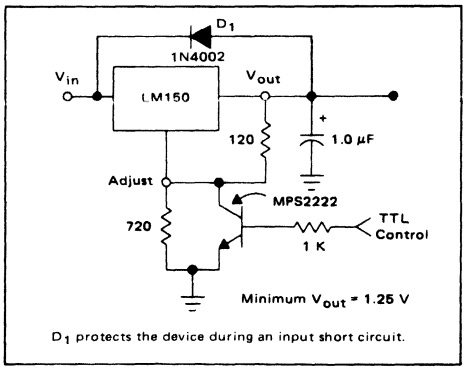


FIGURE 22 – SLOW TURN-ON REGULATOR

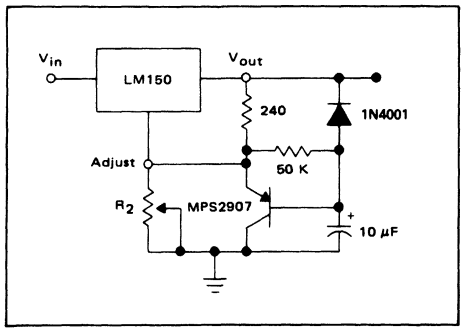
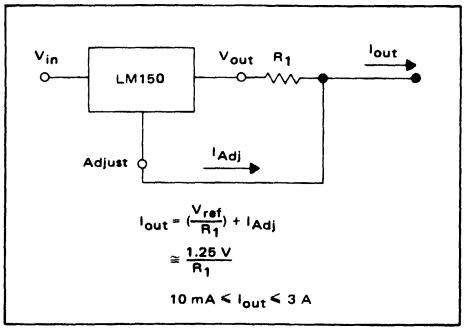


FIGURE 23 – CURRENT REGULATOR



MOTOROLA

LM317M

THREE-TERMINAL ADJUSTABLE OUTPUT POSITIVE VOLTAGE REGULATOR

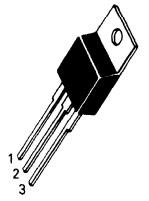
The LM317M is an adjustable 3-terminal positive voltage regulator capable of supplying in excess of 500 mA over an output voltage range of 1.2 V to 37 V. This voltage regulator is exceptionally easy to use and requires only two external resistors to set the output voltage. Further, it employs internal current limiting, thermal shutdown and safe area compensation, making it essentially blow-out proof.

The LM317M serves a wide variety of applications including local, on-card regulation. This device also makes an especially simple adjustable switching regulator, a programmable output regulator, or by connecting a fixed resistor between the adjustment and output, the LM317M can be used as a precision current regulator.

- Output Current in Excess of 500 mA
- Output Adjustable Between 1.2 V and 37 V
- Internal Thermal Overload Protection
- Internal Short-Circuit-Current Limiting
- Output Transistor Safe-Area Compensation
- Floating Operation for High Voltage Applications
- Standard 3-Lead Transistor Packages
- Eliminates Stocking Many Fixed Voltages

MEDIUM-CURRENT THREE-TERMINAL ADJUSTABLE POSITIVE VOLTAGE REGULATOR

SILICON MONOLITHIC INTEGRATED CIRCUIT



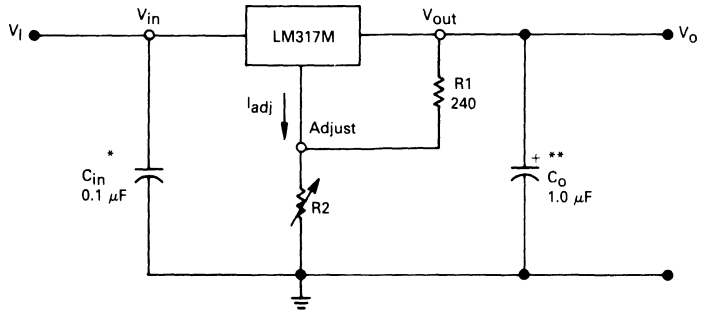
PIN 1. ADJUST
2. V_{out}
3. V_{in}

T SUFFIX
PLASTIC PACKAGE
CASE 221A-04

ORDERING INFORMATION

Device	Tested Operating Temperature Range	Package
LM317MT	T_J = 0°C to +125°C	Plastic Power

STANDARD APPLICATION



*C_{in} is required if regulator is located in appreciable distance from power supply filter.

**C_O is not needed for stability, however it does improve transient response.

$$V_O = 1.25\ V\ (1 + \frac{R_2}{R_1}) + I_{adj}\ R_2$$

Since I_{adj} is controlled to less than 100 μA, the error associated with this term is negligible in most applications.

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Input-Output Voltage Differential	V_I-V_O	40	Vdc
Power Dissipation	P_D	Internally Limited	
Operating Junction Temperature Range	T_J	0 to +150	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C

ELECTRICAL CHARACTERISTICS

(V_I-V_O = 5.0 V, I_O = 0.1 A, T_J = T_{low} to T_{high} [see Note 1], P_{max} per Note 2, unless otherwise specified.)

Characteristic	Figure	Symbol	Min	Typ	Max	Unit
Line Regulation (Note 3) T_A = 25°C, 3.0 V ≤ V_I-V_O ≤ 40 V	1	Reg_{line}	—	0.01	0.04	%/V
Load Regulation (Note 3) T_A = 25°C, 10 mA ≤ I_O ≤ 0.5 A V_O ≤ 5.0 V V_O ≥ 5.0 V	2	Reg_{load}	 — —	 5.0 0.1	 25 0.5	 mV % V_O
Adjustment Pin Current	3	I_{adj}	—	50	100	μA
Adjustment Pin Current Change 2.5 V ≤ V_I-V_O ≤ 40 V, 10 mA ≤ I_L ≤ 0.5 A, P_D ≤ P_{max}	1,2	ΔI_{adj}	—	0.2	5.0	μA
Reference Voltage (Note 4) 3.0 V ≤ V_I-V_O ≤ 40 V, 10 mA ≤ I_O ≤ 0.5 A, P_D ≤ P_{max}	3	V_{ref}	1.20	1.25	1.30	V
Line Regulation (Note 3) 3.0 V ≤ V_I-V_O ≤ 40 V	1	Reg_{line}	—	0.02	0.07	%/V
Load Regulation (Note 3) 10 mA ≤ I_O ≤ 0.5 A V_O ≤ 5.0 V V_O ≥ 5.0 V	2	Reg_{load}	 — —	 20 0.3	 70 1.5	 mV % V_O
Temperature Stability (T_{low} ≤ T_J ≤ T_{high})	3	T_S	—	0.7	—	% V_O
Minimum Load Current to Maintain Regulation (V_I-V_O = 40 V)	3	I_{Lmin}	—	3.5	10	mA
Maximum Output Current V_I-V_O ≤ 15 V, P_D ≤ P_{max} V_I-V_O = 40 V, P_D ≤ P_{max}, T_A = 25°C	3	I_{max}	 0.5 0.15	 0.9 0.25	 — —	A
RMS Noise, % of V_O T_A = 25°C, 10 Hz ≤ f ≤ 10 kHz	—	N	—	0.003	—	% V_O
Ripple Rejection, V_O = 10 V, f = 120 Hz (Note 5) Without C_{adj} C_{adj} = 10 μF	4	RR	 — 66	 65 80	 — —	dB
Long Term Stability, T_J = T_{high} (Note 6) T_A = 25°C for Endpoint Measurements	3	S	—	0.3	1.0	%/1.0 k Hrs.
Thermal Resistance Junction to Case	—	$R_{\theta JC}$	—	7.0	—	°C/W

NOTES:

(1) T_{low} to T_{high} = 0°C to +125°C

(2) P_{max} = 7.5 W

(3) Load and line regulation are specified at constant junction temperature. Changes in V_O due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

(4) Selected devices with tightened tolerance reference voltage available.

(5) C_{adj}, when used, is connected between the adjustment pin and ground.

(6) Since Long Term Stability cannot be measured on each device before shipment, this specification is an engineering estimate of average stability from lot to lot.

SCHEMATIC DIAGRAM

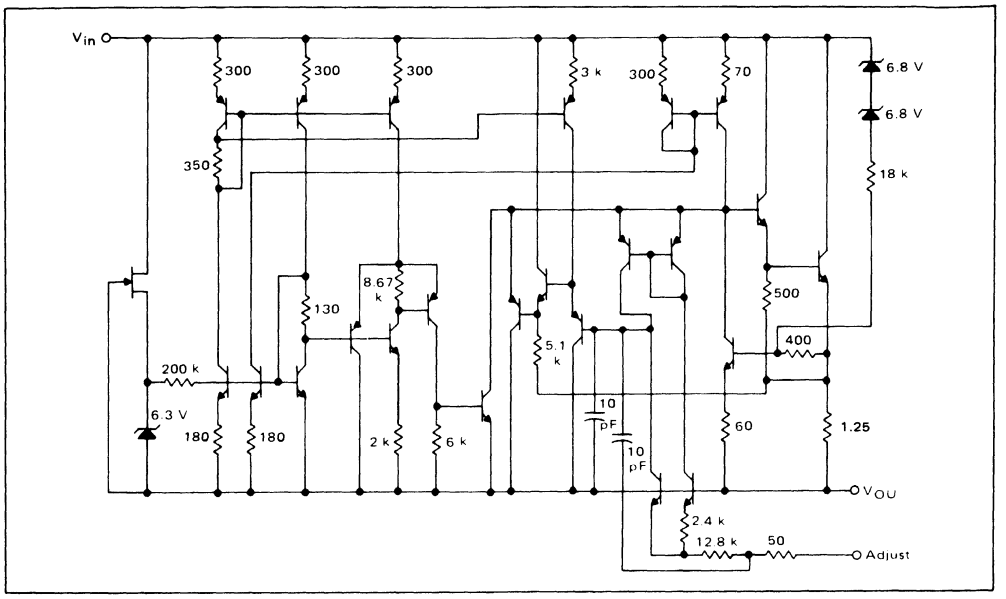


FIGURE 1 – LINE REGULATION AND ΔI_{Adj}/LINE TEST CIRCUIT

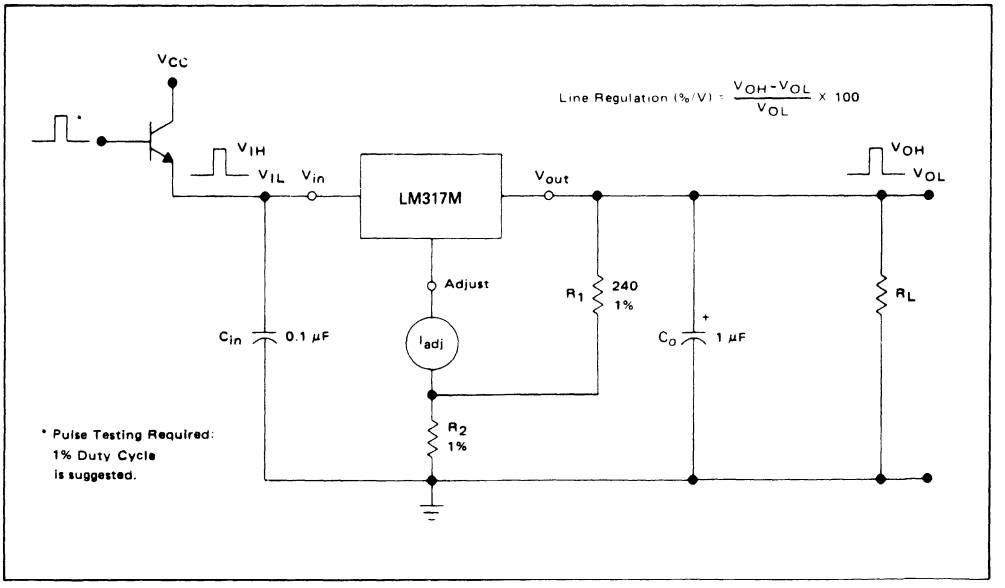


FIGURE 2 – LOAD REGULATION AND ΔI_{Adj}/LOAD TEST CIRCUIT

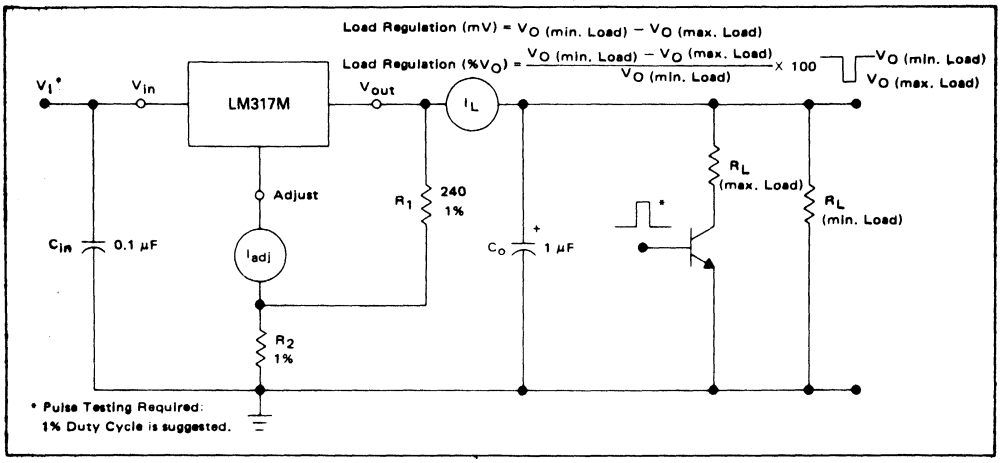


FIGURE 3 – STANDARD TEST CIRCUIT

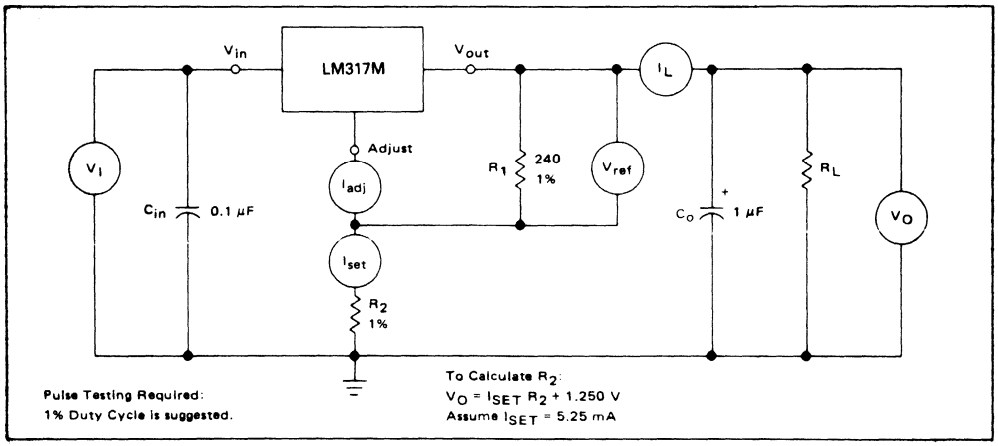


FIGURE 4 – RIPPLE REJECTION TEST CIRCUIT

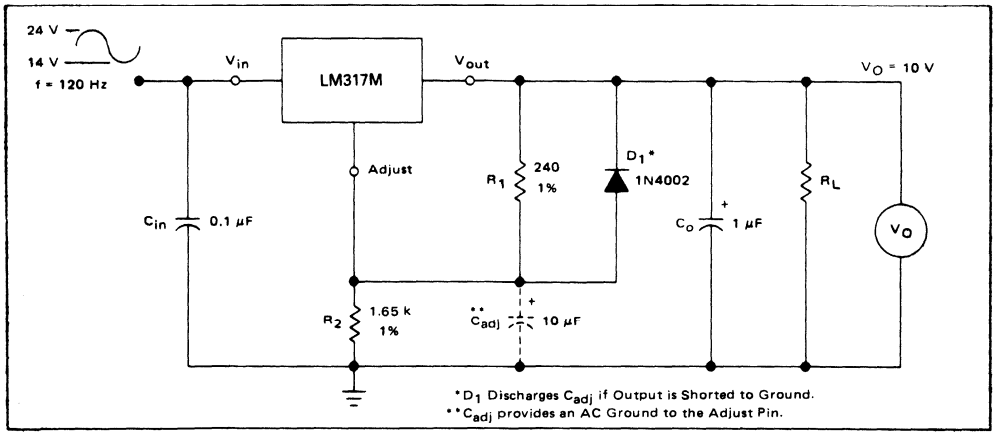


FIGURE 5 – LOAD REGULATION

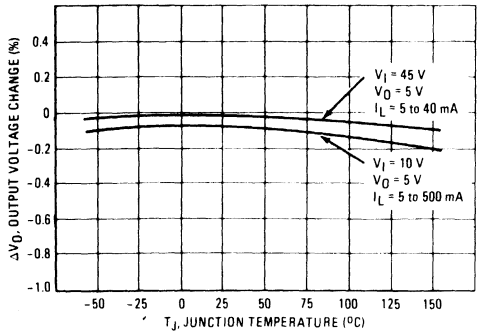


FIGURE 6 – RIPPLE REJECTION

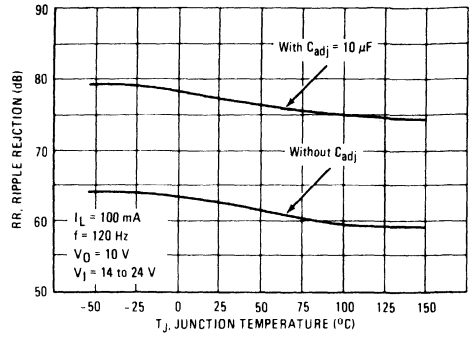


FIGURE 7 – CURRENT LIMIT

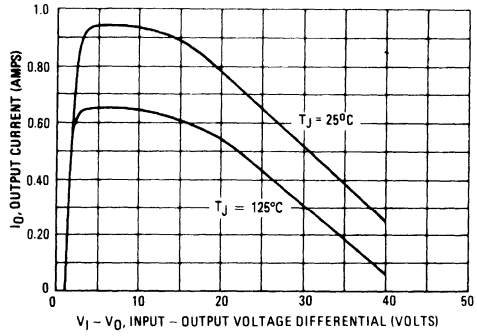


FIGURE 8 – DROPOUT VOLTAGE

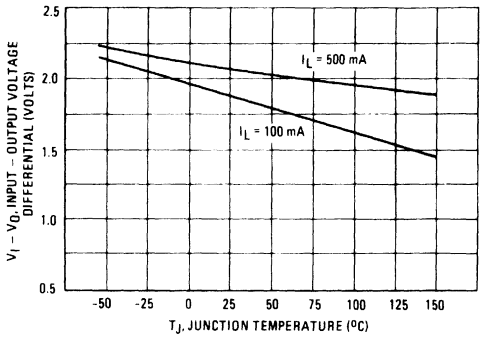


FIGURE 9 – MINIMUM OPERATING CURRENT

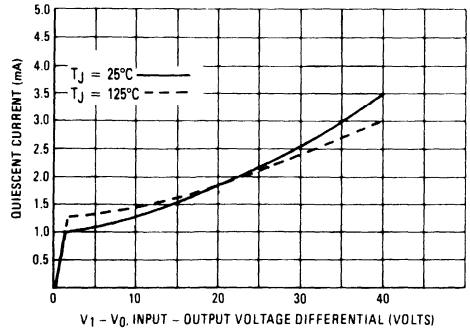


FIGURE 10 – RIPPLE REJECTION versus FREQUENCY

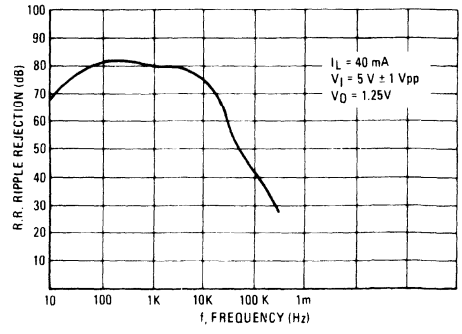


FIGURE 11 – TEMPERATURE STABILITY

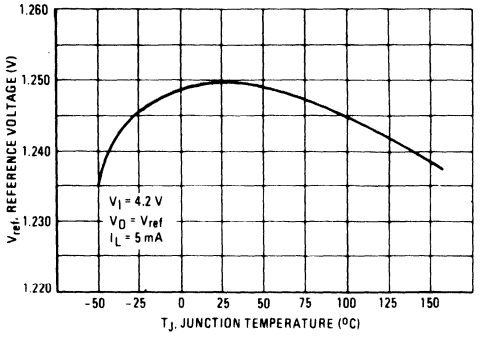


FIGURE 12 – ADJUSTMENT PIN CURRENT

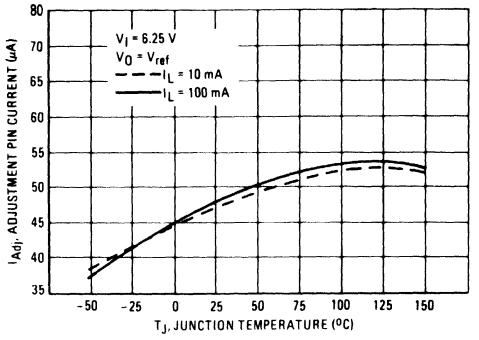


FIGURE 13 – LINE REGULATION

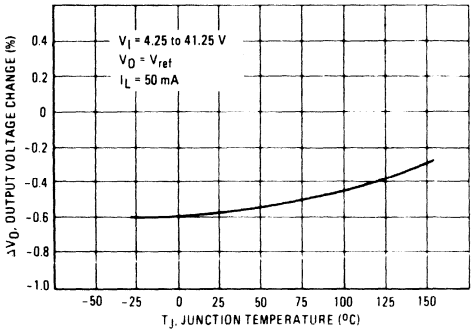


FIGURE 14 – OUTPUT NOISE

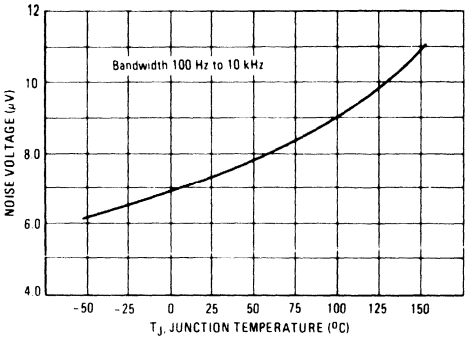


FIGURE 15 – LINE TRANSIENT RESPONSE

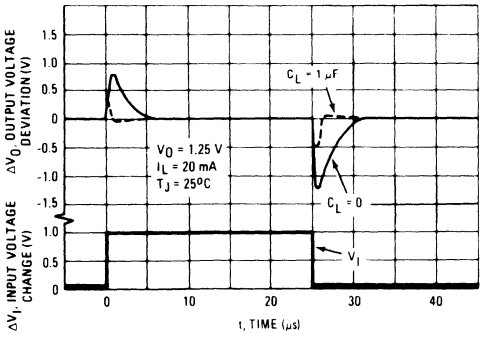
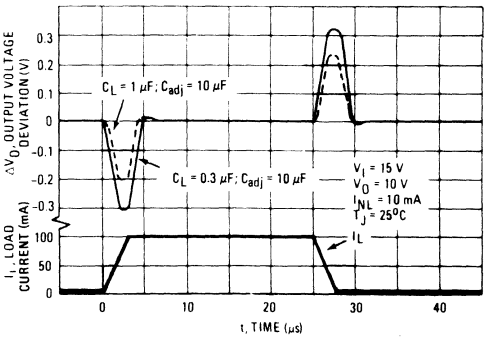


FIGURE 16 – LOAD TRANSIENT RESPONSE



APPLICATIONS INFORMATION

BASIC CIRCUIT OPERATION

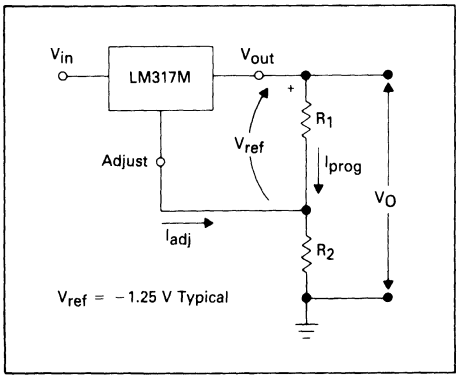
The LM317M is a 3-terminal floating regulator. In operation, the LM317M develops and maintains a nominal 1.25 volt reference (V_{ref}) between its output and adjustment terminals. This reference voltage is converted to a programming current (I_{prog}) by R1 (see Figure 17), and this constant current flows through R2 to ground. The regulated output voltage is given by:

$$V_O = V_{ref}(1 + \frac{R2}{R1}) + I_{adj}R2$$

Since the current from the adjustment terminal (I_{adj}) represents an error term in the equation, the LM317M was designed to control I_{adj} to less than 100 μA and keep it constant. To do this, all quiescent operating current is returned to the output terminal. This imposes the requirement for a minimum load current. If the load current is less than this minimum, the output voltage will rise.

Since the LM317M is a floating regulator, it is only the voltage differential across the circuit that is important to performance, and operation at high voltages with respect to ground is possible.

FIGURE 17 — BASIC CIRCUIT CONFIGURATION



LOAD REGULATION

The LM317M is capable of providing extremely good load regulation, but a few precautions are needed to obtain maximum performance. For best performance, the programming resistor (R1) should be connected as close to the regulator as possible to minimize line drops which effectively appear in series with the reference, thereby degrading regulation. The ground end of R2 can be returned near the load ground to provide remote ground sensing and improve load regulation.

EXTERNAL CAPACITORS

A 0.1 μF disc or 1 μF tantalum input bypass capacitor (C_{in}) is recommended to reduce the sensitivity to input line impedance.

The adjustment terminal may be bypassed to ground to improve ripple rejection. This capacitor (C_{adj}) prevents ripple from being amplified as the output voltage is increased. A 10 μF capacitor should improve ripple rejection about 15 dB at 120 Hz in a 10 volt application.

Although the LM317M is stable with no output capacitance, like any feedback circuit, certain values of external capacitance can cause excessive ringing. An output capacitance (C_O) in the form of a 1 μF tantalum or 25 μF aluminum electrolytic capacitor on the output swamps this effect and insures stability.

PROTECTION DIODES

When external capacitors are used with any I.C. regulator it is sometimes necessary to add protection diodes to prevent the capcitors from discharging through low current points into the regulator.

Figure 18 shows the LM317M with the recommended protection diodes for output voltages in excess of 25 V or high capacitance values ($C_O > 25$ μF, $C_{adj} > 5.0$ μF). Diode D1 prevents C_O from discharging thru the I.C. during an input short circuit. Diode D2 protects against capacitor C_{adj} discharging through the I.C. during an output short circuit. The combination of diodes D1 and D2 prevents C_{adj} from discharging through the I.C. during an input short circuit.

FIGURE 18 — VOLTAGE REGULATOR WITH PROTECTION DIODES

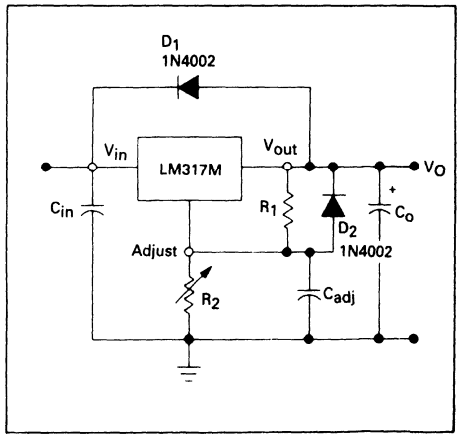


FIGURE 19 – ADJUSTABLE CURRENT LIMITER

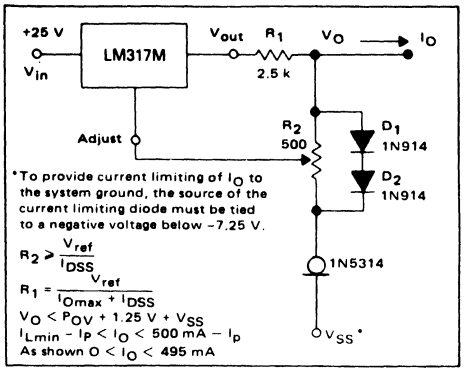


FIGURE 20 – 5 V ELECTRONIC SHUTDOWN REGULATOR

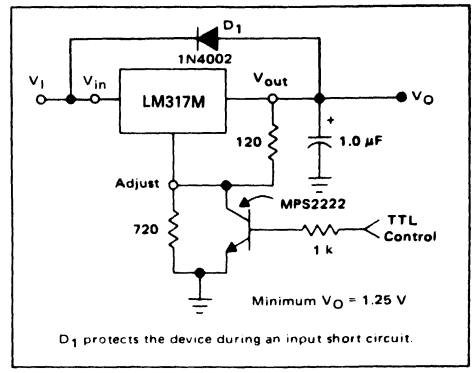


FIGURE 21 – SLOW TURN-ON REGULATOR

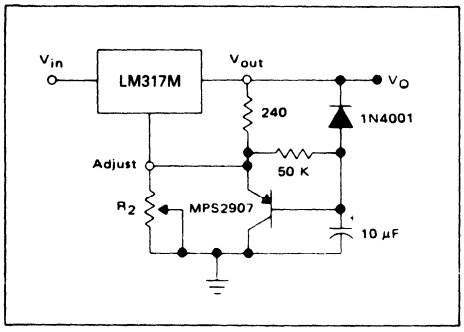
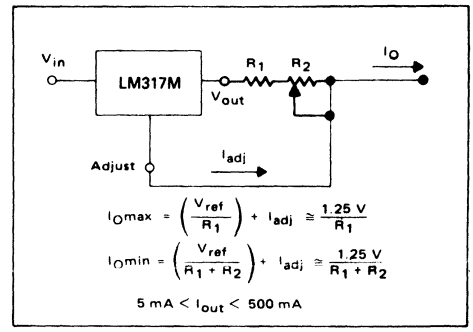


FIGURE 22 – CURRENT REGULATOR



MOTOROLA

LM337M

Specifications and Applications Information

THREE-TERMINAL ADJUSTABLE OUTPUT NEGATIVE VOLTAGE REGULATOR

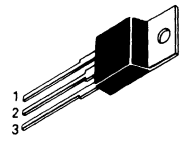
The LM337M is an adjustable 3-terminal negative voltage regulator capable of supplying in excess of 500 mA over an output voltage range of −1.2 V to −37 V. This voltage regulator is exceptionally easy to use and requires only two external resistors to set the output voltage. Further, it employs internal current limiting, thermal shutdown and safe area compensation, making it essentially blow-out proof.

The LM337M serves a wide variety of applications including local, on-card regulation. This device can also be used to make a programmable output regulator; or, by connecting a fixed resistor between the adjustment and output, the LM337M can be used as a precision current regulator.

- Output Current in Excess of 500 mA
- Output Adjustable Between −1.2 V and −37 V
- Internal Thermal Overload Protection
- Internal Short-Circuit-Current Limiting
- Output Transistor Safe-Area Compensation
- Floating Operation for High Voltage Applications
- Standard 3-Lead Transistor Packages
- Eliminates Stocking Many Fixed Voltages

MEDIUM-CURRENT THREE-TERMINAL ADJUSTABLE NEGATIVE VOLTAGE REGULATOR

SILICON MONOLITHIC INTEGRATED CIRCUIT



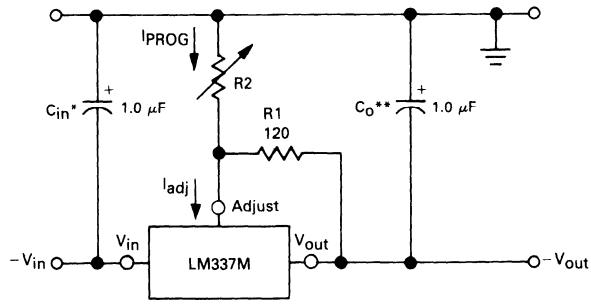
PIN 1. ADJUST
2. V_{in}
3. V_{out}

T SUFFIX
PLASTIC PACKAGE
CASE 221A-04

ORDERING INFORMATION

Device	Tested Operating Temperature Range	Package
LM337MT	T_J = 0°C to +125°C	Plastic Power

STANDARD APPLICATION



*C_{in} is required if regulator is located more than 4 inches from power supply filter. A 1.0 μF solid tantalum or 10 μF aluminum electrolytic is recommended.

**C_o is necessary for stability. A 1.0 μF solid tantalum or 10 μF aluminum electrolytic is recommended.

$$V_{out} = -1.25\ V\ (1 + \frac{R2}{R1})$$

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Input-Output Voltage Differential	V_I-V_O	40	Vdc
Power Dissipation	P_D	Internally Limited	
Operating Junction Temperature Range	T_J	0 to +150	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C

ELECTRICAL CHARACTERISTICS ($|V_I-V_O|$ = 5.0 V, I_O = 0.1; T_J = T_{low} to T_{high} [see Note 1], P_{max} per Note 2, unless otherwise specified.)

Characteristic	Figure	Symbol	Min	Typ	Max	Unit
Line Regulation (Note 3) T_A = 25°C, 3.0 V ≤ $\|V_I-V_O\|$ ≤ 40 V	1	Reg_{line}	—	0.01	0.04	%/V
Load Regulation (Note 3) T_A = 25°C, 10 mA ≤ I_O ≤ 0.5 A $\|V_O\|$ ≤ 5.0 V $\|V_O\|$ ≥ 5.0 V	2	Reg_{load}	 — —	 15 0.3	 50 1.0	 mV % V_O
Thermal Regulation 10 ms Pulse, T_A = 25°C	—	Reg_{therm}	—	0.03	0.04	%V_O/W
Adjustment Pin Current	3	I_{adj}	—	65	100	μA
Adjustment Pin Current Change 2.5 V ≤ $\|V_I-V_O\|$ ≤ 40 V, 10 mA ≤ I_L ≤ 0.5 A, P_D ≤ P_{max}, T_A = 25°C	1,2	ΔI_{adj}	—	2.0	5.0	μA
Reference Voltage (Note 4) 3.0 V ≤ $\|V_I-V_O\|$ ≤ 40 V, 10 mA ≤ I_O ≤ 0.5 A, P_D ≤ P_{max}, T_A = 25°C T_{low} to T_{high}	3	V_{ref}	 −1.213 −1.20	 −1.250 −1.25	 −1.287 −1.30	V
Line Regulation (Note 3) 3.0 V ≤ $\|V_I-V_O\|$ ≤ 40 V	1	Reg_{line}	—	0.02	0.07	%/V
Load Regulation (Note 3) 10 mA ≤ I_O ≤ 0.5 A $\|V_O\|$ ≤ 5.0 V $\|V_O\|$ ≥ 5.0 V	2	Reg_{load}	 — —	 20 0.3	 70 1.5	 mV % V_O
Temperature Stability (T_{low} ≤ T_J ≤ T_{high})	3	T_S	—	0.6	—	% V_O
Minimum Load Current to Maintain Regulation ($\|V_I-V_O\|$ ≤ 10 V) ($\|V_I-V_O\|$ ≤ 40 V)	3	I_{Lmin}	 — —	 1.5 2.5	 6.0 10	mA
Maximum Output Current $\|V_I-V_O\|$ ≤ 15 V, P_D ≤ P_{max} $\|V_I-V_O\|$ = 40 V, P_D ≤ P_{max}, T_A = 25°C	3	I_{max}	 0.5 0.1	 0.9 0.25	 — —	A
RMS Noise, % of V_O T_A = 25°C, 10 Hz ≤ f ≤ 10 kHz	—	N	—	0.003	—	% V_O
Ripple Rejection, V_O = −10 V, f = 120 Hz (Note 5) Without C_{adj} C_{adj} = 10 μF	4	RR	 — 66	 60 77	 — —	dB
Long Term Stability, T_J = T_{high} (Note 6) T_A = 25°C for Endpoint Measurements	3	S	—	0.3	1.0	%/1.0 k Hrs.
Thermal Resistance Junction to Case	—	$R_{\theta JC}$	—	7.0	—	°C/W

NOTES:
(1) T_{low} to T_{high} = 0°C to +125°C

(2) P_{max} = 7.5 W

(3) Load and line regulation are specified at constant junction temperature. Changes in V_O due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

(4) Selected devices with tightened tolerance reference voltage available.

(5) C_{adj}, when used, is connected between the adjustment pin and ground.

(6) Since Long Term Stability cannot be measured on each device before shipment, this specification is an engineering estimate of average stability from lot to lot.

SCHEMATIC DIAGRAM

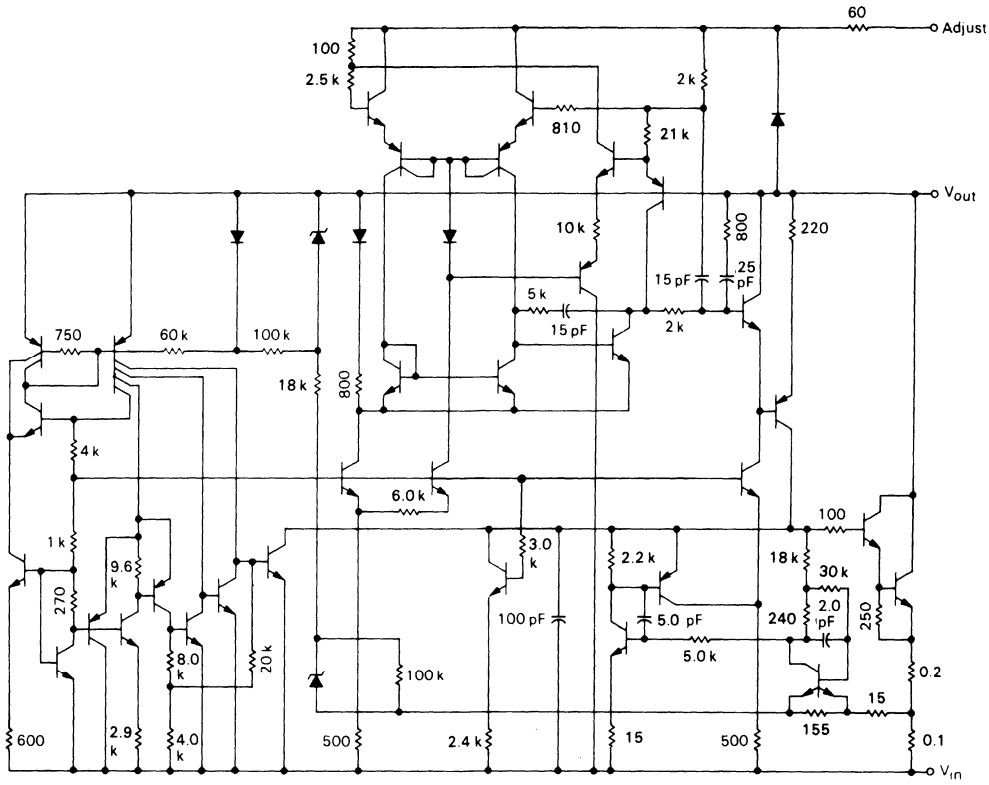


FIGURE 1 – LINE REGULATION AND ΔI_{adj}/LINE TEST CIRCUIT

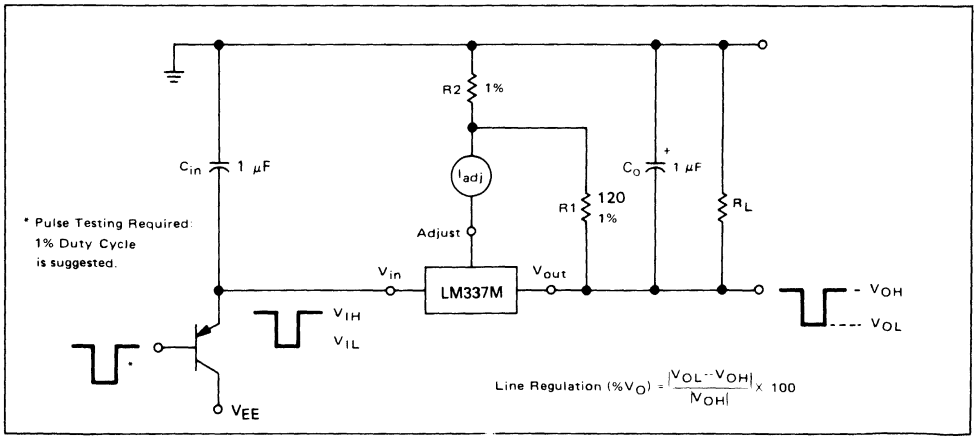


FIGURE 2 – LOAD REGULATION AND ΔI_{adj}/LOAD TEST CIRCUIT

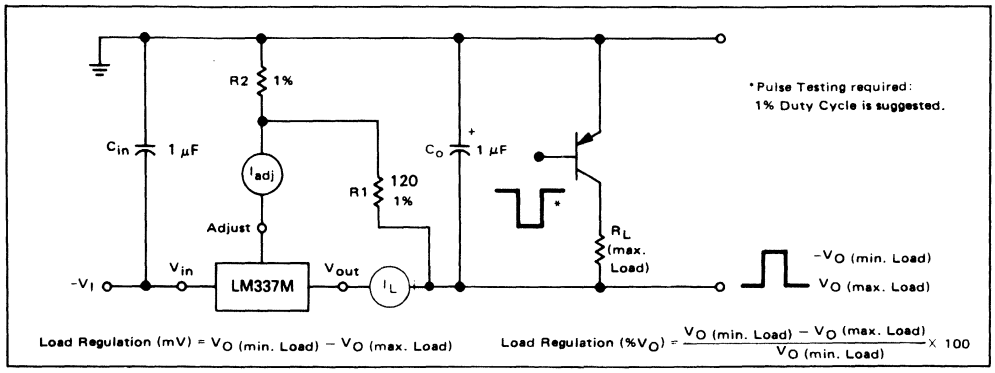


FIGURE 3 – STANDARD TEST CIRCUIT

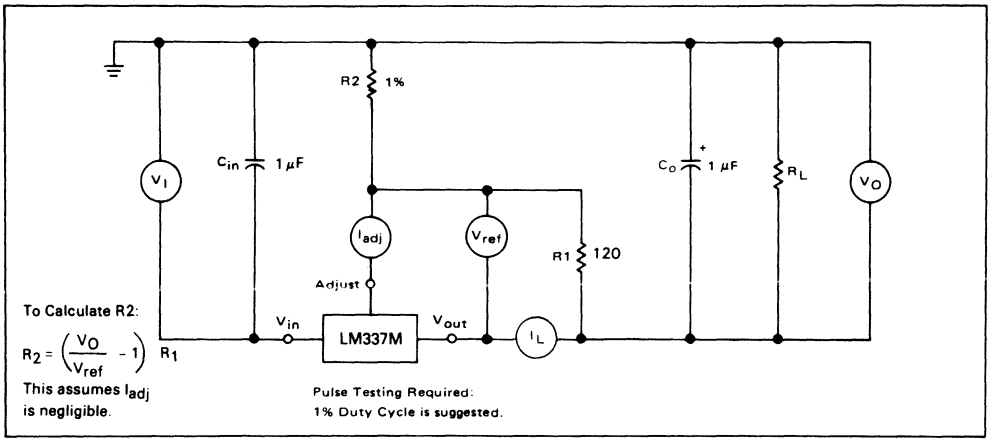


FIGURE 4 – RIPPLE REJECTION TEST CIRCUIT

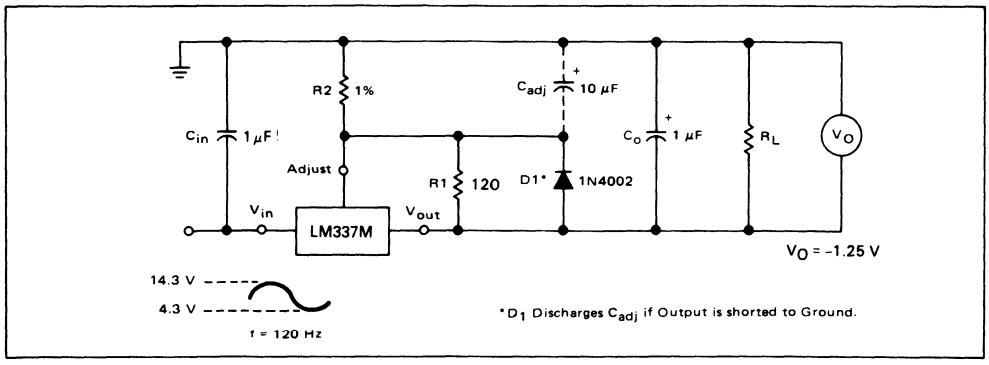


FIGURE 5 – LOAD REGULATION

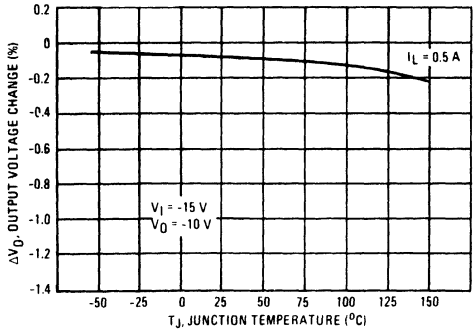


FIGURE 6 – CURRENT LIMIT

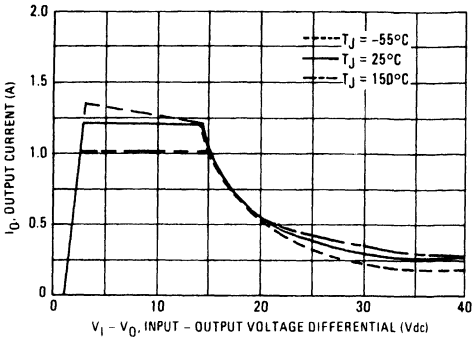


FIGURE 7 – ADJUSTMENT PIN CURRENT

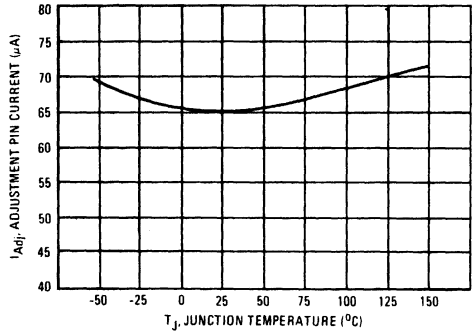


FIGURE 8 – DROPOUT VOLTAGE

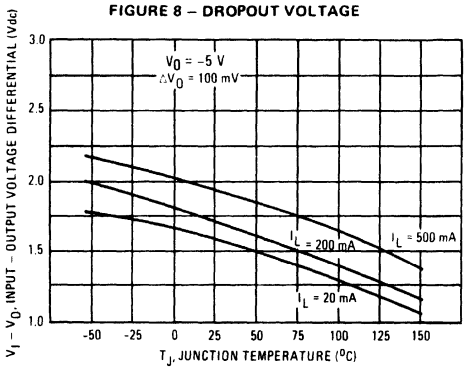


FIGURE 9 – TEMPERATURE STABILITY

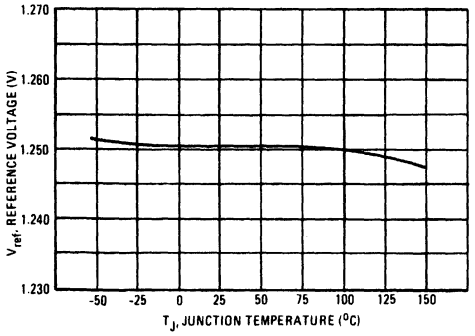


FIGURE 10 – MINIMUM OPERATING CURRENT

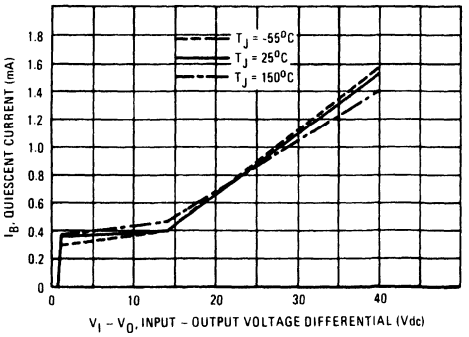


FIGURE 11 — RIPPLE REJECTION versus OUTPUT VOLTAGE

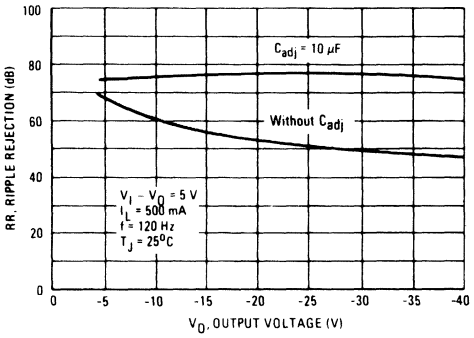


FIGURE 12 — RIPPLE REJECTION versus OUTPUT CURRENT

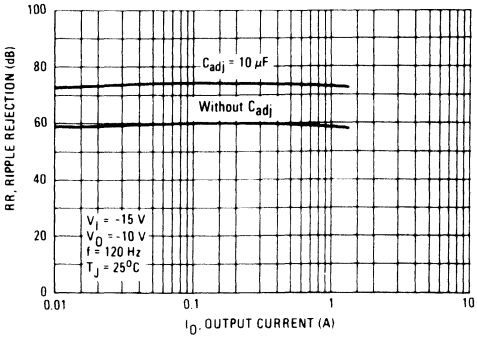


FIGURE 13 — RIPPLE REJECTION versus FREQUENCY

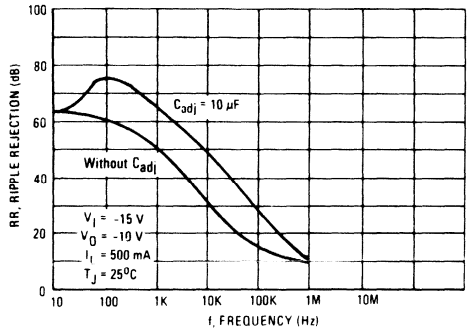


FIGURE 14 — OUTPUT IMPEDANCE

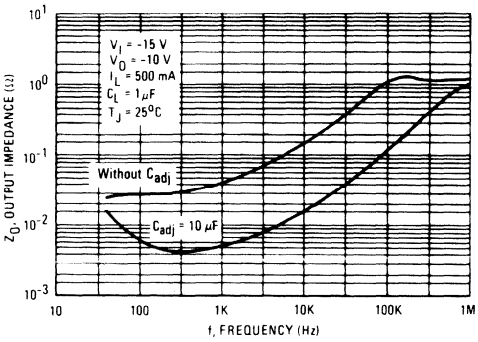


FIGURE 15 — LINE TRANSIENT RESPONSE

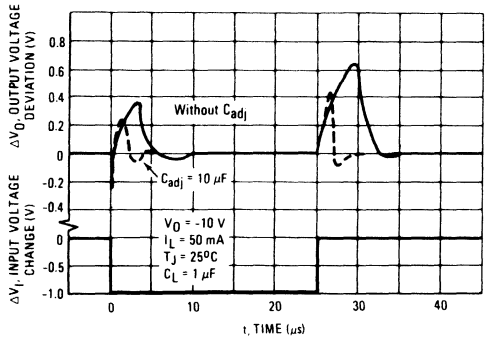
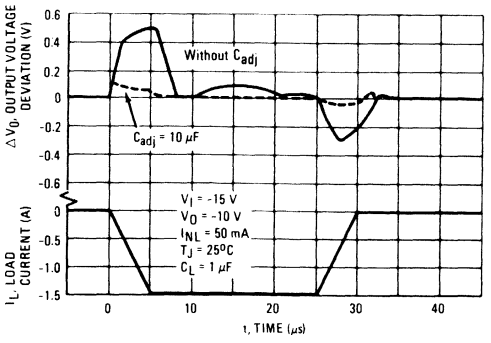


FIGURE 16 — LOAD TRANSIENT RESPONSE



APPLICATIONS INFORMATION

BASIC CIRCUIT OPERATION

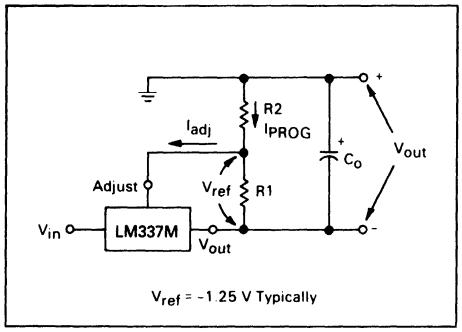
The LM337M is a 3-terminal floating regulator. In operation, the LM337M develops and maintains a nominal −1.25 volt reference (V_{ref}) between its output and adjustment terminals. This reference voltage is converted to a programming current (I_{PROG}) by R1 (see Figure 17), and this constant current flows through R2 from ground. The regulated output voltage is given by:

$$V_{out} = V_{ref}\left(1 + \frac{R2}{R1}\right) + I_{adj}R2$$

Since the current into the adjustment terminal (I_{adj}) represents an error term in the equation, the LM337M was designed to control I_{adj} to less than 100 μA and keep it constant. To do this, all quiescent operating current is returned to the output terminal. This imposes the requirement for a minimum load current. If the load current is less than this minimum, the output voltage will increase.

Since the LM337M is a floating regulator, it is only the voltage differential across the circuit that is important to performance, and operation at high voltages with respect to ground is possible.

FIGURE 17— BASIC CIRCUIT CONFIGURATION



V_{ref} = −1.25 V Typically

LOAD REGULATION

The LM337M is capable of providing extremely good load regulation, but a few precautions are needed to obtain maximum performance. For best performance, the programming resistor (R1) should be connected as close to the regulator as possible to minimize line drops which effectively appear in series with the reference, thereby degrading regulation. The ground end of R2 can be returned near the load ground to provide remote ground sensing and improve load regulation.

EXTERNAL CAPACITORS

A 1.0 μF tantalum input bypass capacitor (C_{in}) is recommended to reduce the sensitivity to input line impedance.

The adjustment terminal may be bypassed to ground to improve ripple rejection. This capacitor (C_{adj}) prevents ripple from being amplified as the output voltage is increased. A 10 μF capacitor should improve ripple rejection about 15 dB at 120 Hz in a 10 volt application.

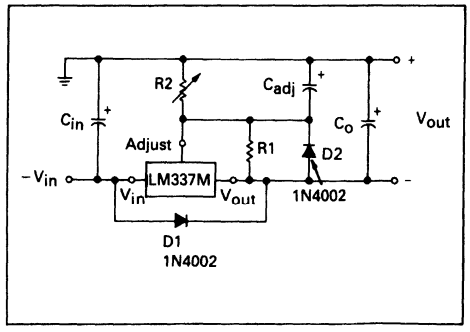
An output capacitor (C_O) in the form of a 1.0 μF tantalum or 10 μF aluminum electrolytic capacitor is required for stability.

PROTECTION DIODES

When external capacitors are used with any I.C. regulator it is sometimes necessary to add protection diodes to prevent the capacitors from discharging through low current points into the regulator.

Figure 18 shows the LM337M with the recommended protection diodes for output voltages in excess of −25 V or high capacitance values (C_O > 25 μF, C_{adj} > 10 μF). Diode D_1 prevents C_O from discharging thru the I.C. during an input short circuit. Diode D_2 protects against capacitor C_{adj} discharging through the I.C. during an output short circuit. The combination of diodes D1 and D2 prevents C_{adj} from discharging through the I.C. during an input short circuit.

FIGURE 18— VOLTAGE REGULATOR WITH PROTECTION DIODES



MOTOROLA

LM2931 Series

LOW DROPOUT VOLTAGE REGULATORS

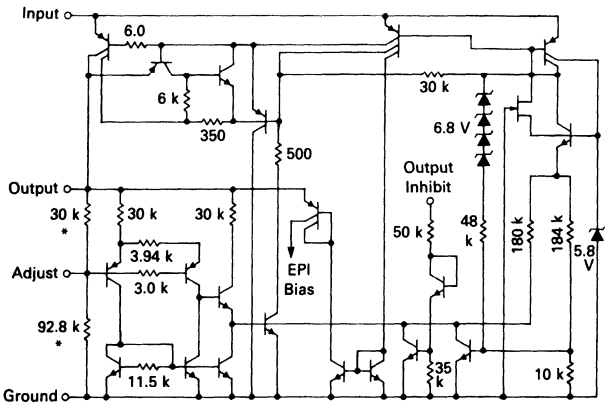
The LM2931 series consists of positive fixed and adjustable output voltage regulators that are specifically designed to maintain proper regulation with an extremely low input-to-output voltage differential. These devices are capable of supplying output currents in excess of 100 mA and feature a low bias current of 0.4 mA at 10 mA output.

Designed primarily to survive in the harsh automotive environment, these devices will protect all external load circuitry from input fault conditions caused by reverse battery connection, two battery jump starts, and excessive line transients during load dump. This series also includes internal current limiting, thermal shutdown, and additionally, is able to withstand temporary power-up with mirror-image insertion.

Due to the low dropout voltage and bias current specifications, the LM2931 series is ideally suited for battery powered industrial and consumer equipment where an extension of useful battery life is desirable. The 'C' suffix adjustable output regulators feature an output inhibit pin which is extremely useful in microprocessor-based systems.

- Input-to-Output Voltage Differential of Less Than 0.6 V at 100 mA
- Output Current in Excess of 100 mA
- Low Bias Current
- 60 V Load Dump Protection
- −50 V Reverse Transient Protection
- Internal Current Limiting with Thermal Shutdown
- Temporary Mirror-Image Protection
- Ideally Suited for Battery Powered Equipment

INTERNAL SCHEMATIC



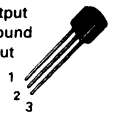
*Deleted on Adjustable Regulators

LOW DROPOUT VOLTAGE REGULATORS

SILICON MONOLITHIC INTEGRATED CIRCUITS

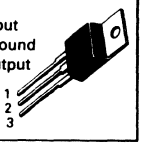
Z SUFFIX
PLASTIC PACKAGE
CASE 29-04

Pin 1. Output
2. Ground
3. Input

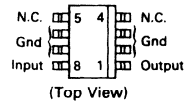


T SUFFIX
PLASTIC PACKAGE
CASE 221A-04
(Heatsink surface connected to Pin 2)

Pin 1. Input
2. Ground
3. Output

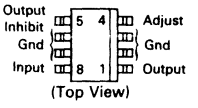


FIXED



(Top View)

ADJUSTABLE



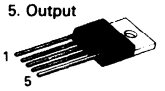
(Top View)

D SUFFIX
PLASTIC PACKAGE
CASE 751-03
(SOP-8)

ADJUSTABLE

T SUFFIX
PLASTIC PACKAGE
CASE 314D-02
(Heatsink surface connected to Pin 3)

Pin 1. Adjust
2. Output Inhibit
3. Ground
4. Input
5. Output



ORDERING INFORMATION

Device	Output Voltage	Output Tolerance	Package Case Number
LM2931AD-5.0	5.0 V	±2.5%	751
LM2931AT-5.0	5.0 V	±2.5%	221A
LM2931AZ-5.0	5.0 V	±2.5%	29
LM2931D-5.0	5.0 V	±5.0%	751
LM2931T-5.0	5.0 V	±5.0%	221A
LM2931Z-5.0	5.0 V	±5.0%	29
LM2931CD	Adjustable	±5.0%	751
LM2931CT	Adjustable	±5.0%	314D

DS9677R1

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Input Voltage Continuous	V_{in}	40	Vdc
Transient Input Voltage ($\tau \leq 100$ ms)	$V_{in(\tau)}$	60	V_{pk}
Transient Reverse Polarity Input Voltage 1.0% Duty Cycle, $\tau \leq 100$ ms	$-V_{in(\tau)}$	−50	V_{pk}
Power Dissipation			
Case 29-04 (TO-92)			
T_A = 25°C	P_D	Internally Limited	Watts
Thermal Resistance Junction to Ambient	θ_{JA}	178	°C/W
Thermal Resistance Junction to Case	θ_{JC}	83	°C/W
Case 751-02 (SOP-8)			
T_A = 25°C	P_D	Internally Limited	Watts
Thermal Resistance Junction to Ambient	θ_{JA}	180	°C/W
Thermal Resistance Junction to Case	θ_{JC}	45	°C/W
Case 221A-04 and 314D-02 (TO-220 Type)			
T_A = 25°C	P_D	Internally Limited	Watts
Thermal Resistance Junction to Ambient	θ_{JA}	65	°C/W
Thermal Resistance Junction to Case	θ_{JC}	5.0	°C/W
Tested Operating Junction Temperature Range	T_J	−40 to +125	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C

ELECTRICAL CHARACTERISTICS (V_{in} = 14 V, I_O = 10 mA, C_O = 100 μF, $C_{O(ESR)}$ = 0.3 Ω, T_J = 25°C, Note 1, unless otherwise noted.)

Characteristic	Symbol	LM2931A-5.0			LM2931-5.0			Unit
		Min	Typ	Max	Min	Typ	Max	
FIXED OUTPUT								
Output Voltage	V_O							V
V_{in} = 14 V, I_O = 10 mA, T_J = 25°C		4.81	5.0	5.19	4.75	5.0	5.25	
V_{in} = 6.0 V to 26 V, $I_O \leq$ 100 mA, T_J = −40 to 125°C		4.75	—	5.25	4.50	—	5.50	
Line Regulation	Reg_{line}							mV
V_{in} = 9.0 V to 16 V		—	2.0	10	—	2.0	10	
V_{in} = 6.0 V to 26 V		—	4.0	30	—	4.0	30	
Load Regulation (I_O = 5.0 mA to 100 mA)	Reg_{load}	—	14	50	—	14	50	mV
Output Impedance I_O = 10 mA, ΔI_O = 1.0 mA, f = 100 Hz to 10 kHz	Z_O	—	200	—	—	200	—	mΩ
Bias Current	I_B							mA
V_{in} = 14 V, I_O = 100 mA, T_J = 25°C		—	5.8	30	—	5.8	30	
V_{in} = 6.0 V to 26 V, I_O = 10 mA, T_J = −40 to 125°C		—	0.4	1.0	—	0.4	1.0	
Output Noise Voltage (f = 10 Hz to 100 kHz)	V_n	—	700	—	—	700	—	μVrms
Long-Term Stability	S	—	20	—	—	20	—	mV/kHR
Ripple Rejection (f = 120 Hz)	RR	60	90	—	60	90	—	dB
Dropout Voltage	V_{in}-V_O							V
I_O = 10 mA		—	0.015	0.2	—	0.015	0.2	
I_O = 100 mA		—	0.16	0.6	—	0.16	0.6	
Over-Voltage Shutdown Threshold	$V_{th(OV)}$	26	29.5	40	26	29.5	40	V
Output Voltage with Reverse Polarity Input (V_{in} = −15 V)	$-V_O$	−0.3	0	—	−0.3	0	—	V

NOTES:
1) Low duty cycle pulse techniques are used during test to maintain junction temperature as close to ambient as possible.
2) The reference voltage on the adjustable device is measured from the output to the adjust pin across R_1.

ELECTRICAL CHARACTERISTICS (V_{in} = 14 V, V_O = 3.0 V, I_O = 10 mA, R_1 = 27 k, C_O = 100 μF, $C_{O(ESR)}$ = 0.3 Ω, T_J = 25°C, Note 1, unless otherwise noted.)

Characteristic	Symbol	LM2931C Min	LM2931C Typ	LM2931C Max	Unit
ADJUSTABLE OUTPUT					
Reference Voltage (Note 2, Figure 18) I_O = 10 mA, T_J = 25°C $I_O \leq$ 100 mA, T_J = −40 to 125°C	V_{ref}	 1.14 1.08	 1.20 —	 1.26 1.32	V
Output Voltage Range	V_{Orange}	3.0	2.7 to 29.5	24	V
Line Regulation (V_{in} = V_O + 0.6 V to 26 V)	Reg_{line}	—	0.2	1.5	mV/V
Load Regulation (I_O = 5.0 mA to 100 mA)	Reg_{load}	—	0.3	1.0	%/V
Output Impedance I_O = 10 mA, ΔI_O = 1.0 mA, f = 10 Hz to 10 kHz	Z_O	—	40	—	mΩ/V
Bias Current I_O = 100 mA I_O = 10 mA Output Inhibited ($V_{th(OI)}$ = 2.5 V)	I_B	 — — —	 6.0 0.4 0.2	 — 1.0 1.0	mA
Adjustment Pin Current	I_{Adj}	—	0.2	—	μA
Output Noise Voltage (f = 10 Hz to 100 kHz)	V_n	—	140	—	μVrms/V
Long-Term Stability	S	—	0.4	—	%/kHR
Ripple Rejection (f = 120 Hz)	RR	0.10	0.003	—	%/V
Dropout Voltage I_O = 10 mA I_O = 100 mA	V_{in}-V_O	 — —	 0.015 0.16	 0.2 0.6	V
Over-Voltage Shutdown Threshold	$V_{th(OV)}$	26	29.5	40	V
Output Voltage with Reverse Polarity Input (V_{in} = −15 V)	$-V_O$	−0.3	0	—	V
Output Inhibit Threshold Voltages Output "On," T_J = 25°C T_J = −40 to 125°C Output "Off," T_J = 25°C T_J = −40 to 125°C	$V_{th(OI)}$	 — — 2.50 3.25	 2.15 — 2.26 —	 1.90 1.20 — —	V
Output Inhibit Threshold Current ($V_{th(OI)}$ = 2.5 V)	$I_{th(OI)}$	—	30	50	μA

NOTES:
1) Low duty cycle pulse techniques are used during test to maintain junction temperature as close to ambient as possible.
2) The reference voltage on the adjustable device is measured from the output to the adjust pin across R_1.

DEFINITIONS

Dropout Voltage — The input/output voltage differential at which the regulator output no longer maintains regulation against further reductions in input voltage. Measured when the output decreases 100 mV from nominal value at 14 V input, dropout voltage is affected by junction temperature and load current.

Line Regulation — The change in output voltage for a change in the input voltage. The measurement is made under conditions of low dissipation or by using pulse techniques such that the average chip temperature is not significantly affected.

Load Regulation — The change in output voltage for a change in load current at constant chip temperature.

Maximum Power Dissipation — The maximum total device dissipation for which the regulator will operate within specifications.

Bias Current — That part of the input current that is not delivered to the load.

Output Noise Voltage — The rms ac voltage at the output, with constant load and no input ripple, measured over a specified frequency range.

Long-Term Stability — Output voltage stability under accelerated life test conditions with the maximum rated voltage listed in the devices electrical characteristics and maximum power dissipation.

FIGURE 1 — DROPOUT VOLTAGE versus OUTPUT CURRENT

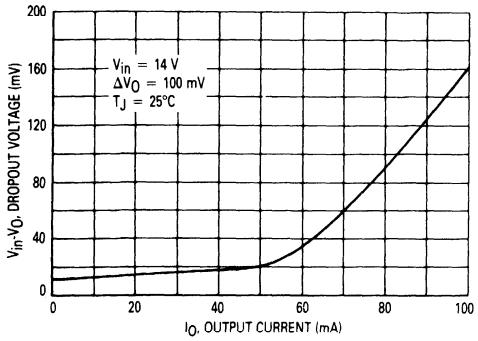


FIGURE 2 — DROPOUT VOLTAGE versus JUNCTION TEMPERATURE

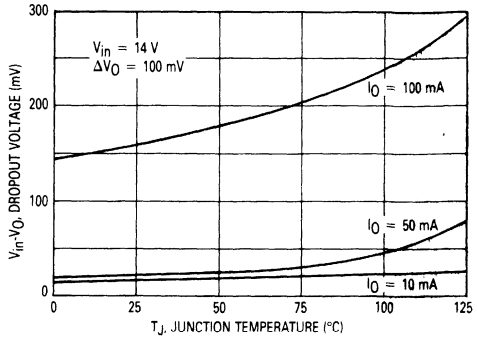


FIGURE 3 — PEAK OUTPUT CURRENT versus INPUT VOLTAGE

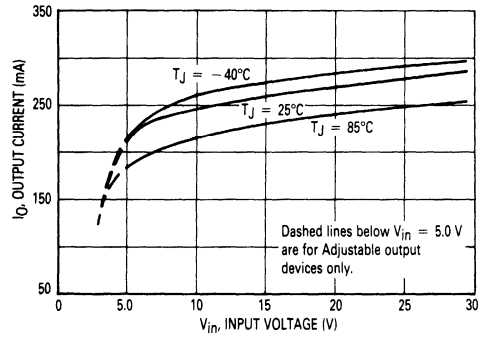


FIGURE 4 — OUTPUT VOLTAGE versus INPUT VOLTAGE

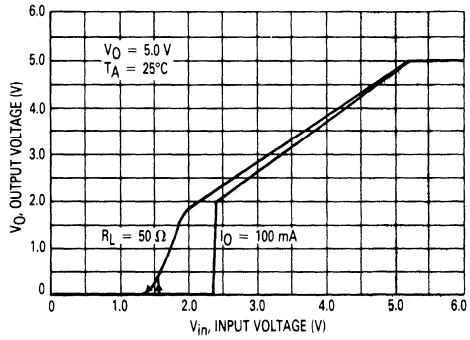


FIGURE 5 — OUTPUT VOLTAGE versus INPUT VOLTAGE

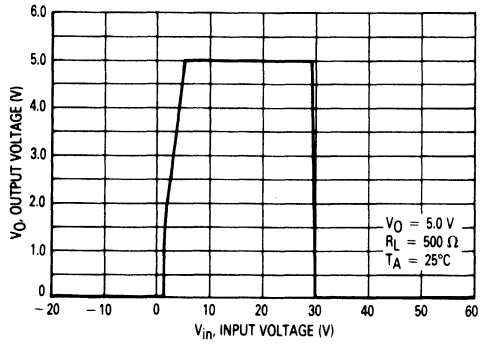


FIGURE 6 — LOAD DUMP CHARACTERISTICS

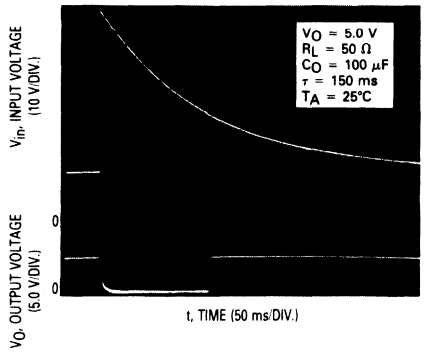


FIGURE 7 — BIAS CURRENT versus INPUT VOLTAGE

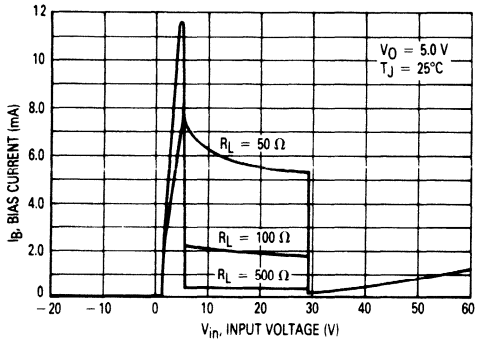


FIGURE 8 — BIAS CURRENT versus OUTPUT CURRENT

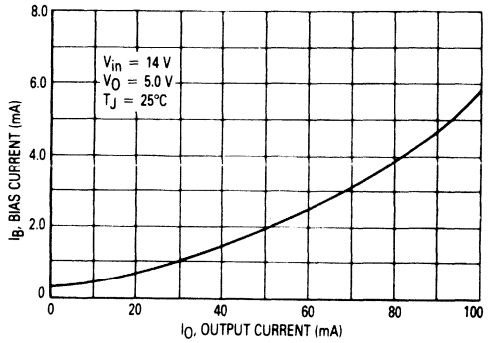


FIGURE 9 — BIAS CURRENT versus JUNCTION TEMPERATURE

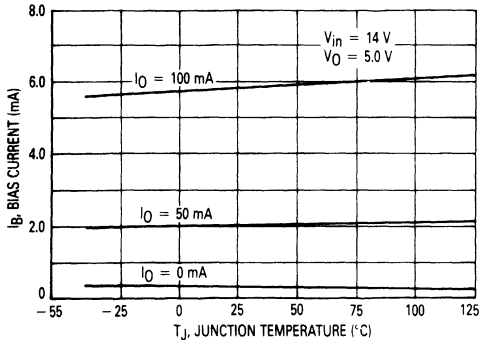


FIGURE 10 — OUTPUT IMPEDANCE versus FREQUENCY

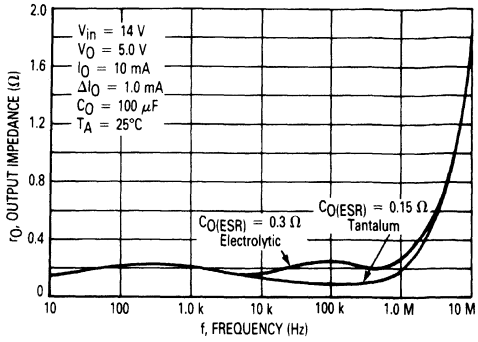


FIGURE 11 — RIPPLE REJECTION versus FREQUENCY

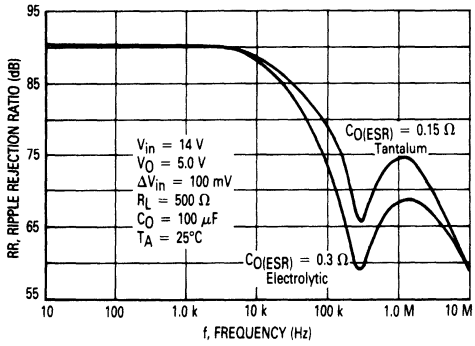


FIGURE 12 — RIPPLE REJECTION versus OUTPUT CURRENT

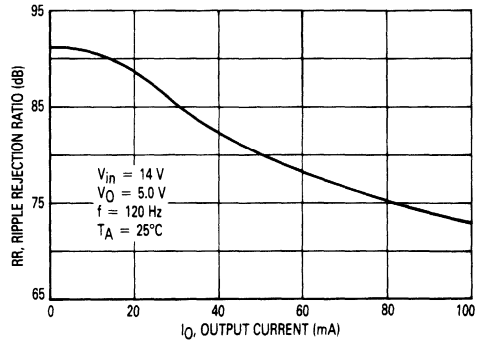


FIGURE 13 — LINE REGULATION

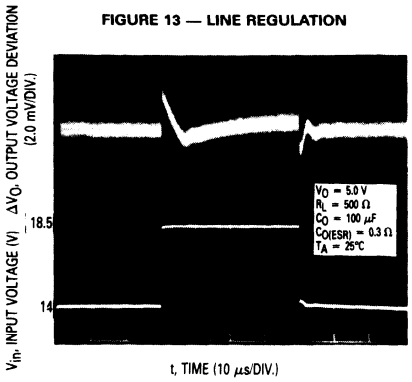


FIGURE 14 — LOAD REGULATION

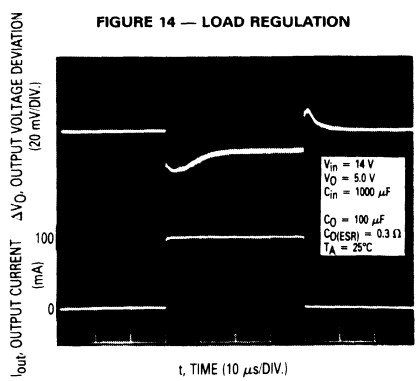


FIGURE 15 — REFERENCE VOLTAGE versus OUTPUT VOLTAGE

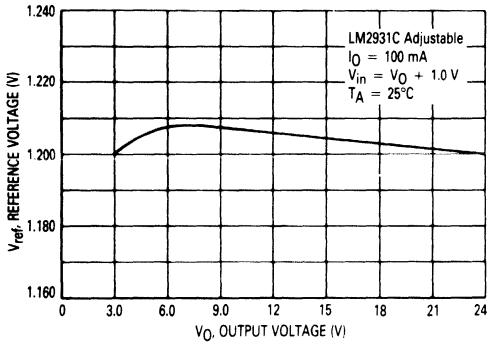
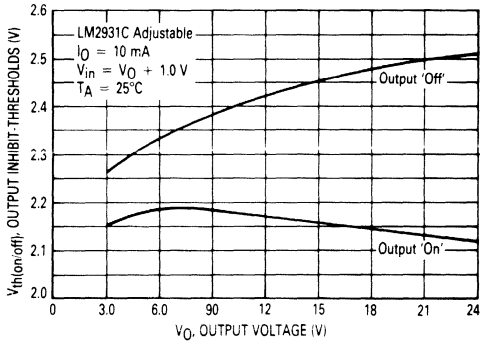


FIGURE 16 — OUTPUT INHIBIT-THRESHOLDS versus OUTPUT VOLTAGE



TYPICAL APPLICATIONS

FIGURE 17 — FIXED OUTPUT REGULATOR

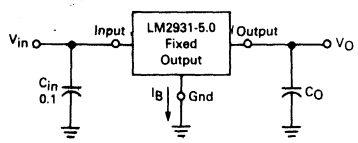
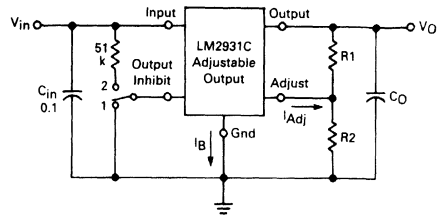


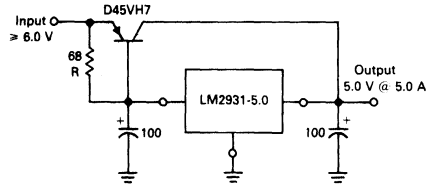
FIGURE 18 — ADJUSTABLE OUTPUT REGULATOR



Switch Position 1 = Output 'On,' 2 = Output 'Off'

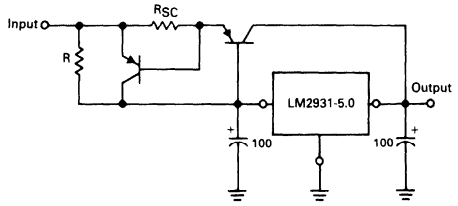
$$V_O = V_{ref}\left(1 + \frac{R2}{R1}\right) + I_{Adj}\,R2 \qquad 22.5\ k \geq \frac{R1\ R2}{R1 + R2}$$

FIGURE 19 — 5.0 A LOW DIFFERENTIAL VOLTAGE REGULATOR



The LM2931 series can be current boosted with a PNP transistor. The D45VH7, on a heatsink, will provide an output current of 5.0 A with an input to output voltage differential of approximately 1.0 V. Resistor R in conjunction with the V_{BE} of the PNP determines when the pass transistor begins conducting. This circuit is not short-circuit proof.

FIGURE 20 — CURRENT BOOST REGULATOR WITH SHORT-CIRCUIT PROJECTION



The circuit of Figure 19 can be modified to provide supply protection against short circuits by adding the current sense resistor R_{SC} and an additional PNP transistor. The current sensing PNP must be capable of handling the short-circuit current of the LM2931. Safe operating area of both transistors must be considered under worst case conditions.

FIGURE 21 — CONSTANT INTENSITY LAMP FLASHER

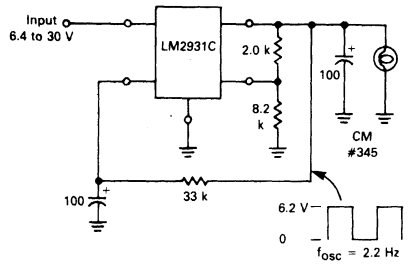
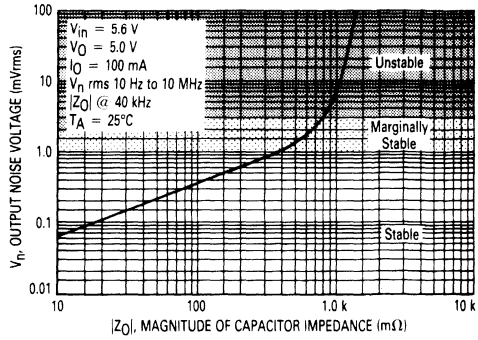


FIGURE 22 — OUTPUT NOISE VOLTAGE versus OUTPUT CAPACITOR IMPEDANCE



APPLICATIONS INFORMATION

The LM2931 series regulators are designed with many protection features making them essentially blow-out proof. These features include internal current limiting, thermal shutdown, overvoltage and reverse polarity input protection, and the capability to withstand temporary power-up with mirror-image insertion. Typical application circuits for the fixed and adjustable output device are shown in Figures 17 and 18.

The input bypass capacitor C_{in} is recommended if the regulator is located an appreciable distance ($\geq$ 4") from the supply input filter. This will reduce the circuit's sensitivity to the input line impedance at high frequencies.

This regulator series is not internally compensated and thus requires an external output capacitor for stability. The capacitance value required is dependent upon the load current, output voltage for the adjustable regulator, and the type of capacitor selected. The least stable condition is encountered at maximum load current and minimum output voltage. Figure 22 shows that for operation in the "Stable" region, under the conditions specified, the magnitude of the output capacitor impedance $|Z_O|$ must not exceed 0.4 Ω. This limit must be observed over the entire operating temperature range of the regulator circuit.

With economical electrolytic capacitors, cold temperature operation can pose a serious stability problem. As the electrolyte freezes, around −30°C, the capacitance will decrease and the equivalent series resistance ESR will increase drastically, causing the circuit to oscillate. Quality electrolytic capacitors with extended temperature ranges of −40 to 85°C and −55 to 105°C are readily available. Solid tantalum capacitors may be a better choice if small size is a requirement, however, the maximum $|Z_O|$ limit over temperature must be observed.

Note that in the stable region, the output noise voltage is linearly proportional to $|Z_O|$. In effect, C_O dictates the high frequency roll-off point of the circuit. Operation in the area titled "Marginally Stable" will cause the output of the regulator to exhibit random bursts of oscillation that decay in an under-damped fashion. Continuous oscillation occurs when operating in the area titled "Unstable." It is suggested that oven testing of the entire circuit be performed with maximum load, minimum input voltage, and minimum ambient temperature.

MOTOROLA

MC1466L

Specifications and Applications Information

PRECISION WIDE RANGE VOLTAGE and CURRENT REGULATOR

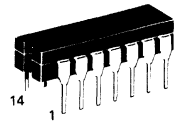
SILICON MONOLITHIC INTEGRATED CIRCUIT

PRECISION WIDE RANGE VOLTAGE AND CURRENT REGULATOR

This unique "floating" regulator can deliver hundreds of volts — limited only by the breakdown voltage of the external series pass transistor. Output voltage and output current are adjustable. The MC1466 integrated circuit voltage and current regulator is designed to give "laboratory" power-supply performance.

- Voltage/Current Regulation with Automatic Crossover
- Excellent Line Voltage Regulation, 0.03% +3.0 mV (Max)
- Excellent Load Voltage Regulation, 0.03% +3.0 mV (Max)
- Excellent Current Regulation, 0.2% +1.0 mA
- Short-Circuit Protection
- Output Voltage Adjustable to Zero Volts
- Internal Reference Voltage
- Adjustable Internal Current Source

L SUFFIX
CERAMIC PACKAGE
CASE 632-08



ORDERING INFORMATION		
Device	Temperature Range	Package
MC1466L	0°C to +70° C	Ceramic DIP

TYPICAL APPLICATIONS

FIGURE 1 – 0-TO-15 VDC, 10-AMPERES REGULATOR

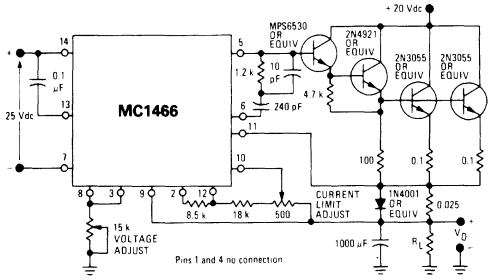


FIGURE 2 – 0-TO-40 VDC, 0.5-AMPERE REGULATOR

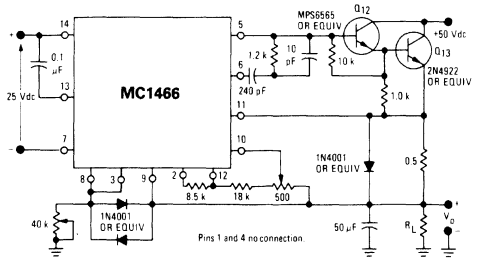


FIGURE 3 – 0-TO-250 VDC, 0.1-AMPERE REGULATOR

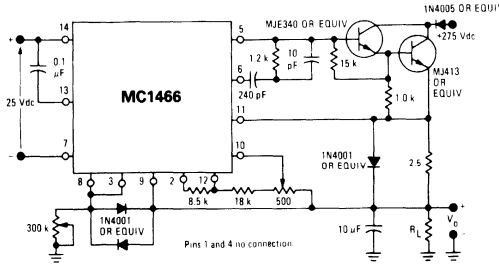
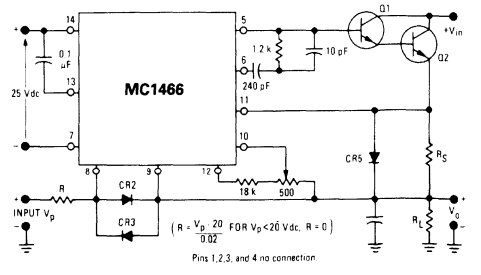


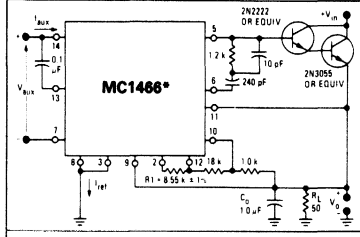
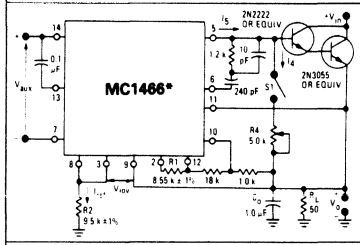
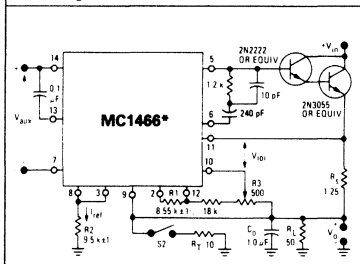
FIGURE 4 – REMOTE PROGRAMMING



MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Auxiliary Voltage	V_{aux}	30	Vdc
Power Dissipation (Package Limitation) Derate above T_A = +50°C	P_D $1/\theta_{JA}$	750 6.0	mW mW/°C
Operating Temperature Range	T_A	0 to +70	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C

ELECTRICAL CHARACTERISTICS (T_A = +25°C, V_{aux} = +25 Vdc unless otherwise noted)

Characteristic Definition	Characteristic	Symbol	Min	Typ	Max	Units
	Auxiliary Voltage (See Notes 1 & 2) (Voltage from pin 14 to pin 7)	V_{aux}	21	—	30	Vdc
	Auxiliary Current	I_{aux}	—	9.0	12	mAdc
	Internal Reference Voltage (Voltage from pin 12 to pin 7)	V_{IR}	17.3	18.2	19.7	Vdc
	Reference Current (See Note 3)	I_{ref}	0.8	1.0	1.2	mAdc
	Input Current — Pin 8	I_8	—	6.0	12	μAdc
	Power Dissipation	P_D	—	—	360	mW
	Input Offset Voltage, Voltage Control Amplifier (See Note 4)	V_{iov}	0	15	40	mVdc
	Load Voltage Regulation (See Note 5)	ΔV_{iov} $\Delta V_{ref}/V_{ref}$	— —	1.0 0.015	3.0 0.03	mV %
	Line Voltage Regulation (See Note 6)	ΔV_{iov} $\Delta V_{ref}/V_{ref}$	— —	1.0 0.015	3.0 0.03	mV %
	Temperature Coefficient of Output Voltage (T_A = 0 to +75°C)	TCV_o	—	0.01	—	%/°C
	Input Offset Voltage, Current Control Amplifier (See Note 4) (Voltage from pin 10 to pin 11)	V_{ioi}	0	15	40	mVdc
	Load Current Regulation (See Note 7)	$\Delta I_L/I_L$ ΔI_{ref}	— —	0.2 —	— 1.0	% mAdc

*Pins 1 and 4 no connection.

NOTE 1:
The instantaneous input voltage, V_{aux}, must not exceed the maximum value of 30 volts for the MC1466. The instantaneous value of V_{aux} must be greater than 21 volts for the MC1466 for proper internal regulation.

NOTE 2:
The auxiliary supply voltage V_{aux}, must "float" and be electrically isolated from the unregulated high voltage supply, V_{in}.

NOTE 3:
Reference current may be set to any value of current less than 1.2 mAdc by applying the relationship:

$$I_{ref}\ (mA) = \frac{8.55}{R_1\ (k\Omega)}.$$

NOTE 4:
A built-in offset voltage (15 mVdc nominal) is provided so that the power supply output voltage or current may be adjusted to zero.

NOTE 5:
Load Voltage Regulation is a function of two additive components, ΔV_{iov} and ΔV_{ref}, where ΔV_{iov} is the change in input offset voltage (measured between pins 8 and 9) and ΔV_{ref} is the change in voltage across R2 (measured between pin 8 and ground). Each component may be measured separately or the sum may be measured across the load. The measurement procedure for the test circuit shown is:

a. With S1 open (I_4 = 0) measure the value of $V_{iov\ (1)}$ and $V_{ref\ (1)}$.
b. Close S1, adjust R4 so that I_4 = 500 μA and note $V_{iov\ (2)}$ and $V_{ref\ (2)}$.

Then $\Delta V_{iov} = V_{iov\ (1)} - V_{iov\ (2)}$

% Reference Regulation =

$$\frac{[V_{ref\ (1)} - V_{ref\ (2)}]}{V_{ref\ (1)}}\ (100\%) = \frac{\Delta V_{ref}}{V_{ref}}\ (100\%)$$

Load Voltage Regulation =

$$\frac{\Delta V_{ref}}{V_{ref}}\ (100\%) + \Delta V_{iov}.$$

NOTE 6:
Line Voltage Regulation is a function of the same two additive components as Load Voltage Regulation, ΔV_{iov} and ΔV_{ref} (see Note 5). The measurement procedure is:

a. Set the auxiliary voltage, V_{aux}, to 22 volts. Read the value of $V_{iov\ (1)}$ and $V_{ref\ (1)}$.
b. Change the V_{aux} to 28 volts and note the value of $V_{iov\ (2)}$ and $V_{ref\ (2)}$. Then compute Line Voltage Regulation:

$\Delta V_{iov} = \Delta V_{iov\ (1)} - V_{iov\ (2)}$

% Reference Regulation =

$$\frac{[V_{ref\ (1)} - V_{ref\ (2)}]}{V_{ref\ (1)}}\ (100\%) = \frac{\Delta V_{ref}}{V_{ref}}\ (100\%)$$

Line Voltage Regulation =

$$\frac{\Delta V_{ref}}{V_{ref}}\ (100\%) + \Delta V_{iov}.$$

NOTE 7:
Load Current Regulation is measured by the following procedure:

a. With S2 open, adjust R3 for an initial load current, $I_{L(1)}$, such that V_O is 8.0 Vdc.
b. With S2 closed, adjust R_T for V_O = 1.0 Vdc and read $I_{L(2)}$.

Then Load Current Regulation =

$$\frac{[I_{L(2)} - I_{L(1)}]}{I_{L(1)}}\ (100\%) + I_{ref}$$

where I_{ref} is 1.0 mAdc, Load Current Regulation is specified in this manner because I_{ref} passes through the load in a direction opposite that of load current and does not pass through the current sense resistor, R_S.

FIGURE 5

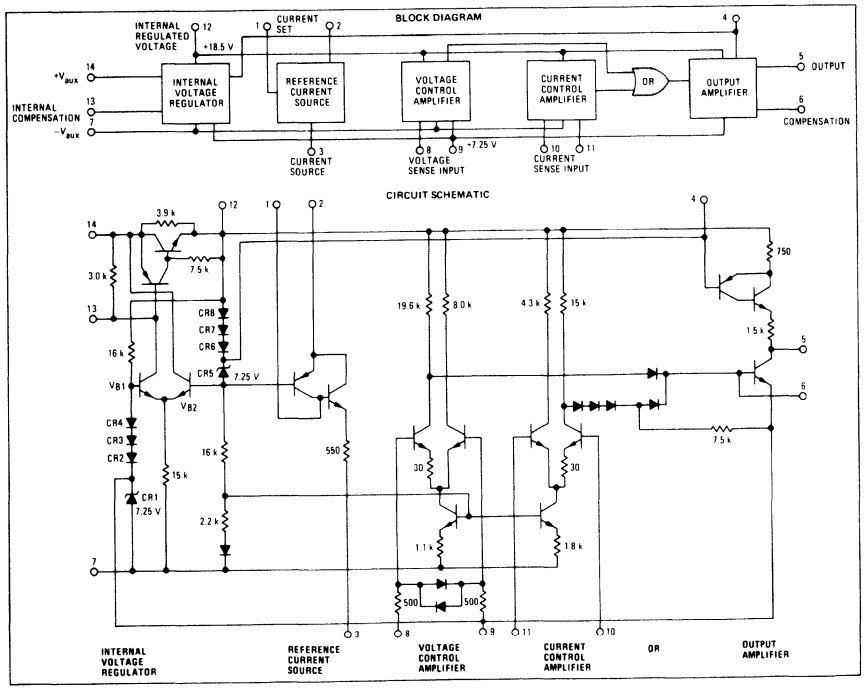
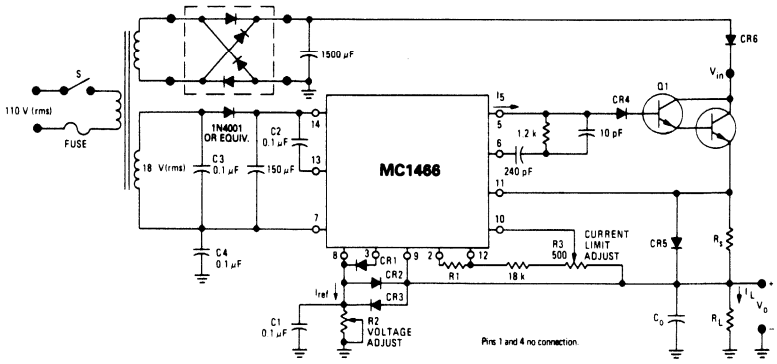
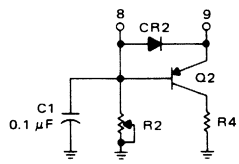


FIGURE 6 – TYPICAL CIRCUIT CONNECTION



NORMAL DESIGN PROCEDURE AND DESIGN CONSIDERATIONS

1. Constant Voltage:
   For constant voltage operation, output voltage V_O is given by:
   $V_O = (I_{ref})(R_2)$
   where R2 is the resistance from pin 8 to ground and I_{ref} is the output current of pin 3.
   The recommended value of I_{ref} is 1.0 mAdc. Resistor R1 sets the value of I_{ref}:
   $$I_{ref} = \frac{8.5}{R_1}$$
   where R1 is the resistance between pins 2 and 12.
2. Constant Current:
   For constant current operation:
   (a) Select R_S for a 250 mV drop at the maximum desired regulated output current, I_{max}.
   (b) Adjust potentiometer R3 to set constant current output at desired value between zero and I_{max}.
3. If V_{in} is greater than 20 Vdc, CR2, CR3, and CR4 are necessary to protect the MC1466 during short circuit or transient conditions.
4. In applications where very low output noise is desired, R2 may be bypassed with C1 (0.1 μF to 2.0 μF). When R2 is bypassed, CR1 is necessary for protection during short circuit conditions.
5. CR5 is recommended to protect the MC1466 from simultaneous pass transistor failure and output short circuit.
6. The RC network (10 pF, 240 pF, 1.2 kΩ) is used for compensation. The values shown are valid for all applications. However, the 10 pF capacitor may be omitted if f_T of Q1 and Q2 is greater than 0.5 MHz.
7. For remote sense applications, the positive voltage sense terminal (Pin 9) is connected to the positive load terminal through a separate sense lead; and the negative sense terminal (the ground side of R2) is connected to the negative load terminal through a separate sense lead.
8. C_O may be selected by using the relationship:
   $C_O = (100\ \mu F)\ I_{L(max)}$, where $I_{L(max)}$ is the maximum load current in amperes.
9. C2 is necessary for the internal compensation of the MC1466.
10. For optimum regulation, current out of Pin 5, I_5 should not exceed 0.5 mAdc. Therefore select Q1 and Q2 such that:
    $$\frac{I_{max}}{\beta 1 \beta 2} \leq 0.5\ \text{mAdc}$$
    where: I_{max} = maximum short-circuit load current (mAdc)
    $\beta 1$ = minimum beta of Q1
    $\beta 2$ = minimum beta of Q2
    Although Pin 5 will source up to 1.5 mAdc, $I_5 > 0.5$ mAdc will result in a degradation in regulation.
11. CR6 is recommended when $V_O > 150$ Vdc and should be rated such that Peak Inverse Voltage > V_O.
12. In applications where R2 might be rapidly reduced in value, it is recommended that CR3 be replaced by Q2 and R4.



This design consideration prevents R2 from being destroyed by excessive discharge current from C_O. Components Q2 and R4 should be selected such that:

$$R4 = \frac{R2}{10} \text{ and}$$

$$V_{CEO} \text{ of } Q2 \geq V_O$$

OPERATION AND APPLICATIONS

This section describes the operation and design of the MC1466 voltage and current regulator and also provides information on useful applications.

SUBJECT SEQUENCE

Theory of Operation
Applications
Transient Failures
Voltage/Current Mode Indicator

THEORY OF OPERATION

The schematic of Figure 5 can be simplified by breaking it down into basic functions, beginning with a simplified version of the voltage reference, Figure 7. Zener diodes CR1 and CR5 with their associated forward biased diodes CR2 through CR4 and CR6 through CR8 form the stable reference needed to balance the differential amplifier. At balance ($V_{B1} = V_{B2}$), the output voltage, ($V_{12} - V_7$), is at a value that is twice the drop across either of the two diode strings: $V_{12} - V_7 = 2 (V_{CR1} + V_{CR2} + V_{CR3} + V_{CR4})$. Other voltages, temperature compensated or otherwise, are also derived from these diodes strings for use in other parts of the circuit.

The voltage controlled current source (Figure 8) is a PNP-NPN composite which, due to the high NPN beta, yields a good working PNP from a lateral device working at a collector current of only a few microamperes. Its base voltage (V_{B_2}) is derived from a temperature compensated portion of the diode string and consequently the overall current is dependent on the value of emitter resistor R1. Temperature compensation of the base emitter junction of Q3 is not important because approximately 9 volts exists between V_{B_2} and V_{12}, making the ΔV_{BE}'s very small in percentage. Circuit reference voltage is derived from the product of I_R and R_R; if I_R is set at 1 mA (R1 = 8.5 kΩ), then R_R (in kΩ) = V_o. Other values of current may be used as long as the following restraints are kept in mind: 1) package dissipation will be increased by about 11 mW/mA and 2) bias current for the voltage control amplifier is 3 μA, temperature dependent, and is extracted from the reference current. The reference current should

FIGURE 7 – REFERENCE VOLTAGE REGULATOR

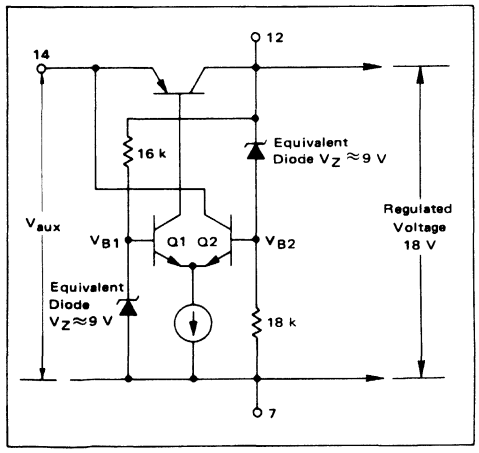
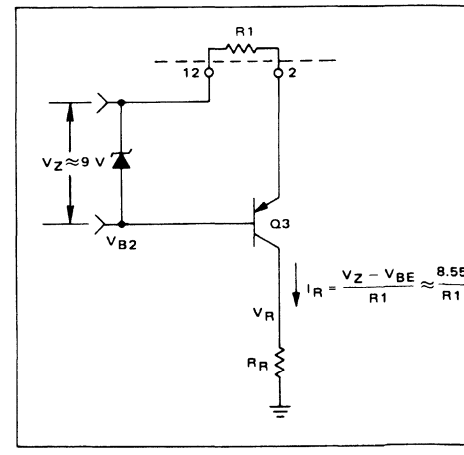


FIGURE 8 – VOLTAGE CONTROLLED CURRENT SOURCE



be at least two orders of magnitude above the largest expected bias current.

Loop amplification in the constant voltage mode is supplied by the voltage controlled amplifier (Figure 9), a standard high gain differential amplifier. The inputs are diode-protected against differential overvoltages and an emitter degenerating resistor, R_{OS}, has been added to one of the transistors. For an emitter current in both Q5 and Q6 of 1/2 milliampere there will exist a preset offset voltage in this differential amplifier of 15 mV to insure that the output voltage will be zero when the reference voltage is zero. Without R_{OS}, the output voltage could be a few millivolts above zero due to the inherent offset. Since the load resistor is so large in this stage compared with the load (Q9) it will be more instructive to look at the gain on a transconductance basis rather than voltage gain. Transconductance of the differential stage is defined for small signals as:

$$g_m = \frac{1}{2r_e + R_E} \qquad (1)$$

where

$$r_e \approx \frac{0.026}{I_E} \text{ and}$$

R_E = added emitter degenerating resistance.

For I_E = 0.5 mA,

$$g_m = \frac{1}{104 + 30} = \frac{1}{134} = 7.5 \text{ mA/volt.} \qquad (2)$$

FIGURE 9 – VOLTAGE CONTROL AMPLIFIER

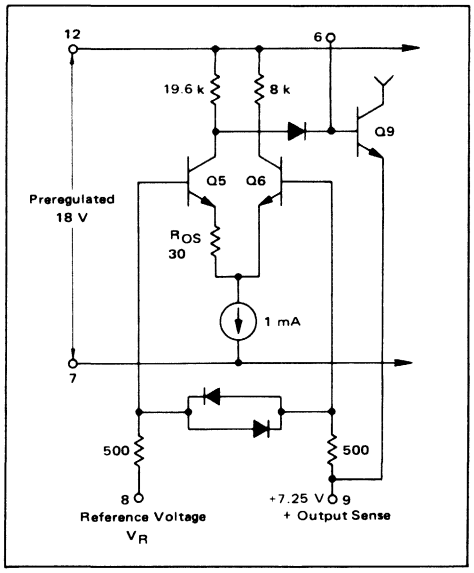
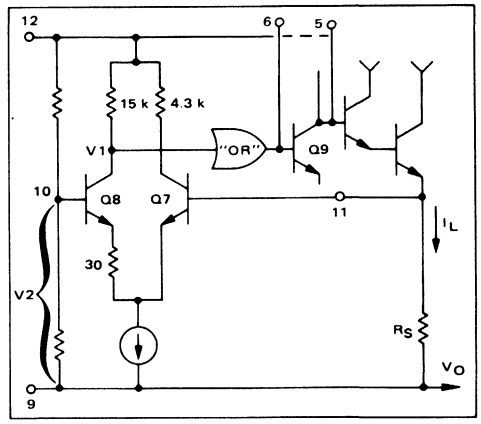


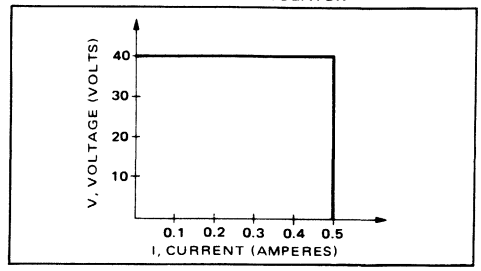
FIGURE 10 – CURRENT CONTROL CIRCUIT



This level is further boosted by the output stage such that in the constant voltage mode overall transconductance is about 300 mA/volt.

A second differential stage nearly identical to the first stage, serves as the current control amplifier (Figure 10). The gain of this stage insures a rapid crossover from the constant voltage to constant current modes and provides a convenient point to control the maximum deliverable load current. In use, a reference voltage derived from the preregulator and a voltage divider is applied to pin 10 while the output current is sampled across R_S by pin 11. When I_L R_S is 15 mV below the reference value, voltage V_1 begins to rapidly rise, eventually gaining complete control of Q9 and limiting output current to a value of V_2/R_S. If V_2 is derived from a variable source, short circuit current may be controlled over the complete output current capability of the regulator. Since the constant-voltage to constant-current change-over requires only a few millivolts the voltage regulation maintains its quality to the current limit and accordingly shows a very sharp "knee" (1% +1 mA, Figure 11). Note that the regulator can switch back into the constant voltage mode if the output voltage reaches a value greater than V_R. Operation through zero milliamperes is guaranteed by the inclusion of another emitter offsetting resistor.

FIGURE 11 – V_I CURVE FOR 0-TO-40 V, 0.5-AMPERE REGULATOR



Transistor Q9 and five diodes comprise the essential parts of the output stage (Figure 12). The diodes perform an "OR" function which allows only one mode of operation at a time - constant current or constant voltage. However, an additional stage (Q9) must be included to invert the logic and make it compatible with the driving requirements of series pass transistors as well as provide additional gain. A 1.5 mA collector current source sets the maximum deliverable output current and boosts the output impedance to that of the current source.

Note that the negative (substrate) side of the MC1466 is 7.25 volts lower than the output voltage, and the reference regulator guarantees that the positive side is 11 volts above the output. Thus the IC remains at a voltage (relative to ground) solely dependent on the output, "floating" above and below V_O. V_{CE} across Q9 is only two or three V_{BE}'s depending on the number of transistors used in the series pass configuration.

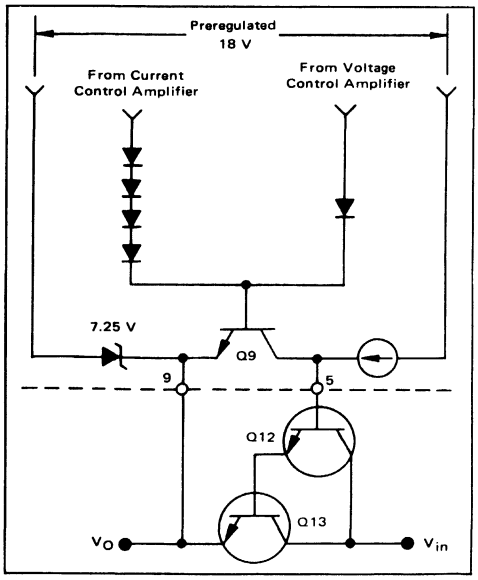
Performance characteristics of the regulator may be approximately calculated for a given circuit (Figure 2). Assuming that the two added transistors (Q12 and Q13) have minimum betas of 20, then the overall regulator transconductance will be:

$$g_{mT} = (400)\,300 \text{ mA/volt} = 120 \text{ A/volt.} \quad (3)$$

For a change in current of 500 mA the output voltage will drop only:

$$\Delta V = \frac{0.5}{120} = 4.2 \text{ mV.} \quad (4)$$

FIGURE 12 — MC1466 OUTPUT STAGE



The analysis thus far does not consider changes in V_R due to output current changes. If I_L increases by 500 mA the collector current of Q9 decreases by 1.25 mA, causing the collector current of Q5 to increase by 30 μA. Accordingly, I_R will be decreased by ≈0.30 μA which will drop the output by 0.03%. This figure may be improved considerably by either using high beta devices as the pass transistors, or by increasing I_R. Note again, however, that the maximum power rating of the package must be kept in mind. For example if I_R = 4 mA, power dissipation is

$$P_D = 20 \text{ V } (8 \text{ mA}) + (11 \text{ V x } 3 \text{ mA}) = 193 \text{ mW.} \quad (5)$$

This indicates that the circuit may be safely operated up to 118°C using 20 volts at the auxiliary supply voltage. If, however, the auxiliary supply voltage is 35 volts,

$$P_D = 35 \text{ V } (8 \text{ mA}) + 26 \text{ V } (3 \text{ mA}) = 358 \text{ mW.} \quad (6)$$

which dictates that the maximum operating temperature must be less than 91°C to keep package dissipation within specified limits.

Line voltage regulation is also a function of the voltage change between pins 8 and 9, and the change of V_{ref}. In this case, however, these voltages change due to changes in the internal regulator's voltages, which in turn are caused by changes in V_{aux}. Note that line voltage regulation is not a function of V_{in}. Note also that the instantaneous value of V_{aux} must always be between 20 and 35 volts.

Figure 6 shows six external diodes (CR_1 to CR_6) added for protective purposes. CR_1 should be used if the output voltage is less than 20 volts and CR_2, CR_3 are absent. For V_O higher than 20 volts, CR_1 should be discarded in favor of CR_2 and CR_3. Diode CR_4 prevents IC failure if the series pass transistors develop collector-base shorts while the main power transistor suffers a simultaneous open emitter. If the possibility of such a transistor failure mode seems remote, CR_4 may be deleted. To prevent instantaneous differential and common mode breakdown of the current sense amplifier, CR_5 must be placed across the current limit resistor R_S.

Load transients occasionally produce a damaging reversal of current flow from output to input $V_O > 150$ volts (which will destroy the IC). Diode CR_6 prevents such reversal and renders the circuit immune from destruction for such conditions, e.g., adding a large output capacitor after the supply is turned "on". Diodes CR_1, CR_2, CR_3, and CR_5 may be general purpose silicon units such as 1N4001 or equivalent whereas CR_4 and CR_6 should have a peak inverse voltage rating equal to V_{in} or greater.

APPLICATIONS

Figure 2 shows a typical 0-to-40 volts, 0.5-ampere regulator with better than 0.01% performance. The RC network between pins 5 and 6 and the capacitor between pins 13 and 14 provide frequency compensation for the MC1466. The external pass transistors are used to boost load current, since the output current of the regulator is less than 2 mA.

Figure 1 is a 0-to-15 volts, 10-ampere regulator with the pass transistor configuration necessary to boost the load current to 10 amperes. Note that C_O has been increased to 1000 μF following the general rule:

$$C_O = 100\ \mu F/A\ I_L.$$

The prime advantage of the MC1466 is its use as a high voltage regulator, as shown in Figure 3. This 0-to-250 volts 0.1-ampere regulator is typical of high voltage applications, limited only by the breakdown and safe areas of the output pass transistors.

The primary limiting factor in high voltage series regulators is the pass transistor. Figure 13 shows a safe area curve for the MJ413. Looking at Figure 3, we see that if the output is shorted, the transistor will have a collector current of 100 mA, with a V_{CE} approximately equal to 260 volts. Thus this point falls on the dc line of the safe area curve, insuring that the transistor will not enter secondary breakdown.

In this respect (Safe Operating Area) the foldback circuit of Figure 14 is superior for handling high voltages and yet is short-circuit protected. This is due to the fact that load current is diminished as output voltage drops (V_{CE} increases as V_O drops) as seen in Figure 15. By careful design the load current at a short, I_{SC} can be made low enough such that the combined V_{CE} (V_{in}) and I_{SC} still falls within the dc safe operating area of the transistor. For the illustrated design (Figure 14), an input voltage of 210 volts is compatible with a short circuit current of 100 mA. Yet current foldback allows us to design for a maximum regulated load current of 500 mA. the pertinent design equations are:

Let $R_2\ (k\Omega) = V_O$

$$\alpha = \frac{0.25}{V_O}\left[\frac{I_k}{I_{SC}} - 1\right]$$

$$R_1\ (k\Omega) = \frac{\alpha}{1-\alpha}\ V_O$$

$$R_{SC} = \frac{0.25}{(1-\alpha)\ I_{SC}}.$$

FIGURE 13 – SAFE AREA CURVE FOR THE MJ413

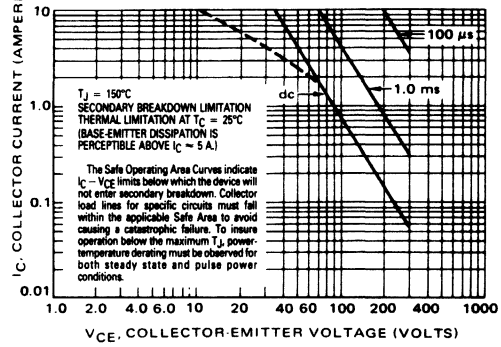
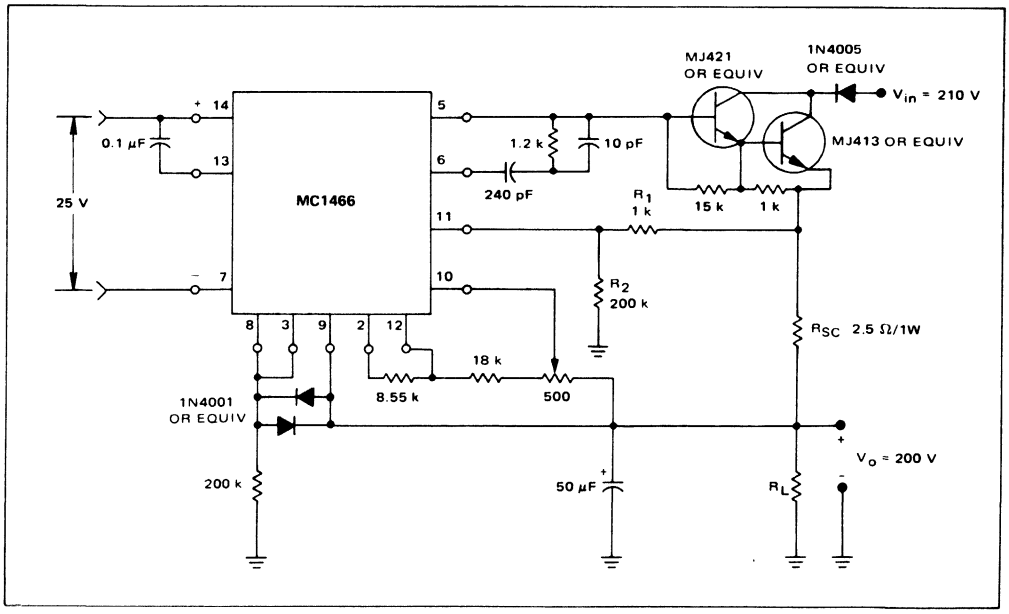


FIGURE 14 – A 200 V, 0.5-AMPERE REGULATOR WITH CURRENT FOLDBACK



The terms I_{SC} and I_k correspond to the short-circuit current and maximum available load current as shown in Figure 15.

FIGURE 15 – TYPICAL FOLDBACK PERFORMANCE

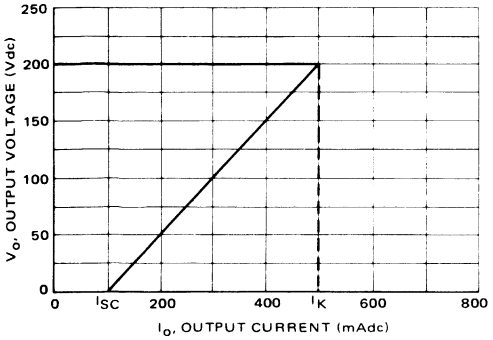


Figure 16 shows a remote sense application which should be used when high current or long wire lengths are used. This type of wiring is recommended for any application where the best possible regulation is desired. Since the sense lines draw only a small current, large voltage drops do not destroy the excellent regulation of the MC1466.

TRANSIENT FAILURES

In industrial areas where electrical machinery is used the normal ac line often contains bursts of voltage running from hundreds to thousands of volts in magnitude and only microseconds in duration. Under some conditions this energy is dissipated across the internal zener connected between pins 9 and 7. This transient condition may produce a total failure of the regulator device without any apparent explanation. This type of failure is identified by absence of the 7 volt zener (CR1) between pin 9 and pin 7. To prevent this failure mode the use of a shielded power transformer is recommended, as shown in Figure 6. In addition, it is recommended that C1, C3 and C4 be included to aid in transient repression. These capacitors should have good high frequency characteristics.

If the possibility of transients on the output exists, the addition of a resistor and zener diode between pins 9 and 7 as shown on Figure 17 should be added.

VOLTAGE/CURRENT MODE INDICATOR

There may be times when it is desirable to know when the MC1466 is in the constant current mode or constant voltage mode. A mode indicator can be easily added to provide this feature. Figure 18 shows how a PNP transistor has replaced a protection diode between pins 8 and 9 of Figure 2. When the MC1466 goes from constant voltage mode to constant current mode, V_O will drop below V_8 and the PNP transistor will turn on. The 1 mA current supplied by pin 8 will now be shunted to base of Q2 thereby turning on the indicator device I1.

FIGURE 16 – REMOTE SENSE

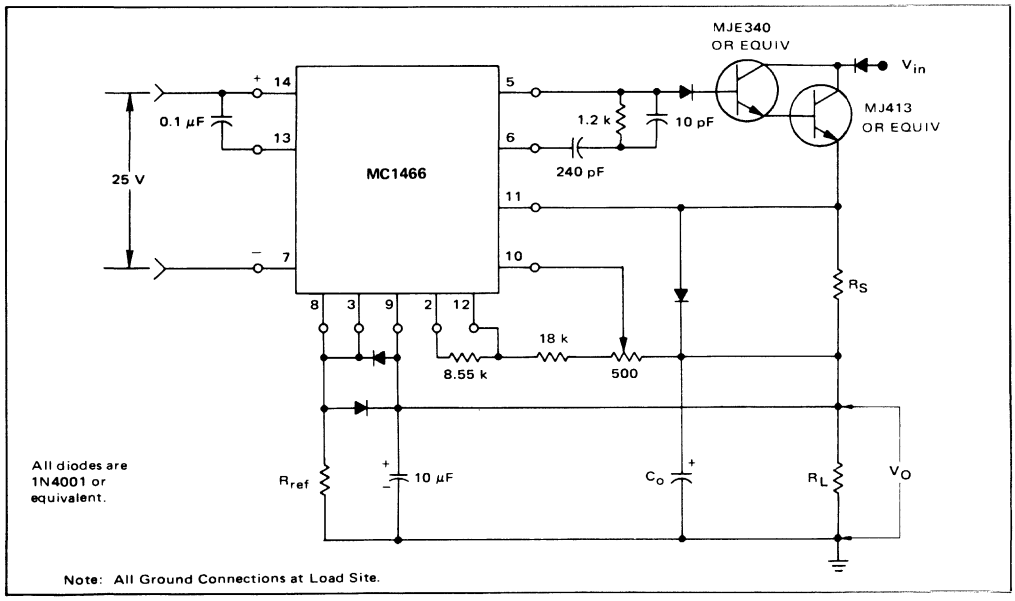


FIGURE 17 – A 0-TO-250 VOLT, 0.1-AMPERE REGULATOR

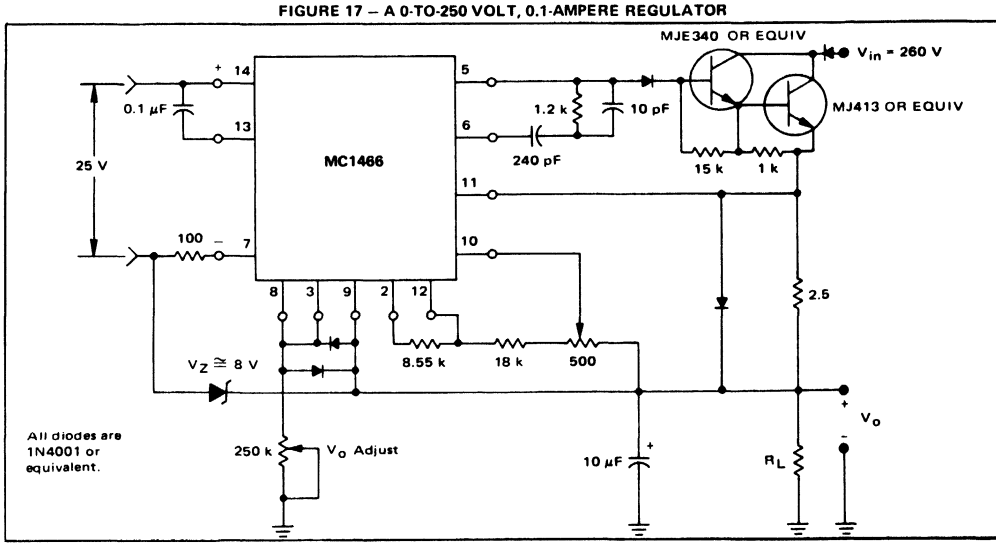
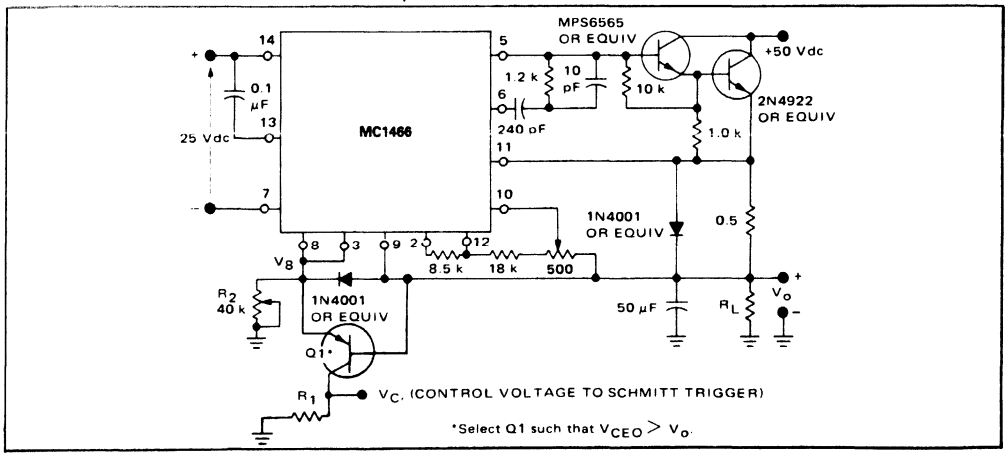


FIGURE 18 – 0-TO-40 Vdc, 0.5-AMPERE REGULATOR WITH MODE INDICATOR



MOTOROLA

MC1468
MC1568

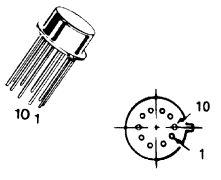
DUAL ±15-VOLT REGULATOR

The MC1568/MC1468 is a dual polarity tracking regulator designed to provide balanced positive and negative output voltages at currents to 100 mA. Internally, the device is set for ±15-volt outputs but an external adjustment can be used to change both outputs simultaneously from 8.0 to 20 volts. Input voltages up to ±30 volts can be used and there is provision for adjustable current limiting.

- Internally Set to ±15 V Tracking Outputs
- Output Currents to 100 mA
- Outputs Balanced to within 1.0% (MC1568)
- Line and Load Regulation of 0.06%
- 1.0% Maximum Output Variation Due to Temperature Changes
- Standby Current Drain of 3.0 mA
- Externally Adjustable Current Limit
- Remote Sensing Provisions

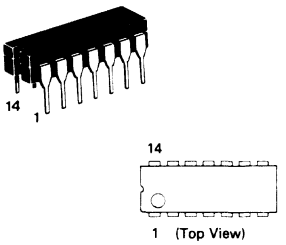
DUAL ±15-VOLT TRACKING REGULATOR

SILICON MONOLITHIC INTEGRATED CIRCUIT



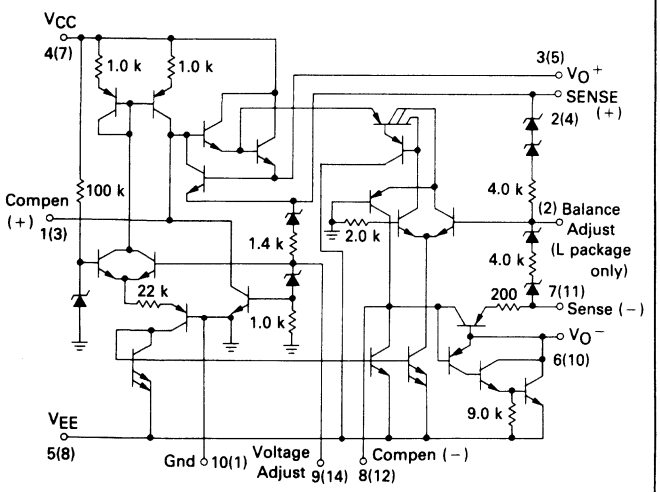
(Bottom View)

G SUFFIX
METAL PACKAGE
CASE 603C-01



L SUFFIX
CERAMIC PACKAGE
CASE 632-08

CIRCUIT SCHEMATIC



Pin numbers adjacent to terminals are for the G suffix package and pin numbers in parentheses are for the L suffix package.

ORDERING INFORMATION

Device	Temperature Range	Package
MC1468G	0°C to +70°C	Metal Can
MC1468L	0°C to +70°C	Ceramic DIP
MC1568G	−55°C to +125°C	Metal Can
MC1568L	−55°C to +125°C	Ceramic DIP

MAXIMUM RATINGS (T_C = +25°C unless otherwise noted.)

Rating	Symbol	Value		Unit
Input Voltage	V_{CC},$\|V_{EE}\|$	30		Vdc
Peak Load Current	I_{pk}	100		mA
Power Dissipation and Thermal Characteristics		**G Package**	**L Package**	
T_A = +25°C	P_D	0.83	1.25	Watts
Derate above T_A = +25°C	$1/\theta_{JA}$	6.6	10	mW/°C
Thermal Resistance, Junction to Air	θ_{JA}	150	100	°C/W
T_C = +25°C	P_D	1.8	2.5	Watts
Derate above T_C = +25°C	$1/\theta_{JC}$	14.3	20	mW/°C
Thermal Resistance, Junction to Case	θ_{JC}	70	50	°C/W
Storage Junction to Temperature Range	T_J, T_{stg}	−65 to +150		°C
Minimum Short-Circuit Resistance	R_{SC}(min)	4.0		Ohms

OPERATING TEMPERATURE RANGE

Ambient Temperature	T_A		°C
MC1468		0 to +70	
MC1568		−55 to +125	

ELECTRICAL CHARACTERISTICS (V_{CC} = +20 V, V_{EE} = −20 V, C1 = C2 = 1500 pF, C3 = C4 = 1.0 μF, $R_{SC}^+ = R_{SC}^-$ = 4.0 Ω, $I_L^+ = I_L^-$ = 0, T_C = +25°C unless otherwise noted.) (See Figure 1.)

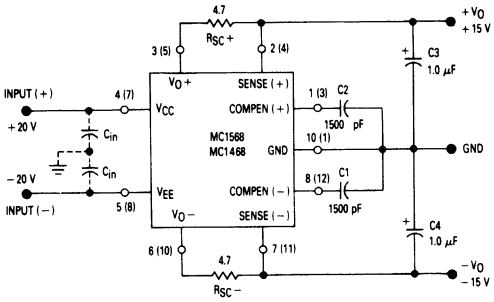
Characteristic	Symbol	MC1568			MC1468			Unit
		Min	Typ	Max	Min	Typ	Max	
Output Voltage	V_O	±14.5	±15	±15.5	±14.5	±15	±15.5	Vdc
Input Voltage	V_{in}	—	—	±30	—	—	±30	Vdc
Input-Output Voltage Differential	$\|V_{in}-V_O\|$	2.0	—	—	2.0	—	—	Vdc
Output Voltage Balance (L package only)	V_{Bal}	—	±50	±150	—	±50	±300	mV
Line Regulation Voltage	Reg_{line}							mV
(V_{in} = 18 V to 30 V)		—	—	10	—	—	10	
(T_{low}① to T_{high}②)		—	—	20	—	—	20	
Load Regulation Voltage	Reg_{load}							mV
(I_L = 0 to 50 mA, T_J = constant)		—	—	10	—	—	10	
(T_A = T_{low} to T_{high})		—	—	30	—	—	30	
Output Voltage Range	V_{OR}							Vdc
L Package (See Figure 4)		±8.0	—	±20	±8.0	—	±20	
G Package (See Figures 2 and 13)		±14.5	—	±20	±14.5	—	±20	
Ripple Rejection (f = 120 Hz)	RR	—	75	—	—	75	—	dB
Output Voltage Temperature Stability (T_{low} to T_{high})	$\|TS_{VO}\|$	—	0.3	1.0	—	0.3	1.0	%
Short-Circuit Current Limit (R_{SC} = 10 ohms)	I_{SC}	—	60	—	—	60	—	mA
Output Noise Voltage (BW = 100 Hz–10 kHz)	V_n	—	100	—	—	100	—	μV(RMS)
Positive Standby Current (V_{in} = +30 V)	I_B^+	—	2.4	4.0	—	2.4	4.0	mA
Negative Standby Current (V_{in} = −30 V)	I_B^-	—	1.0	3.0	—	1.0	3.0	mA
Long-Term Stability	$\Delta V_O/\Delta t$	—	0.2	—	—	0.2	—	%/k Hr

① T_{low} = 0°C for MC1468
= −55°C for MC1568

② T_{high} = +70°C for MC1468
= +125°C for MC1568

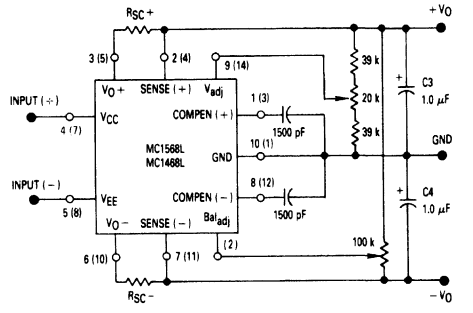
TYPICAL APPLICATIONS

FIGURE 1 — BASIC 50-mA REGULATOR



C1 and C2 should be located as close to the device as possible. A 0.1 μF ceramic capacitor (C_{in}) may be required on the input lines if the device is located an appreciable distance from the rectifier filter capacitors. C3 and C4 may be increased to improve load transient response and to reduce the output noise voltage. At low temperature operation, it may be necessary to bypass C4 with a 0.1 μF ceramic disc capacitor.

FIGURE 2 — VOLTAGE ADJUST AND BALANCE ADJUST CIRCUIT
(14.5 V ≤ V_{out} ≤ 20 V)



Balance adjust available in MC1568L, MC1468L ceramic dual in-line package only.

FIGURE 3 — ± 1.5-AMPERE REGULATOR
(Short-Circuit Protected, with Proper Heatsinking)

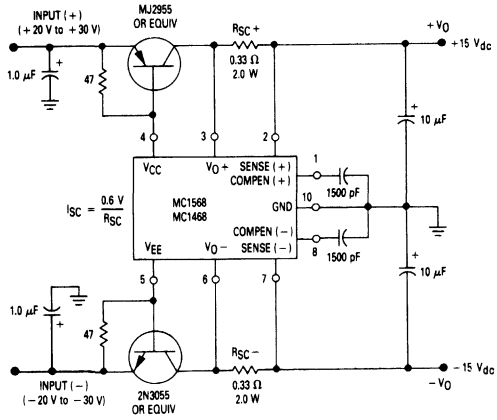
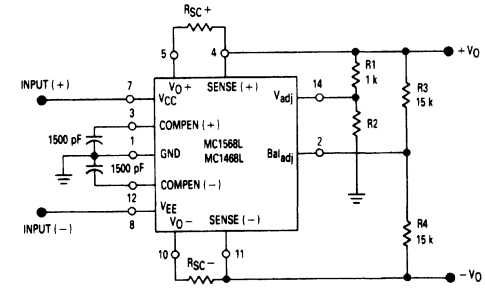


FIGURE 4 — OUTPUT VOLTAGE ADJUSTMENT FOR 8.0 V ≤ |±VO| ≤ 14.5 V
(Ceramic-Packaged Devices Only)



The presence of Bal_{adj}, pin 2, on devices housed in the dual in-line package (L suffix) allows the user to adjust the output voltages down to ±8.0 V. The required value of resistor R2 can be calculated from

$$R2 = \frac{R1\,R_{int}\,(\phi + V_z)}{R_{int}\,(V_O - \phi - V_z) - \phi\,R1}$$

Where: R_{int} = An Internal Resistor = R1 = 1.0 kΩ
ϕ = 0.68 V
V_z = 6.6 V

Some common design values are listed below:

±VO(V)	R2	TC VO (%/°C)	IB + (mA)
14	1.2 k	0.003	10
12	1.8 k	0.022	7.2
10	3.5 k	0.025	5.0
8.0	∞	0.028	2.6

TYPICAL CHARACTERISTICS

(V_{CC} = +20 V, V_{EE} = −20 V, V_O = ±15 V, T_A = +25°C unless otherwise noted.)

FIGURE 5 — LOAD REGULATION

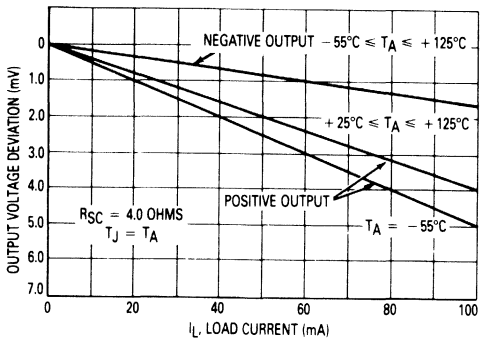


FIGURE 6 — REGULATOR DROPOUT VOLTAGE

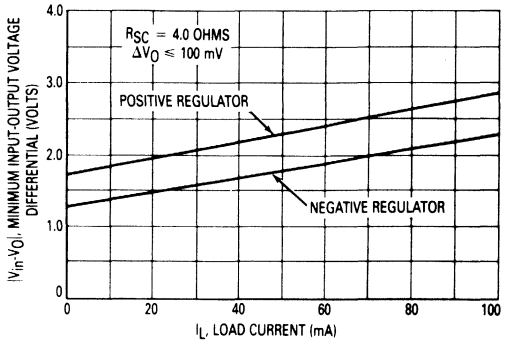


FIGURE 7 — MAXIMUM CURRENT CAPABILITY

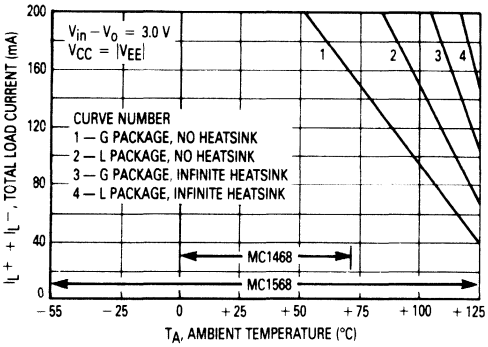


FIGURE 8 — MAXIMUM CURRENT CAPABILITY

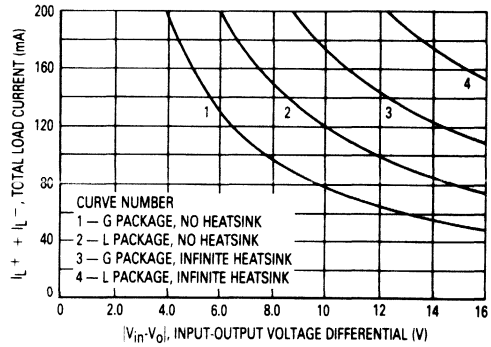


FIGURE 9 — I_{SC} versus R_{SC}

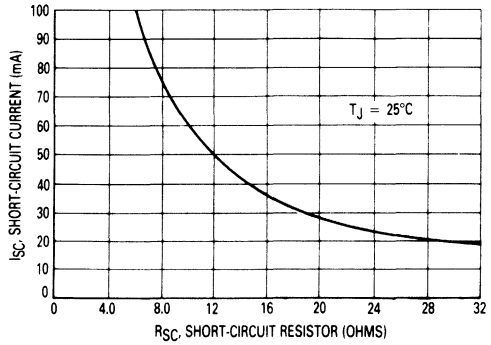
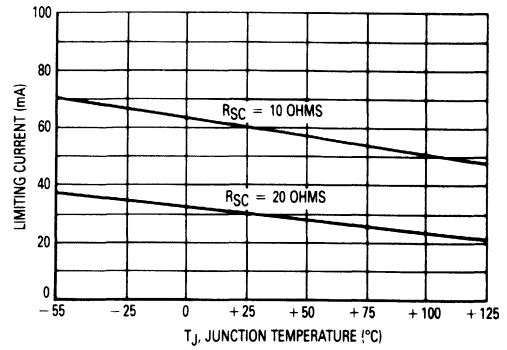


FIGURE 10 — CURRENT-LIMITING CHARACTERISTICS



TYPICAL CHARACTERISTICS (continued)

(V_{CC} = +20 V, V_{EE} = −20 V, V_O = ±15 V, T_A = +25°C unless otherwise noted.)

FIGURE 11 — STANDBY CURRENT DRAIN

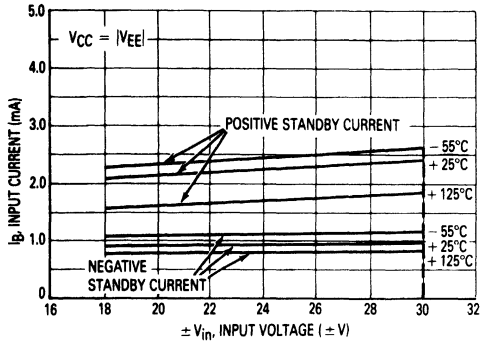


FIGURE 12 — STANDBY CURRENT DRAIN

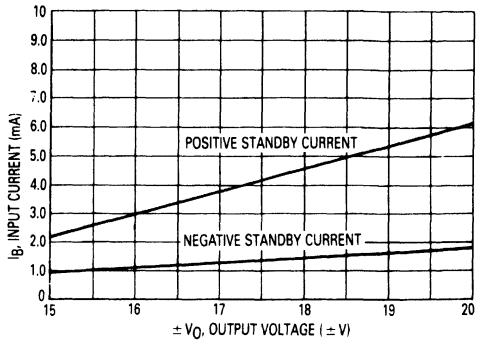


FIGURE 13 — TEMPERATURE COEFFICIENT OF OUTPUT VOLTAGE

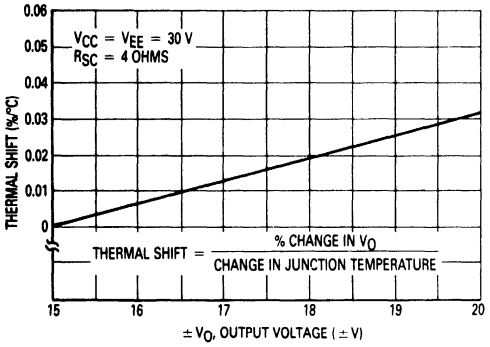


FIGURE 14 — LOAD TRANSIENT RESPONSE

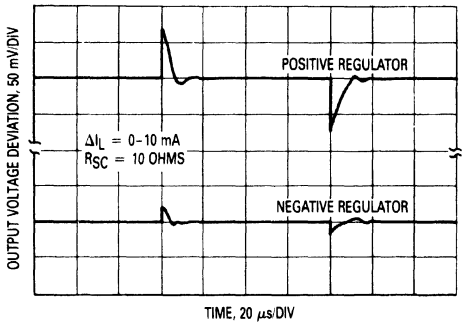


FIGURE 15 — LINE TRANSIENT RESPONSE

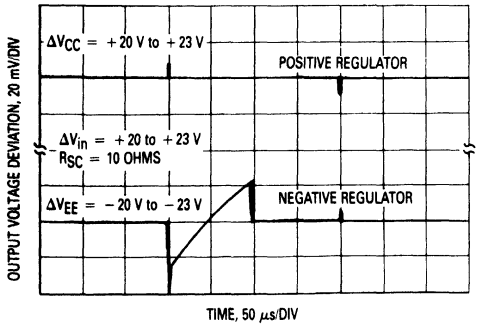
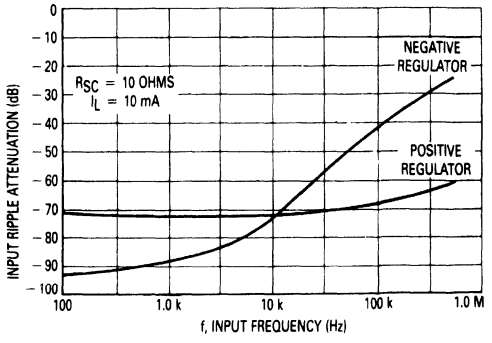
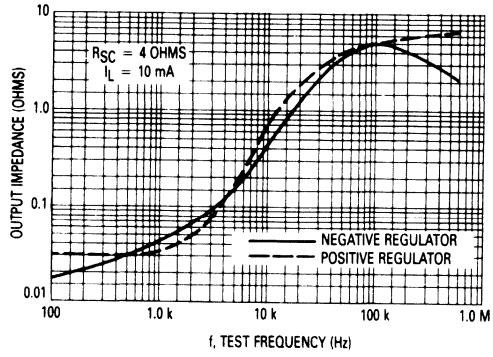


FIGURE 16 — RIPPLE REJECTION



TYPICAL CHARACTERISTICS (continued)
(V_{CC} = +20 V, V_{EE} = −20 V, V_O = ±15 V, T_A = +25°C unless otherwise noted.)

FIGURE 17 — OUTPUT IMPEDANCE



ORDERING INFORMATION

Device	Alternate	Temperature Range	Package
MC1723CD		0°C to +70°C	SO-14
MC1723CG	LM723CH, μA723HC	0°C to +70°C	Metal Can
MC1723CL	LM723CJ, μA723DC	0°C to +70°C	Ceramic DIP
MC1723CP	LM723CN, μA723PC	0°C to +70°C	Plastic DIP
MC1723G		−55°C to +125°C	Metal Can
MC1723L		−55°C to +125°C	Ceramic DIP

MC1723
MC1723C

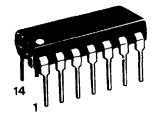
VOLTAGE REGULATOR

SILICON MONOLITHIC INTEGRATED CIRCUIT

VOLTAGE REGULATOR

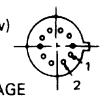
The MC1723 is a positive or negative voltage regulator designed to deliver load current to 150 mAdc. Output current capability can be increased to several amperes through use of one or more external pass transistors. MC1723 is specified for operation over the military temperature range (-55°C to +125°C) and the MC1723C over the commercial temperature range (0 to +70°C)

- Output Voltage Adjustable from 2 Vdc to 37 Vdc
- Output Current to 150 mAdc Without External Pass Transistors
- 0.01% Line and 0.03% Load Regulation
- Adjustable Short-Circuit Protection

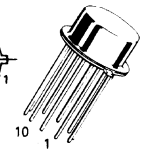


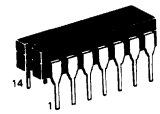
P SUFFIX
PLASTIC PACKAGE
CASE 646-06

(Bottom View)



G SUFFIX
METAL PACKAGE
CASE 603-04

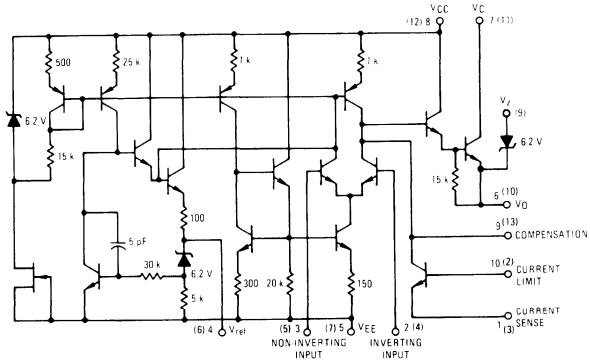




L SUFFIX
CERAMIC PACKAGE
CASE 632-08

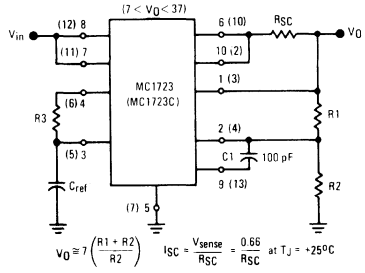
D SUFFIX
PLASTIC PACKAGE
CASE 751A-02
SO-14

FIGURE 1 – CIRCUIT SCHEMATIC



PIN NUMBERS ADJACENT TO TERMINALS ARE FOR THE METAL PACKAGE.
PIN NUMBERS IN PARENTHESIS ARE FOR DUAL IN LINE PACKAGES

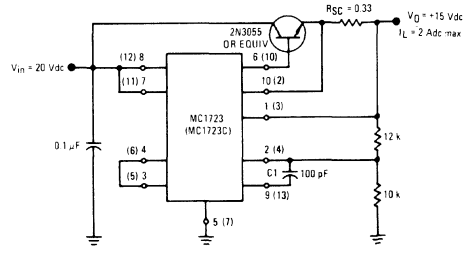
FIGURE 2 – TYPICAL CIRCUIT CONNECTION



$V_O \cong 7\left(\frac{R1 + R2}{R2}\right)$ $I_{SC} = \frac{V_{sense}}{R_{SC}} = \frac{0.66}{R_{SC}}$ at $T_J = +25°C$

For best results 10 k < R2 < 100 k
For minimum drift R3 = R1 ,R2

FIGURE 3 – TYPICAL NPN CURRENT BOOST CONNECTION



MAXIMUM RATINGS (T_A = +25°C unless otherwise noted.)

Rating	Symbol	Value	Unit
Pulse Voltage from V_{CC} to V_{EE} (50 ms)	$V_{in(p)}$	50	V_{peak}
Continuous Voltage from V_{CC} to V_{EE}	V_{in}	40	Vdc
Input-Output Voltage Differential	$V_{in} - V_O$	40	Vdc
Maximum Output Current	I_L	150	mAdc
Current from V_{ref}	I_{ref}	15	mAdc
Current from V_z	I_z	25	mA
Voltage Between Non-Inverting Input and V_{EE}	V_{ie}	8.0	Vdc
Differential Input Voltage	V_{id}	±5.0	Vdc
Power Dissipation and Thermal Characteristics			
Plastic Package			
T_A = +25°C	P_D	1.25	W
Derate above T_A = +25°C	$1/\theta_{JA}$	10	mW/°C
Thermal Resistance, Junction to Air	θ_{JA}	100	°C/W
Metal Package			
T_A = +25°C	P_D	1.0	Watt
Derate above T_A = +25°C	$1/\theta_{JA}$	6.6	mW/°C
Thermal Resistance, Junction to Air	θ_{JA}	150	°C/W
T_C = +25°C	P_D	2.1	Watts
Derate above T_A = +25°C	$1/\theta_{JA}$	14	mW/°C
Thermal Resistance, Junction to Case	θ_{JC}	35	°C/W
Dual In-Line Ceramic Package	P_D	1.5	Watt
Derate above T_A = +25°C	$1/\theta_{JA}$	10	mW/°C
Thermal Resistance, Junction to Air	θ_{JA}	100	°C/W
Operating and Storage Junction Temperature Range	T_J, T_{stg}		°C
Metal Package		-65 to +150	
Dual In-Line Ceramic		-65 to +175	
Operating Ambient Temperature Range	T_A		°C
MC1723C		0 to +70	
MC1723		-55 to +125	

ELECTRICAL CHARACTERISTICS (Unless otherwise noted: T_A = +25°C, V_{in} 12 Vdc, V_O = 5.0 Vdc, I_L = 1.0 mAdc, R_{SC} = 0, C1 = 100 pF, C_{ref} = 0 and divider impedance as seen by the error amplifier ≤ 10 kΩ connected as shown in Figure 2)

Characteristic	Symbol	MC1723			MC1723C			Unit
		Min	Typ	Max	Min	Typ	Max	
Input Voltage Range	V_{in}	9.5	–	40	9.5	–	40	Vdc
Output Voltage Range	V_O	2.0	–	37	2.0	–	37	Vdc
Input-Output Voltage Differential	$V_{in}-V_O$	3.0	–	38	3.0	–	38	Vdc
Reference Voltage	V_{ref}	6.95	7.15	7.35	6.80	7.15	7.50	Vdc
Standby Current Drain (I_L = 0, V_{in} = 30 V)	I_{IB}	–	2.3	3.5	–	2.3	4.0	mAdc
Output Noise Voltage (f = 100 Hz to 10 kHz)	V_n							μV(RMS)
C_{ref} = 0		–	20	–	–	20	–	
C_{ref} = 5.0 μF		–	2.5	–	–	2.5	–	
Average Temperature Coefficient of Output Voltage (T_{low} ① < T_A < T_{high} ②)	TCV_O	–	0.002	0.015	–	0.003	0.015	%/°C
Line Regulation	Reg_{line}							%V_O
(T_A = +25°C) 12 V < V_{in} < 15 V		–	0.01	0.1	–	0.01	0.1	
(T_A = +25°C) 12 V ≤ V_{in} < 40 V		–	0.02	0.2	–	0.1	0.5	
(T_{low} ① < T_A < T_{high} ②) 12 V < V_{in} < 15 V		–	–	0.3	–	–	0.3	
Load Regulation (1.0 mA < I_L < 50 mA)	Reg_{load}							%V_O
T_A = +25°C		–	0.03	0.15	–	0.03	0.2	
T_{low} ① < T_A < T_{high} ②		–	–	0.6	–	–	0.6	
Ripple Rejection (f = 50 Hz to 10 kHz)	RR							dB
C_{ref} = 0		–	74	–	–	74	–	
C_{ref} = 5.0 μF		–	86	–	–	86	–	
Short Circuit Current Limit (R_{SC} = 10 Ω, V_O = 0)	I_{sc}	–	65	–	–	65	–	mAdc
Long Term Stability	$\Delta V_O/\Delta t$	–	0.1	–	–	0.1	–	%/1000 Hr

① T_{low} = 0°C for MC1723C
= -55°C for MC1723

② T_{high} = +70° C for MC1723C
= +125°C for MC1723

TYPICAL CHARACTERISTICS

(V_{in} = 12 Vdc, V_O = 5.0 Vdc, I_L = 1.0 mAdc, R_{SC} = 0, T_A = +25°C unless otherwise noted.)

FIGURE 4 – MAXIMUM LOAD CURRENT AS A FUNCTION OF INPUT-OUTPUT VOLTAGE DIFFERENTIAL

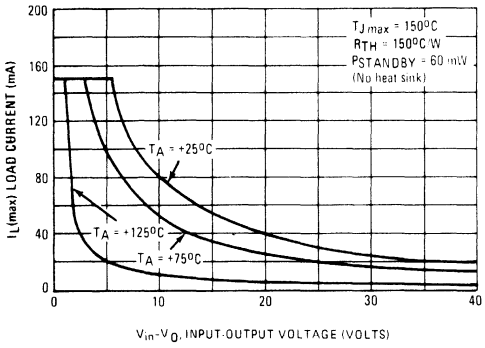


FIGURE 5 – LOAD REGULATION CHARACTERISTICS WITHOUT CURRENT LIMITING

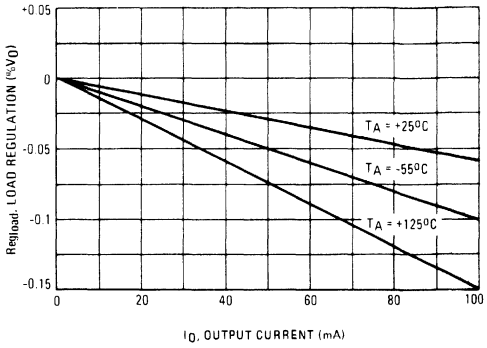


FIGURE 6 – LOAD REGULATION CHARACTERISTICS WITH CURRENT LIMITING

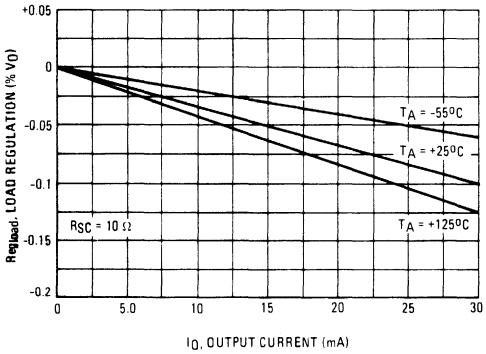


FIGURE 7 – LOAD REGULATION CHARACTERISTICS WITH CURRENT LIMITING

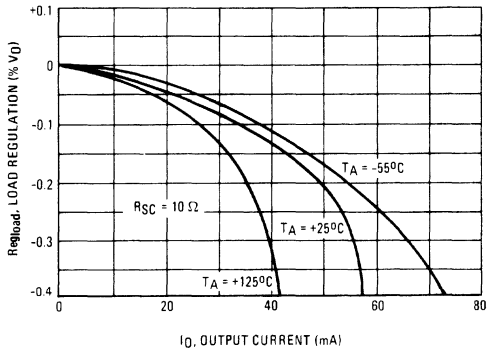


FIGURE 8 – CURRENT LIMITING CHARACTERISTICS

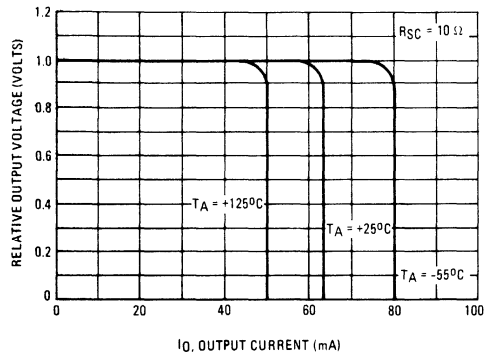
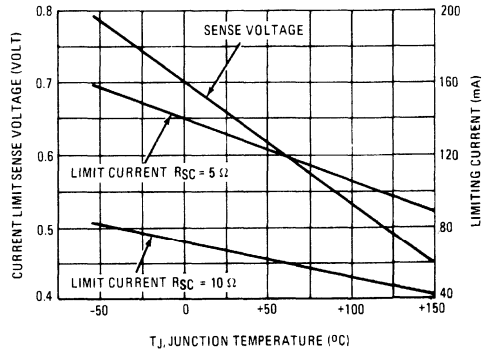


FIGURE 9 – CURRENT LIMITING CHARACTERISTICS AS A FUNCTION OF JUNCTION TEMPERATURE



TYPICAL CHARACTERISTICS (continued)

FIGURE 10 – LINE REGULATION AS A FUNCTION OF INPUT-OUTPUT VOLTAGE DIFFERENTIAL

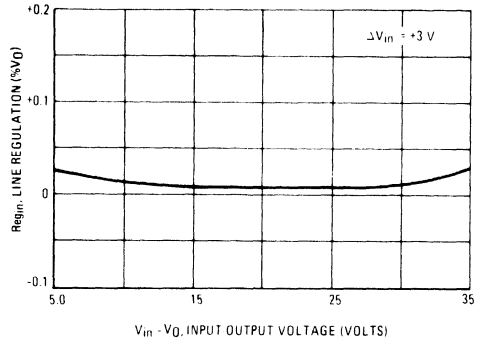


FIGURE 11 – LOAD REGULATION AS A FUNCTION OF INPUT-OUTPUT VOLTAGE DIFFERENTIAL

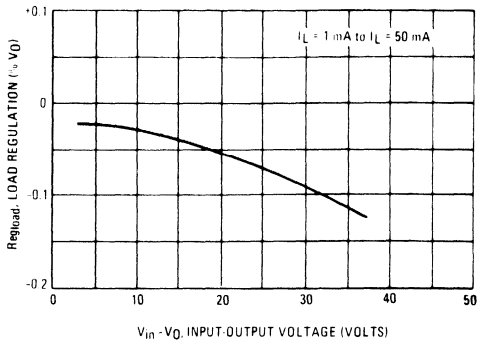


FIGURE 12 – STANDBY CURRENT DRAIN AS A FUNCTION OF INPUT VOLTAGE

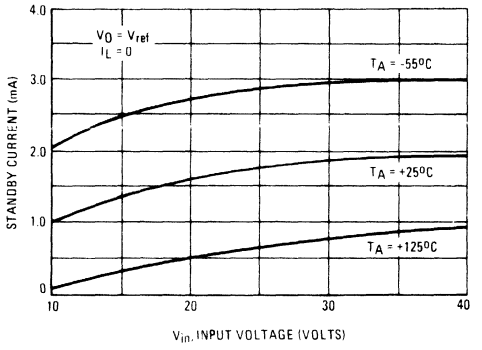


FIGURE 13 – LINE TRANSIENT RESPONSE

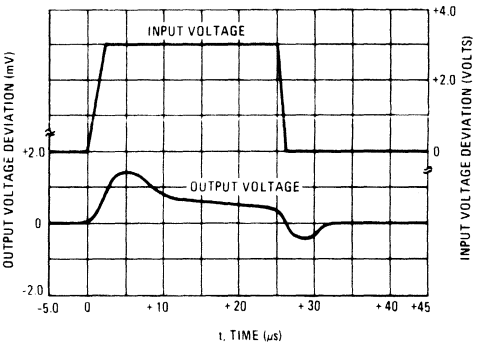


FIGURE 14 – LOAD TRANSIENT RESPONSE

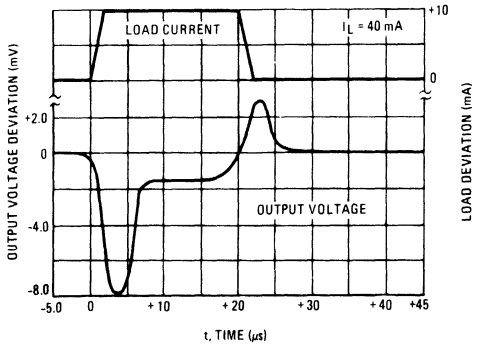
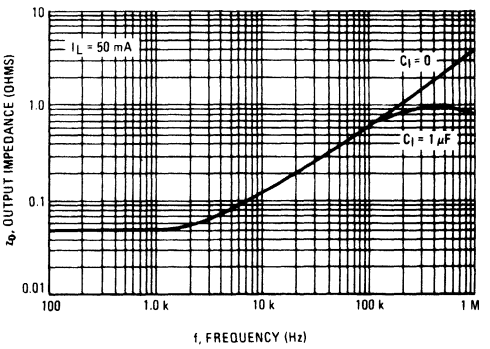


FIGURE 15 – OUTPUT IMPEDANCE AS FUNCTION OF FREQUENCY



TYPICAL APPLICATIONS

Pin numbers adjacent to terminals are for the metal package;
pin numbers in parenthesis are for the dual in-line packages.

FIGURE 16 – TYPICAL CONNECTION FOR $2 < V_O < 7$

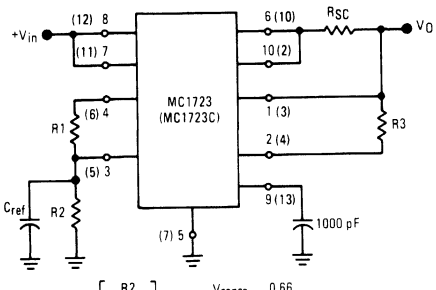


FIGURE 17 – MC1723,C FOLDBACK CONNECTION

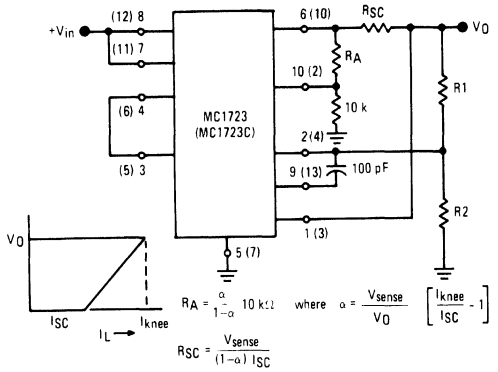


FIGURE 18 – +5 V, 1-AMPERE SWITCHING REGULATOR

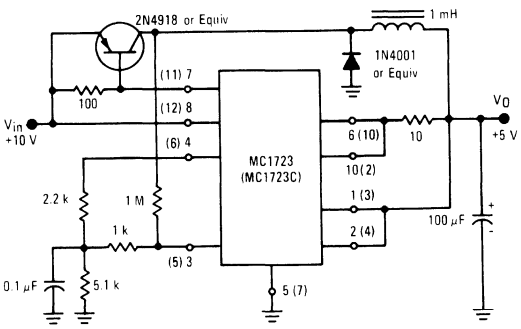


FIGURE 19 – +5 V, 1-AMPERE HIGH EFFICIENCY REGULATOR

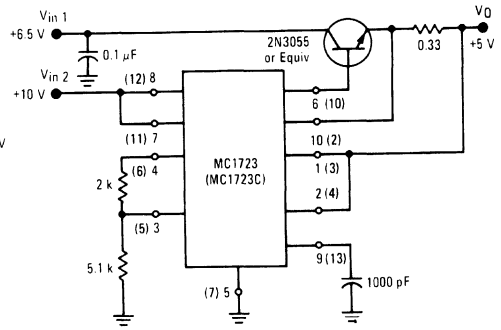


FIGURE 20 – +15 V, 1-AMPERE REGULATOR WITH REMOTE SENSE

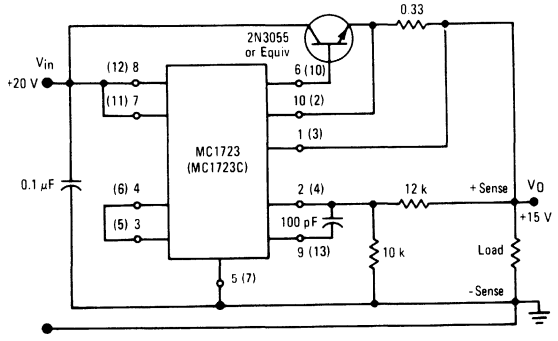
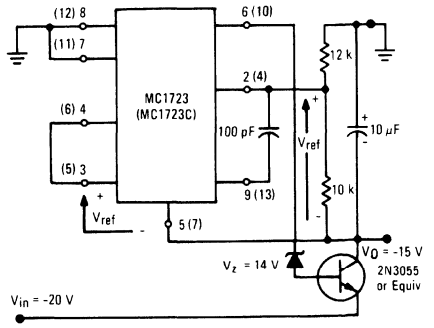
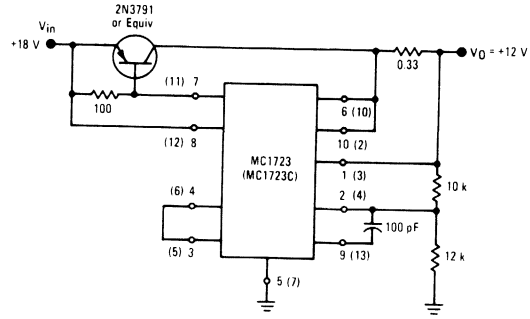


FIGURE 21 – -15 V NEGATIVE REGULATOR



TYPICAL APPLICATIONS (continued)

FIGURE 22 – +12 V, 1-AMPERE REGULATOR USING PNP CURRENT BOOST



MOTOROLA

MC3423
MC3523

Specifications and Applications Information

OVERVOLTAGE "CROWBAR" SENSING CIRCUIT

These overvoltage protection circuits (OVP) protect sensitive electronic circuitry from overvoltage transients or regulator failures when used in conjunction with an external "crowbar" SCR. They sense the overvoltage condition and quickly "crowbar" or short circuit the supply, forcing the supply into current limiting or opening the fuse or circuit breaker.

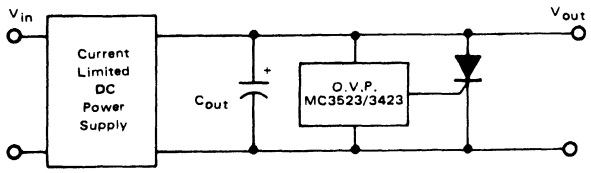
The protection voltage threshold is adjustable and the MC3423/3523 can be programmed for minimum duration of overvoltage condition before tripping, thus supplying noise immunity.

The MC3423/3523 is essentially a "two terminal" system, therefore it can be used with either positive or negative supplies.

MAXIMUM RATINGS

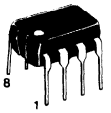
Rating	Symbol	Value	Unit
Differential Power Supply Voltage	V_{CC}-V_{EE}	40	Vdc
Sense Voltage (1)	$V_{Sense\ 1}$	6.5	Vdc
Sense Voltage (2)	$V_{Sense\ 2}$	6.5	Vdc
Remote Activation Input Voltage	V_{act}	7.0	Vdc
Output Current	I_O	300	mA
Operating Ambient Temperature Range MC3423 MC3523	T_A	 0 to +70 −55 to +125	°C
Operating Junction Temperature Plastic Package Ceramic Package	T_J	 125 150	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C

TYPICAL APPLICATION

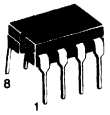


OVERVOLTAGE SENSING CIRCUIT

SILICON MONOLITHIC INTEGRATED CIRCUIT



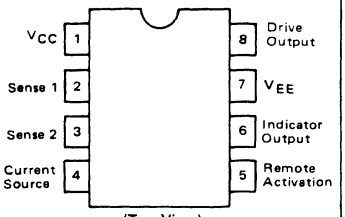
P1 SUFFIX
PLASTIC PACKAGE
CASE 626-05
(MC3423 only)



U SUFFIX
CERAMIC PACKAGE
CASE 693-02

D SUFFIX
PLASTIC PACKAGE
CASE 751-03
SOP-8

PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

Device	Temperature Range	Package
MC3423D	0 to +70°C	SO-8
MC3423P1		Plastic DIP
MC3423U		Ceramic DIP
MC3523U	−55 to +125°C	Ceramic DIP

ELECTRICAL CHARACTERISTICS ($5\ V \leq V_{CC}-V_{EE} \leq 36\ V$, $T_{low} < T_A < T_{high}$ unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Supply Voltage Range	V_{CC}-V_{EE}	4.5	–	40	Vdc
Output Voltage (I_O = 100 mA)	V_O	V_{CC}-2.2	V_{CC}-1.8	–	Vdc
Indicator Output Voltage ($I_{O(Ind)}$ = 1.6 mA)	V_{OL}(Ind)	–	0.1	0.4	Vdc
Sense Trip Voltage (T_A = 25°C)	$V_{Sense\ 1}$, $V_{Sense\ 2}$	2.45	2.6	2.75	Vdc
Temperature Coefficient of $V_{Sense\ 1}$ (Figure 2)	TCV_{S1}	–	0.06	–	%/°C
Remote Activation Input Current (V_{IH} = 2.0 V, V_{CC}-V_{EE} = 5.0 V) (V_{IL} = 0.8 V, V_{CC}-V_{EE} = 5.0 V)	I_{IH} I_{IL}	– –	5.0 -120	40 -180	μA
Source Current	I_{Source}	0.1	0.2	0.3	mA
Output Current Risetime (T_A = 25°C)	t_r	–	400	–	mA/μs
Propagation Delay Time (T_A = 25°C)	t_{pd}	–	0.5	–	μs
Supply Current MC3423 MC3523	I_D	– –	6.0 5.0	10 7.0	mA

T_{low} = -55°C for MC3523 = 0°C for MC3423

T_{high} = +125°C for MC3523 = +70°C for MC3423

FIGURE 1 – BLOCK DIAGRAM

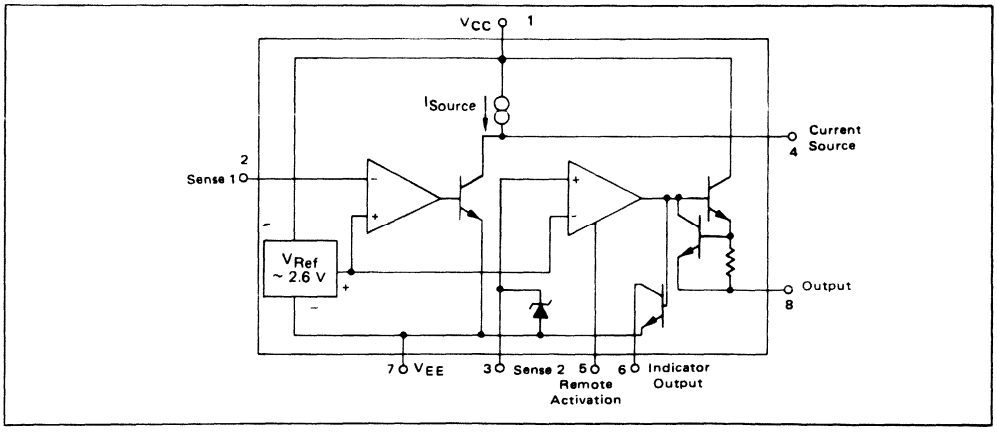
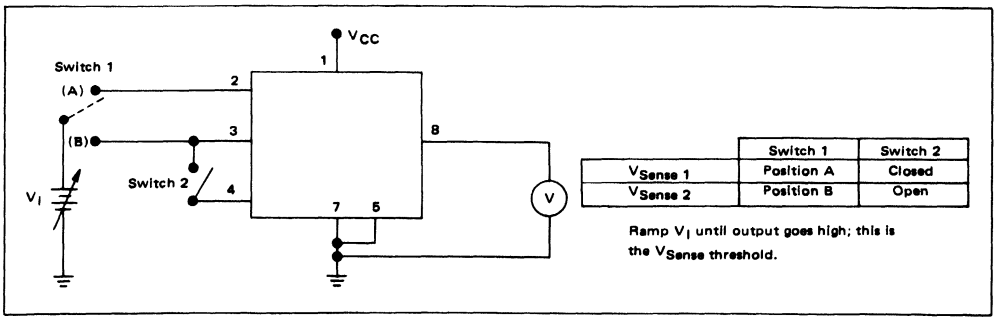


FIGURE 2 – SENSE VOLTAGE TEST CIRCUIT



	Switch 1	Switch 2
$V_{Sense\ 1}$	Position A	Closed
$V_{Sense\ 2}$	Position B	Open

Ramp V_I until output goes high; this is the V_{Sense} threshold.

FIGURE 3 – BASIC CIRCUIT CONFIGURATION

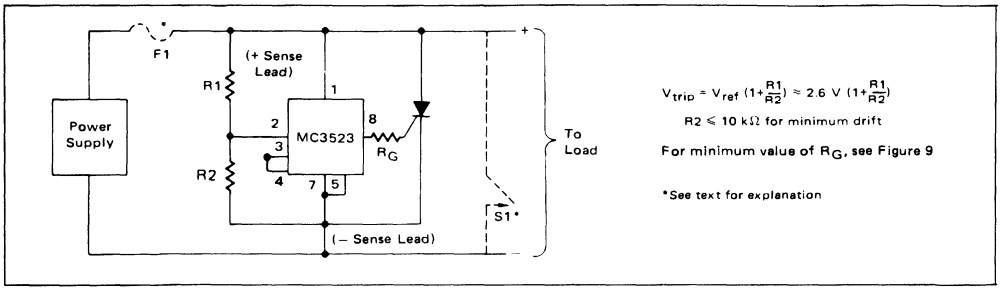


FIGURE 4 – CIRCUIT CONFIGURATION FOR SUPPLY VOLTAGE ABOVE 36 V

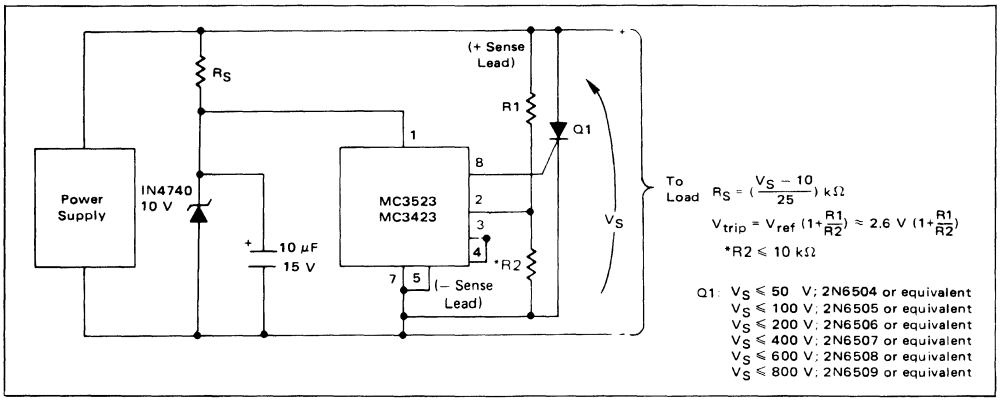
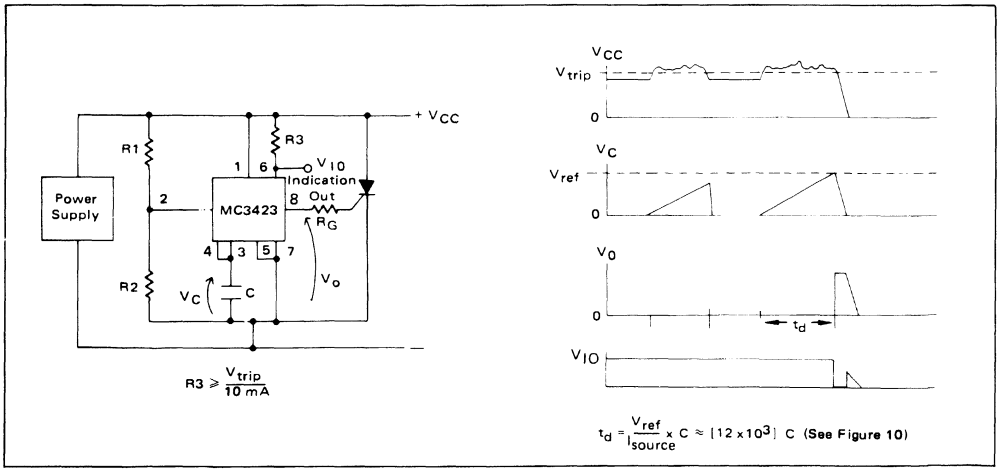


FIGURE 5 – BASIC CONFIGURATION FOR PROGRAMMABLE DURATION OF OVERVOLTAGE CONDITION BEFORE TRIP



APPLICATIONS INFORMATION

BASIC CIRCUIT CONFIGURATION

The basic circuit configuration of the MC3423/3523 OVP is shown in Figure 3 for supply voltages from 4.5 V to 36 V, and in Figure 4 for trip voltages above 36 V. The threshold or trip voltage at which the MC3423/3523 will trigger and supply gate drive to the crowbar SCR, Q1, is determined by the selection of R1 and R2. Their values can be determined by the equation given in Figures 3 and 4, or by the graph shown in Figure 8. The minimum value of the gate current limiting resistor, R_G, is given in Figure 9. Using this value of R_G, the SCR, Q1, will receive the greatest gate current possible without damaging the MC3423/3523. If lower output currents are required, R_G can be increased in value. The switch, S1, shown in Figure 3 may be used to reset the SCR crowbar. Otherwise, the power supply, across which the SCR is connected, must be shut down to reset the crowbar. If a non current-limited supply is used, a fuse or circuit breaker, F1, should be used to protect the SCR and/or the load.

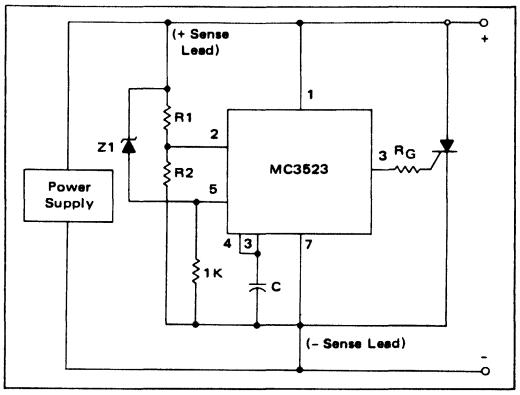
The circuit configurations shown in Figures 3 and 4 will have a typical propogation delay of 1.0 μs. If faster operation is desired, pin 3 may be connected to pin 2 with pin 4 left floating. This will result in decreasing the propogation delay to approximately 0.5 μs at the expense of a slightly increased TC for the trip voltage value.

CONFIGURATION FOR PROGRAMMABLE MINIMUM DURATION OF OVERVOLTAGE CONDITION BEFORE TRIPPING

In many instances, the MC3423/3523 OVP will be used in a noise environment. To prevent false tripping of the OVP circuit by noise which would not normally harm the load, MC3423/3523 has a programmable delay feature. To implement this feature, the circuit configuration of Figure 5 is used. In this configuration, a capacitor is connected from pin 3 to V_{EE}. The value of this capacitor determines the minimum duration of the overvoltage condition which is necessary to trip the OVP. The value of C can be found from Figure 10. The circuit operates in the following manner: When V_{CC} rises above the trip point set by R1 and R2, an internal current source (pin 4) begins charging the capacitor, C, connected to pin 3. If the overvoltage condition disappears before this occurs, the capacitor is discharged at a rate ≅ 10 times faster than the charging rate, resetting the timing feature until the next overvoltage condition occurs.

Occasionally, it is desired that immediate crowbarring of the supply occur when a high overvoltage condition occurs, while retaining the false tripping immunity of Figure 5. In this case, the circuit of Figure 6 can be used. The circuit will operate as previously described for small overvoltages, but will immediately trip if the power supply voltage exceeds V_{Z1} + 1.4 V.

FIGURE 6 – CONFIGURATION FOR PROGRAMMABLE DURATION OF OVERVOLTAGE CONDITION BEFORE TRIP/WITH IMMEDIATE TRIP AT HIGH OVERVOLTAGES



ADDITIONAL FEATURES

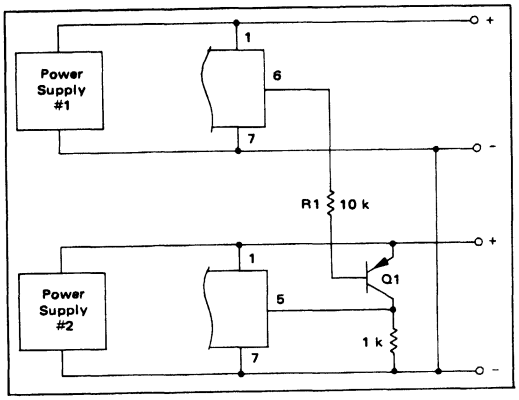
1. Activation Indication Output

An additional output for use as an indicator of OVP activation is provided by the MC3423/3523. This output is an open collector transistor which saturates when the OVP is activated. In addition, it can be used to clock an edge triggered flip-flop whose output inhibits or shuts down the power supply when the OVP trips. This reduces or eliminates the heatsinking requirements for the crowbar SCR.

2. Remote Activation Input

Another feature of the MC3423/3523 is its remote activation input, pin 5. If the volage on this CMOS/TTL compatible input is held below 0.8 V, the MC3423/3523 operates normally. However, if it is raised to a voltage above 2.0 V, the OVP output is activated independent of whether or not an overvoltage condition is present. It should be noted that pin 5 has an internal pull-up current source. This feature can be used to accomplish an orderly and sequenced shutdown of system power supplies during a system fault condition. In addition, the activation indication output of one MC3423/3523 can be used to activate another MC3423/3523 if a single transistor inverter is used to interface the former's indication output to the latter's remote activation input, as shown in Figure 7. In this circuit, the indication output (pin 6) of the MC3423 on power supply 1 is used to activate the MC3423 associated with power supply 2. Q1 is any small PNP with adequate voltage rating.

FIGURE 7 – CIRCUIT CONFIGURATION FOR ACTIVATING ONE MC3523 FROM ANOTHER



Note that both supplies have their negative output leads tied together (i.e., both are positive supplies). If their positive leads are common (two negative supplies) the emitter of Q1 would be moved to the positive lead of supply 1 and R1 would therefore have to be resized to deliver the appropriate drive to Q1.

CROWBAR SCR CONSIDERATIONS

Referring to Figure 11, it can be seen that the crowbar SCR, when activated, is subject to a large current surge from the output capacitance, C_{out}. This capacitance consists of the power supply output caps, the load's decoupling caps, and in the case of Figure 11A, the supply's input filter caps. This surge current is illustrated in Figure 12, and can cause SCR failure or degradation by any one of three mechanisms: di/dt, absolute peak surge, or I^2t. The interrelationship of these failure methods and the breadth of the applications make specification of the SCR by the semiconductor manufacturer difficult and expensive. Therefore, the designer must empirically determine the SCR and circuit elements which result in reliable and effective OVP operation. However, an understanding of the factors which influence the SCR's di/dt and surge capabilities simplifies this task.

1. di/dt

As the gate region of the SCR is driven on, its area of conduction takes a finite amount of time to grow, starting as a very small region and gradually spreading. Since the anode current flows through this turned-on gate region, very high current densities can occur in the gate region if high anode currents appear quickly (di/dt). This can result in immediate destruction of the SCR or gradual degradation of its forward blocking voltage capabilities – depending on the severity of the occasion.

FIGURE 8 – R1 versus TRIP VOLTAGE

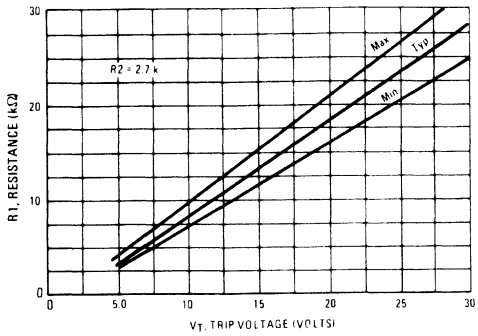


FIGURE 9 – MINIMUM R_G versus SUPPLY VOLTAGE

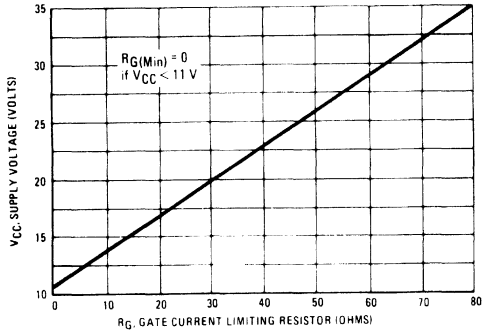


FIGURE 10 – CAPACITANCE versus MINIMUM OVERVOLTAGE DURATION

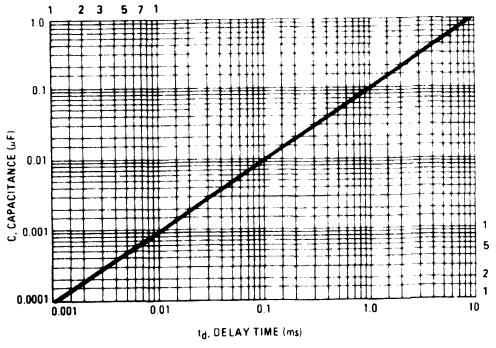


FIGURE 11 – TYPICAL CROWBAR OVP CIRCUIT CONFIGURATIONS

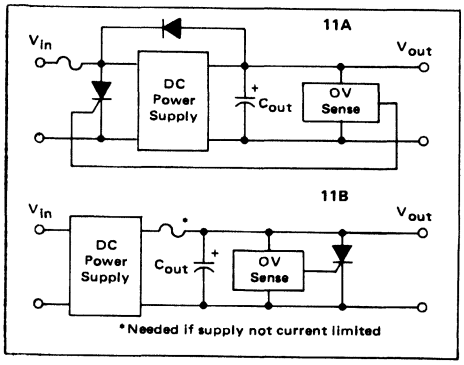


FIGURE 12 – CROWBAR SCR SURGE CURRENT WAVEFORM

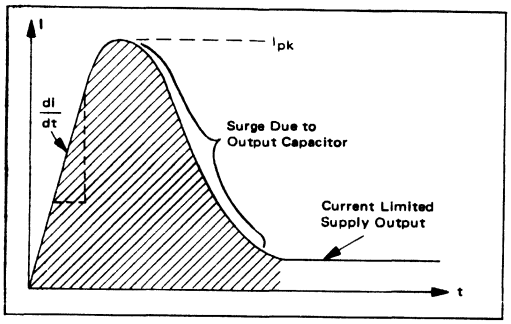
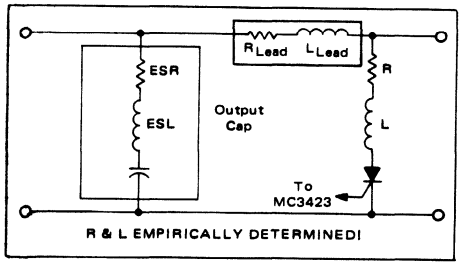


FIGURE 13 – CIRCUIT ELEMENTS AFFECTING SCR SURGE & di/dt



The usual design compromise then is to use a garden variety fuse (3AG or 3AB style) which cannot be relied on to blow before the thyristor does, and trust that if the SCR does fail, it will fail short circuit. In the majority of the designs, this will be the case, though this is difficult to guarantee. Of course, a sufficiently high surge will cause an open. These comments also apply to the fuse in Figure 11B.

For a complete and detailed treatment of SCR and fuse selection, refer to Motorola Application Note AN-789.

The value of di/dt that an SCR can safely handle is influenced by its construction and the characteristics of the gate drive signal. A center-gate-fire SCR has more di/dt capability than a corner-gate-fire type, and heavily overdriving (3 to 5 times I_{GT}) the SCR gate with a fast $< 1.0\ \mu s$ rise time signal will maximize its di/dt capability. A typical maximum number in phase control SCRs of less than 50 A(RMS) rating might be 200 $A/\mu s$, assuming a gate current of five times I_{GT} and $< 1.0\ \mu s$ rise time. If having done this, a di/dt problem is seen to still exist, the designer can also decrease the di/dt of the current waveform by adding inductance in series with the SCR, as shown in Figure 13. Of course, this reduces the circuit's ability to rapidly reduce the dc bus voltage and a tradeoff must be made between speedy voltage reduction and di/dt.

2. Surge Current

If the peak current and/or the duration of the surge is excessive, immediate destruction due to device overheating will result. The surge capability of the SCR is directly proportional to its die area. If the surge current cannot be reduced (by adding series resistance — see Figure 13) to a safe level which is consistent with the system's requirements for speedy bus voltage reduction, the designer must use a higher current SCR. This may result in the average current capability of the SCR exceeding the steady state current requirements imposed by the dc power supply.

A WORD ABOUT FUSING

Before leaving the subject of the crowbar SCR, a few words about fuse protection are in order. Referring back to Figure 11A, it will be seen that a fuse is necessary if the power supply to be protected is not output current limited. This fuse is not meant to prevent SCR failure but rather to prevent a fire!

In order to protect the SCR, the fuse would have to possess an I^2t rating less than that of the SCR and yet have a high enough continuous current rating to survive normal supply output currents. In addition, it must be capable of successfully clearing the high short circuit currents from the supply. Such a fuse as this is quite expensive, and may not even be available.

CROWBAR SCR SELECTION GUIDE

As an aid in selecting an SCR for crowbar use, the following selection guide is presented.

DEVICE	I_{RMS}	I_{FSM}	PACKAGE
2N6400 Series	16A	160A	TO220 Plastic
2N6504 Series	25A	160A	TO220 Plastic
2N1842 Series	16A	125A	Metal Stud
2N2573 Series	25A	260A	Metal TO-3 Type
2N681 Series	25A	200A	Metal Stud
MCR3935-1 Series	35A	350A	Metal Stud
MCR81-5 Series	80A	1000A	Metal Stud

MOTOROLA

MC3425

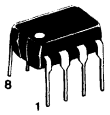
POWER SUPPLY SUPERVISORY/OVER-UNDER-VOLTAGE PROTECTION CIRCUIT

The MC3425 is a power supply supervisory circuit containing all the necessary functions required to monitor over- and under-voltage fault conditions. These integrated circuits contain dedicated over- and under-voltage sensing channels with independently programmable time delays. The over-voltage channel has a high current Drive Output for use in conjunction with an external SCR "Crowbar" for shutdown. The under-voltage channel input comparator has hysteresis which is externally programmable, and an open-collector output for fault indication.

- Dedicated Over- And Under-Voltage Sensing
- Programmable Hysteresis Of Under-Voltage Comparator
- Internal 2.5 V Reference
- 300 mA Over-Voltage Drive Output
- 30 mA Under-Voltage Indicator Output
- Programmable Time Delays
- 4.5 V to 40 V Operation

POWER SUPPLY SUPERVISORY/ OVER-UNDER-VOLTAGE PROTECTION CIRCUIT

SILICON MONOLITHIC INTEGRATED CIRCUIT



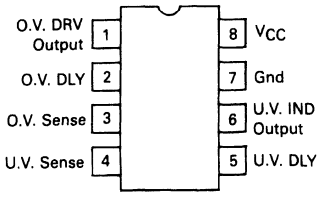
P1 SUFFIX
PLASTIC PACKAGE
CASE 626-05

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	40	Vdc
Comparator Input Voltage Range (Note 1)	V_{IR}	−0.3 to +40	Vdc
Drive Output Short-Circuit Current	$I_{OS(DRV)}$	Internally Limited	mA
Indicator Output Voltage	V_{IND}	0 to 40	Vdc
Indicator Output Sink Current	I_{IND}	30	mA
Power Dissipation and Thermal Characteristics Maximum Power Dissipation @ T_A = 70°C Thermal Resistance Junction to Air	 P_D $R_{\theta JA}$	 1000 80	 mW °C/W
Operating Junction Temperature	T_J	+150	°C
Operating Ambient Temperature Range	T_A	0 to +70	°C
Storage Temperature Range	T_{stg}	−55 to +150	°C

NOTE: (1) The input signal voltage should not be allowed to go negative by more than 300 mV or positive by more than 40 V, independent of V_{CC}, without device destruction.

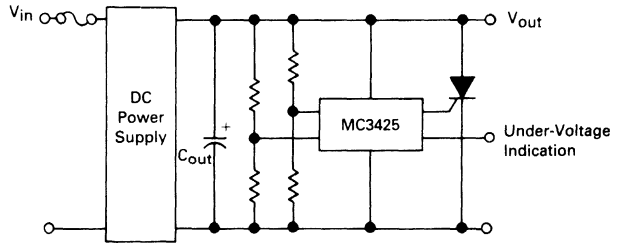
PIN CONNECTIONS



(Top View)

TYPICAL APPLICATION

Over-Voltage Crowbar Protection, Under-Voltage Indication



ORDERING INFORMATION		
Device	**Temperature Range**	**Package**
MC3425P1	0 to +70°C	Plastic DIP

ELECTRICAL CHARACTERISTICS ($4.5\ V \le V_{CC} \le 40\ V$; $T_A = T_{low}$ to T_{high} [see Note 2] unless otherwise specified.)

Characteristic	Symbol	Min	Typ	Max	Unit
REFERENCE SECTION					
Sense Trip Voltage (Reference Voltage) V_{CC} = 15 V T_A = 25°C T_{low} to T_{high} (Note 2)	V_{Sense}	 2.4 2.33	 2.5 2.5	 2.6 2.63	Vdc
Line Regulation of V_{Sense} $4.5\ V \le V_{CC} \le 40\ V$; T_J = 25°C	Reg_{line}	—	7.0	15	mV
Power Supply Voltage Operating Range	V_{CC}	4.5	—	40	Vdc
Power Supply Current V_{CC} = 40 V; T_A = 25°C; No Output Loads O.V. Sense (Pin 3) = 0 V; U.V. Sense (Pin 4) = V_{CC}	$I_{CC(off)}$	—	8.5	10	mA
O.V. Sense (Pin 3) = V_{CC}; U.V. Sense (Pin 4) = 0 V	$I_{CC(on)}$	—	16.5	19	mA
INPUT SECTION					
Input Bias Current, O.V. and U.V. Sense	I_{IB}	—	1.0	2.0	μA
Hysteresis Activation Voltage, U.V. Sense V_{CC} = 15 V; T_A = 25°C; I_H = 10% I_H = 90%	$V_{H(act)}$	 — —	 0.6 0.8	 — —	V
Hysteresis Current, U.V. Sense V_{CC} = 15 V; T_A = 25°C; U.V. Sense (Pin 4) = 2.5 V	I_H	9.0	12.5	16	μA
Delay Pin Voltage (I_{DLY} = 0 mA) Low State High State	 $V_{OL(DLY)}$ $V_{OH(DLY)}$	 — $V_{CC}-0.5$	 0.2 $V_{CC}-0.15$	 0.5 —	V
Delay Pin Source Current V_{CC} = 15 V; V_{DLY} = 0 V	$I_{DLY(source)}$	140	200	260	μA
Delay Pin Sink Current V_{CC} = 15 V; V_{DLY} = 2.5 V	$I_{DLY(sink)}$	1.8	3.0	—	mA
OUTPUT SECTION					
Drive Output Peak Current (T_A = 25°C)	$I_{DRV(peak)}$	200	300	—	mA
Drive Output Voltage I_{DRV} = 100 mA; T_A = 25°C	$V_{OH(DRV)}$	$V_{CC}-2.5$	$V_{CC}-2.0$	—	V
Drive Output Leakage Current V_{DRV} = 0 V	$I_{DRV(leak)}$	—	15	200	nA
Drive Output Current Slew Rate (T_A = 25°C)	di dt	—	2.0	—	A/μs
Drive Output V_{CC} Transient Rejection V_{CC} = 0 V to 15 V at dV/dt = 200 V/μs; O.V. Sense (Pin 3) = 0 V; T_A = 25°C	$I_{DRV(trans)}$	—	1.0	—	mA (Peak)
Indicator Output Saturation Voltage I_{IND} = 30 mA; T_A = 25°C	$V_{IND(sat)}$	—	560	800	mV
Indicator Output Leakage Current $V_{OH(IND)}$ = 40 V	$I_{IND(leak)}$	—	25	200	nA
Output Comparator Threshold Voltage (Note 3)	$V_{th(OC)}$	2.33	2.5	2.63	V
Propagation Delay Time (V_{CC} = 15 V; T_A = 25°C) Input to Drive Output or Indicator Output 100 mV Overdrive, C_{DLY} = 0 μF	$t_{PLH(IN/OUT)}$	—	1.7	—	μs
Input to Delay 2.5 V Overdrive (0 V to 5.0 V Step)	$t_{PLH(IN/DLY)}$	—	700	—	ns

NOTES:
(2) T_{low} = 0°C T_{high} = +70°C
(3) The $V_{th(OC)}$ limits are approximately the V_{Sense} limits over the applicable temperature range.

FIGURE 1 — HYSTERESIS CURRENT versus HYSTERESIS ACTIVATION VOLTAGE

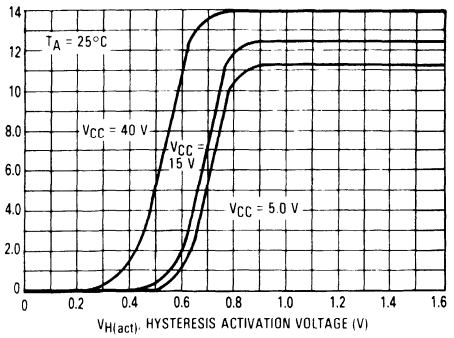


FIGURE 2 — HYSTERESIS ACTIVATION VOLTAGE versus TEMPERATURE

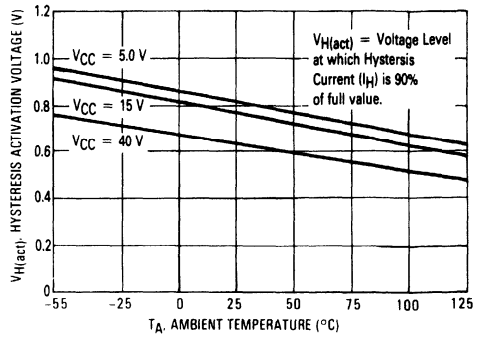


FIGURE 3 — HYSTERESIS CURRENT versus TEMPERATURE

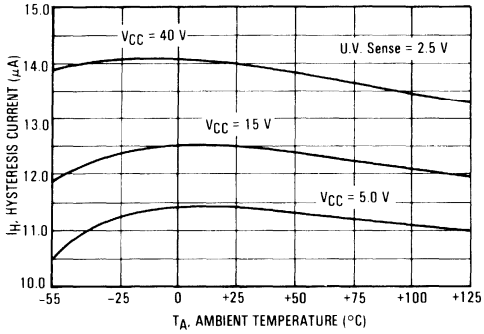


FIGURE 4 — SENSE TRIP VOLTAGE CHANGE versus TEMPERATURE

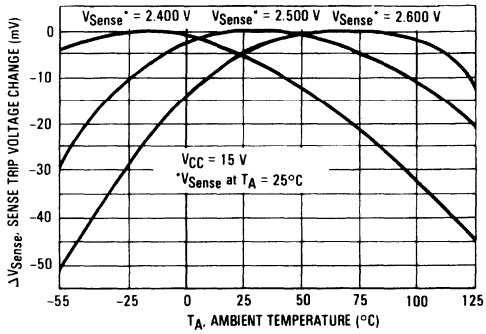


FIGURE 5 — OUTPUT DELAY TIME versus DELAY CAPACITANCE

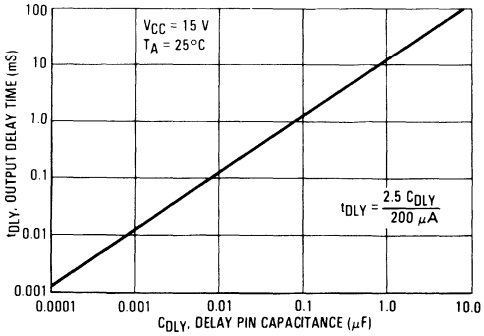


FIGURE 6 — DELAY PIN SOURCE CURRENT versus TEMPERATURE

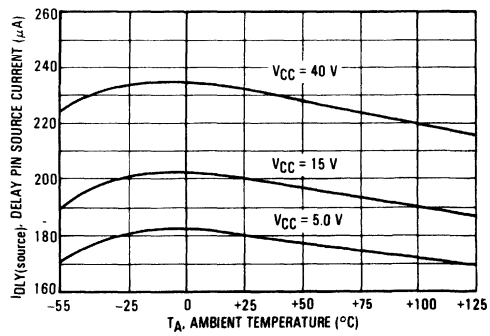


FIGURE 7 — DRIVE OUTPUT SATURATION VOLTAGE versus OUTPUT PEAK CURRENT

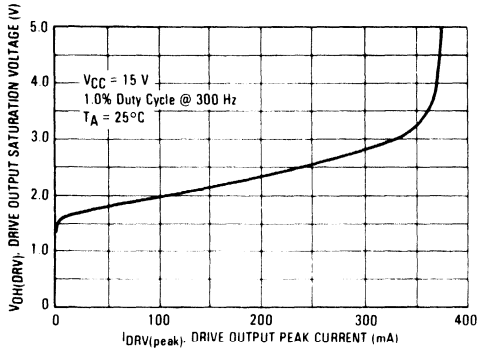


FIGURE 8 — INDICATOR OUTPUT SATURATION VOLTAGE versus OUTPUT SINK CURRENT

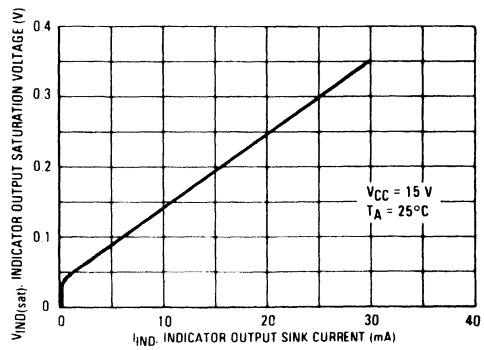


FIGURE 9 — DRIVE OUTPUT SATURATION VOLTAGE versus TEMPERATURE

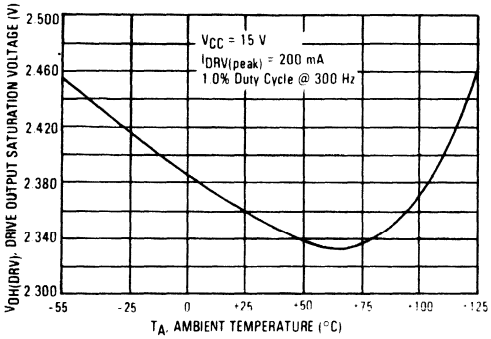
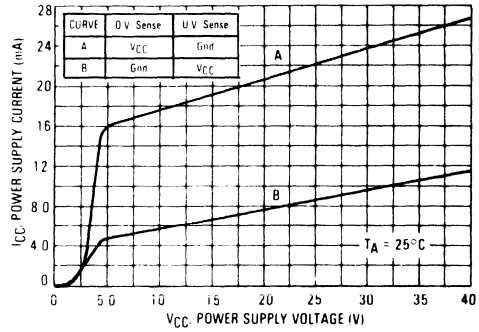
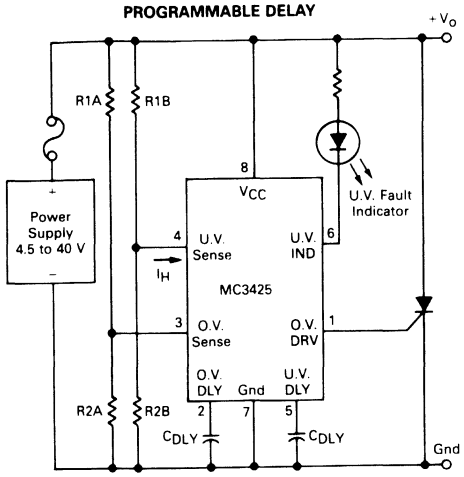


FIGURE 10 — POWER SUPPLY CURRENT versus VOLTAGE



APPLICATIONS INFORMATION

FIGURE 11 — OVERVOLTAGE PROTECTION AND UNDER VOLTAGE FAULT INDICATION WITH PROGRAMMABLE DELAY



U.V. Hysteresis = $I_H \left(\frac{R1B\ R2B}{R1B + R2B} \right)$ $V_{O(trip)} = 2.5\ V \left(1 + \frac{R1A}{R2A} \right)$

$t_{DLY} = 12500\ C_{DLY}$

FIGURE 12 — OVERVOLTAGE PROTECTION OF 5.0 V SUPPLY WITH LINE LOSS DETECTOR

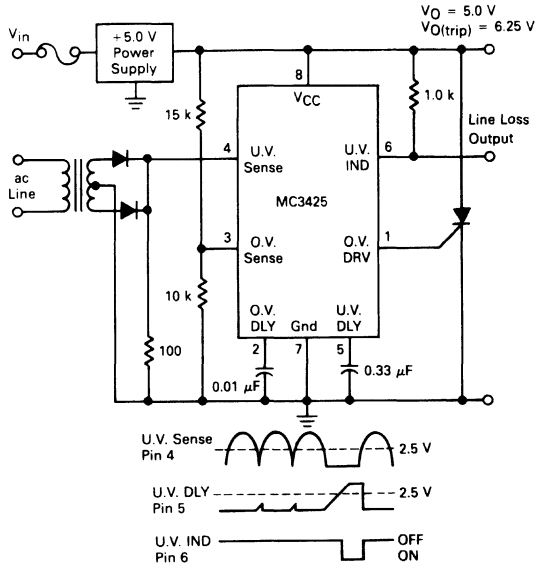


FIGURE 13 — OVERVOLTAGE AUDIO ALARM CIRCUIT

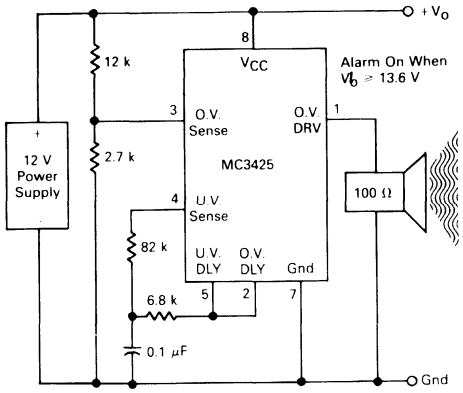
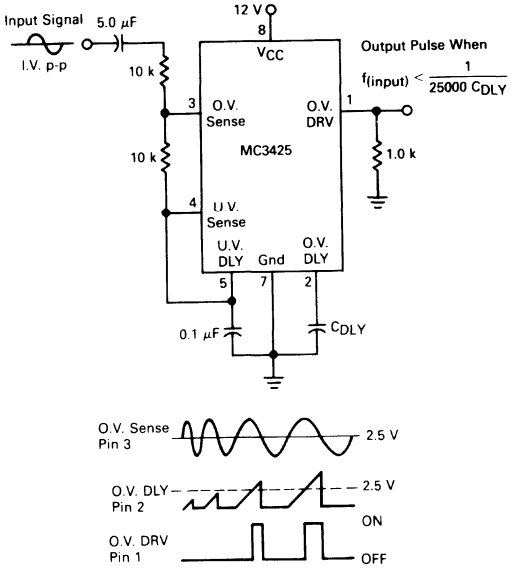


FIGURE 14 — PROGRAMMABLE FREQUENCY SWITCH



CIRCUIT DESCRIPTION

The MC3425 is a power supply supervisory circuit containing all the necessary functions required to monitor over- and under-voltage fault conditions. The block diagram is shown below in Figure 15. The Over-Voltage (O.V.) and Under-Voltage (U.V.) Input Comparators are both referenced to an internal 2.5 V regulator. The U.V. Input Comparator has a feedback activated 12.5 μA current sink (I_H) which is used for programming the input hysteresis voltage (V_H). The source resistance feeding this input (R_H) determines the amount of hysteresis voltage by $V_H = I_H R_H = 12.5 \times 10^{-6} R_H$.

Separate Delay pins (O.V. DLY, U.V. DLY) are provided for each channel to independently delay the Drive and Indicator outputs, thus providing greater input noise immunity. The two Delay pins are essentially the outputs of the respective input comparators, and provide a constant current source, $I_{DLY(source)}$, of typically 200 μA when the non-inverting input voltage is greater than the inverting input level. A capacitor connected from these Delay pins to ground, will establish a predictable delay time (t_{DLY}) for the Drive and Indicator outputs. The Delay pins are internally connected to the non-inverting inputs of the O.V. and U.V. Output Comparators, which are referenced to the internal 2.5 V regulator. Therefore, delay time (t_{DLY}) is based on the constant current source, $I_{DLY(source)}$, charging the external delay capacitor (C_{DLY}) to 2.5 volts.

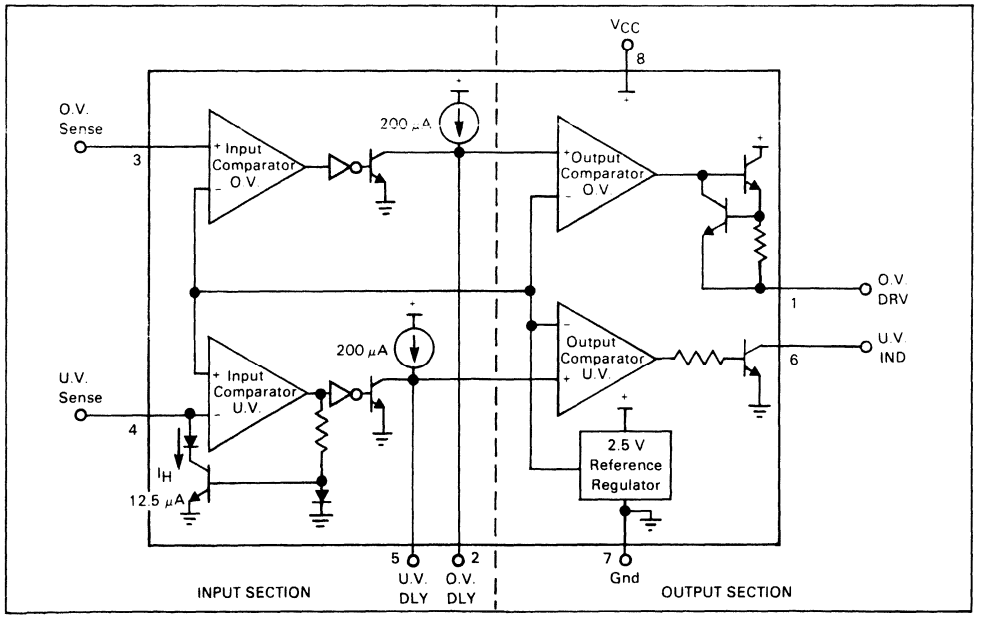
$$t_{DLY} = \frac{V_{ref}\, C_{DLY}}{I_{DLY(source)}} = \frac{2.5\, C_{DLY}}{200\ \mu A} = 12500\, C_{DLY}$$

Figure 5 provides C_{DLY} values for a wide range of time delays. The Delay pins are pulled low when the respective input comparator's non-inverting input is less than the inverting input. The sink current, $I_{DLY(sink)}$, capability of the Delay pins is $\geq$ 1.8 mA and is much greater than the typical 200 μA source current, thus enabling a relatively fast delay capacitor discharge time.

The Over-Voltage Drive Output is a current-limited emitter-follower capable of sourcing 300 mA at a turn-on slew rate of 2.0 A/μs, ideal for driving "Crowbar" SCR's. The Under-Voltage Indicator Output is an open-collector, NPN transistor, capable of sinking 30 mA to provide sufficient drive for LED's, small relays or shut-down circuitry. These current capabilities apply to both channels operating simultaneously, providing device power dissipation limits are not exceeded.

The MC3425 has an internal 2.5 V bandgap reference regulator with an accuracy of ±4.0% for the basic devices and ±1.0% for the A-suffix device types at 25°C. The reference has a typical temperature coefficient of 30 ppm/°C for A-suffix devices.

FIGURE 15 — BLOCK DIAGRAM



Note: All voltages and currents are nominal.

CROWBAR SCR CONSIDERATIONS

Referring to Figure 16, it can be seen that the crowbar SCR, when activated, is subject to a large current surge from the output capacitance, C_{out}. This capacitance consists of the power supply output capacitors, the load's decoupling capacitors, and in the case of Figure 16A, the supply's input filter capacitors. This surge current is illustrated in Figure 17, and can cause SCR failure or degradation by any one of three mechanisms: di/dt, absolute peak surge, or I^2t. The interrelationship of these failure methods and the breadth of the applications make specification of the SCR by the semiconductor manufacturer difficult and expensive. Therefore, the designer must empirically determine the SCR and circuit elements which result in reliable and effective OVP operation. However, an understanding of the factors which influence the SCR's di/dt and surge capabilities simplifies this task.

1. di/dt

As the gate region of the SCR is driven on, its area of conduction takes a finite amount of time to grow, starting as a very small region and gradually spreading. Since the anode current flows through this turned-on gate region, very high current densities can occur in the gate region if high anode currents appear quickly (di/dt). This can result in immediate destruction of the SCR or gradual degradation of its forward blocking voltage capabilities — depending on the severity of the occasion.

The value of di/dt that an SCR can safely handle is influenced by its construction and the characteristics of the gate drive signal. A center-gate-fire SCR has more di/dt capability than a corner-gate-fire type, and heavily overdriving (3 to 5 times I_{GT}) the SCR gate with a fast $<1.0\ \mu s$ rise time signal will maximize its di/dt capability. A typical maximum number in phase control SCRs of less than 50 A(RMS) rating might be 200 $A/\mu s$, assuming a gate current of five times I_{GT} and $< 1.0\ \mu s$ rise time. If having done this, a di/dt problem is seen to still exist, the designer can also decrease the di/dt of the current waveform by adding inductance in series with the SCR, as shown in Figure 18. Of course, this reduces the circuit's ability to rapidly reduce the dc bus voltage and a tradeoff must be made between speedy voltage reduction and di/dt.

FIGURE 16 — TYPICAL CROWBAR CIRCUIT CONFIGURATIONS

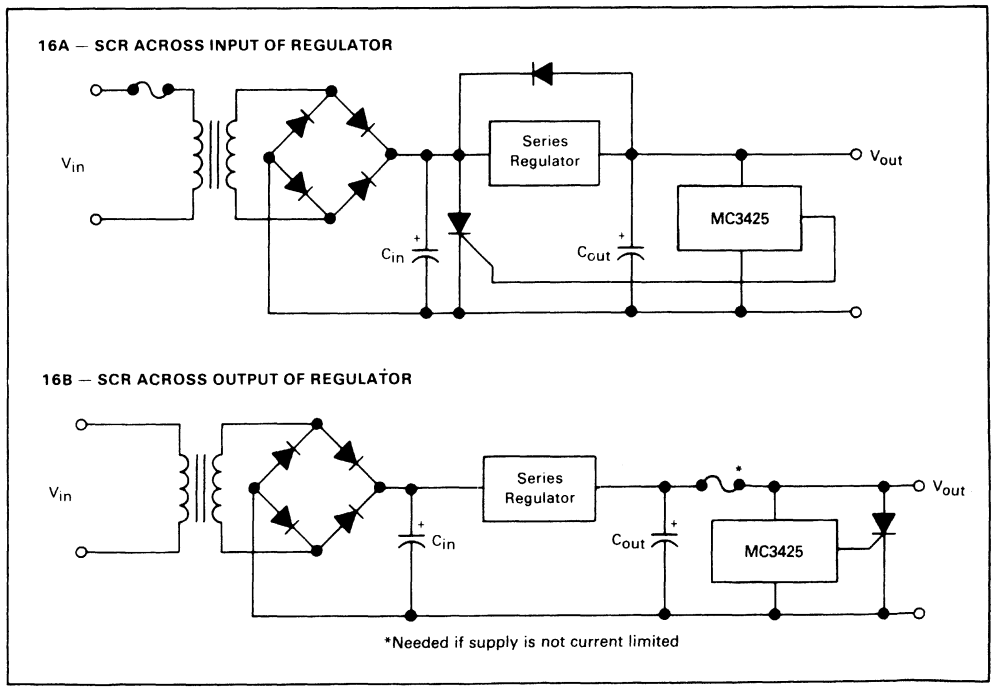
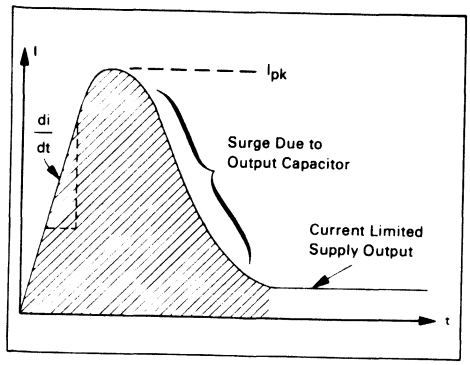


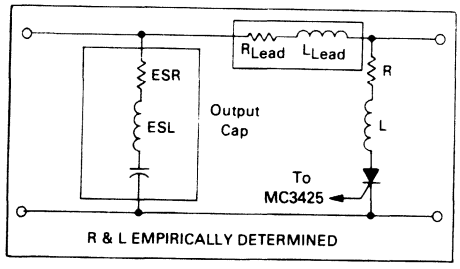
FIGURE 17 — CROWBAR SCR SURGE CURRENT WAVEFORM



2. Surge Current

If the peak current and/or the duration of the surge is excessive, immediate destruction due to device overheating will result. The surge capability of the SCR is directly proportional to its die area. If the surge current cannot be reduced (by adding series resistance — see Figure 18) to a safe level which is consistent with the system's requirements for speedy bus voltage reduction, the designer must use a higher current SCR. This may result in the average current capability of the SCR exceeding the steady state current requirements imposed by the dc power supply.

FIGURE 18 — CIRCUIT ELEMENTS AFFECTING SCR SURGE & di/dt



R & L EMPIRICALLY DETERMINED

A WORD ABOUT FUSING

Before leaving the subject of the crowbar SCR, a few words about fuse protection are in order. Referring back to Figure 16A, it will be seen that a fuse is necessary if the power supply to be protected is not output current limited. This fuse is not meant to prevent SCR failure but rather to prevent a fire!

In order to protect the SCR, the fuse would have to possess an I^2t rating less than that of the SCR and yet have a high enough continuous current rating to survive normal supply output currents. In addition, it must be capable of successfully clearing the high short circuit currents from the supply. Such a fuse as this is quite expensive, and may not even be available.

The usual design compromise then is to use a garden variety fuse (3AG or 3AB style) which cannot be relied on to blow before the thyristor does, and trust that if the SCR does fail, it will fail short circuit. In the majority of the designs, this will be the case, though this is difficult to guarantee. Of course, a sufficiently high surge will cause an open. These comments also apply to the fuse in Figure 16B.

CROWBAR SCR SELECTION GUIDE

As an aid in selecting an SCR for crowbar use, the following selection guide is presented.

DEVICE	I_{RMS}	I_{FSM}	PACKAGE
MCR67 Series	12 A	100 A	Metal Stud
MCR68 Series	12 A	100 A	TO-220 Plastic
2N1842 Series	16 A	125 A	Metal Stud
2N6400 Series	16 A	160 A	TO-220 Plastic
2N6504 Series	25 A	160 A	TO-220 Plastic
2N681 Series	25 A	200 A	Metal Stud
2N2573 Series	25 A	260 A	TO-3 Metal Can
MCR69 Series	25 A	300 A	TO-220 Plastic
MCR70 Series	35 A	350 A	Metal Stud
MCR71 Series	55 A	550 A	Metal Stud

For a complete and detailed treatment of SCR and fuse selection refer to Motorola Application Note AN789.

MOTOROLA

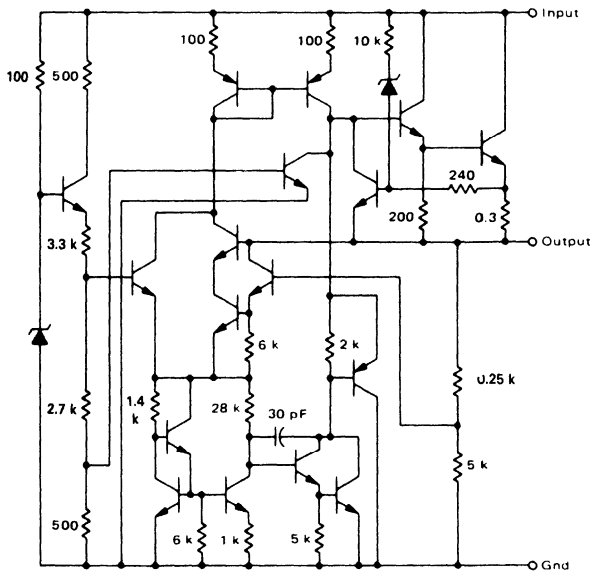
MC7800 Series

THREE-TERMINAL POSITIVE VOLTAGE REGULATORS

These voltage regulators are monolithic integrated circuits designed as fixed-voltage regulators for a wide variety of applications including local, on-card regulation. These regulators employ internal current limiting, thermal shutdown, and safe-area compensation. With adequate heatsinking they can deliver output currents in excess of 1.0 ampere. Although designed primarily as a fixed voltage regulator, these devices can be used with external components to obtain adjustable voltages and currents.

- Output Current in Excess of 1.0 Ampere
- No External Components Required
- Internal Thermal Overload Protection
- Internal Short-Circuit Current Limiting
- Output Transistor Safe-Area Compensation
- Output Voltage Offered in 2% and 4% Tolerance

REPRESENTATIVE SCHEMATIC DIAGRAM



ORDERING INFORMATION

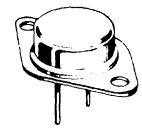
Device	Output Voltage Tolerance	Tested Operating Junction Temp. Range	Package
MC78XXK	4%	−55 to +150°C	Metal Power
MC78XXAK*	2%		
MC78XXCK	4%	0 to +125°C	
MC78XXACK*	2%		
MC78XXCT	4%		Plastic Power
MC78XXACT	2%		
MC78XXBT	4%	−40 to +125°C	

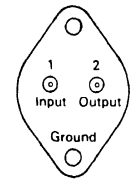
*2% regulators in Metal Power packages are available in 5, 12 and 15 volt devices.

THREE-TERMINAL POSITIVE FIXED VOLTAGE REGULATORS

SILICON MONOLITHIC INTEGRATED CIRCUITS

K SUFFIX
METAL PACKAGE
CASE 1-03

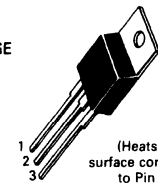




(Bottom View)

Pins 1 and 2 electrically isolated from case. Case is third electrical connection

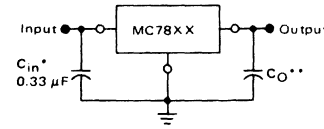
T SUFFIX
PLASTIC PACKAGE
CASE 221A-04



PIN 1. INPUT
2. GROUND
3. OUTPUT

(Heatsink surface connected to Pin 2.)

STANDARD APPLICATION



A common ground is required between the input and the output voltages. The input voltage must remain typically 2.0 V above the output voltage even during the low point on the input ripple voltage.

XX = these two digits of the type number indicate voltage.

* = C_{in} is required if regulator is located an appreciable distance from power supply filter.

** = C_O is not needed for stability; however, it does improve transient response.

XX indicates nominal voltage

TYPE NO./VOLTAGE			
MC7805	5.0 Volts	MC7812	12 Volts
MC7806	6.0 Volts	MC7815	15 Volts
MC7808	8.0 Volts	MC7818	18 Volts
MC7809	9.0 Volts	MC7824	24 Volts

MAXIMUM RATINGS (T_A = +25°C unless otherwise noted.)

Rating	Symbol	Value	Unit
Input Voltage (5.0 V – 18 V) (24 V)	V_{in}	35 40	Vdc
Power Dissipation and Thermal Characteristics			
Plastic Package			
T_A = +25°C	P_D	Internally Limited	Watts
Derate above T_A = +25°C	$1/\theta_{JA}$	15.4	mW/°C
Thermal Resistance, Junction to Air	θ_{JA}	65	°C/W
T_C = +25°C	P_D	Internally Limited	Watts
Derate above T_C = +75°C (See Figure 1)	$1/\theta_{JC}$	200	mW/°C
Thermal Resistance, Junction to Case	θ_{JC}	5.0	°C/W
Metal Package			
T_A = +25°C	P_D	Internally Limited	Watts
Derate above T_A = +25°C	$1/\theta_{JA}$	22.5	mW/°C
Thermal Resistance, Junction to Air	θ_{JA}	45	°C/W
T_C = +25°C	P_D	Internally Limited	Watts
Derate above T_C = +65°C (See Figure 2)	$1/\theta_{JC}$	182	mW/°C
Thermal Resistance, Junction to Case	θ_{JC}	5.5	°C/W
Storage Junction Temperature Range	T_{stg}	–65 to +150	°C
Operating Junction Temperature Range	T_J		°C
MC7800,A		–55 to +150	
MC7800C,AC		0 to +150	
MC7800B		–40 to +150	

DEFINITIONS

Line Regulation — The change in output voltage for a change in the input voltage. The measurement is made under conditions of low dissipation or by using pulse techniques such that the average chip temperature is not significantly affected.

Load Regulation — The change in output voltage for a change in load current at constant chip temperature.

Maximum Power Dissipation — The maximum total device dissipation for which the regulator will operate within specifications.

Quiescent Current — That part of the input current that is not delivered to the load.

Output Noise Voltage — The rms ac voltage at the output, with constant load and no input ripple, measured over a specified frequency range.

Long Term Stability — Output voltage stability under accelerated life test conditions with the maximum rated voltage listed in the devices' electrical characteristics and maximum power dissipation.

MC7805, B, C

ELECTRICAL CHARACTERISTICS (V_{in} = 10 V, I_O = 500 mA, T_J = T_{low} to T_{high} [Note 1] unless otherwise noted).

Characteristic	Symbol	MC7805			MC7805B			MC7805C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Output Voltage (T_J = +25°C)	V_O	4.8	5.0	5.2	4.8	5.0	5.2	4.8	5.0	5.2	Vdc
Output Voltage (5.0 mA ≤ I_O ≤ 1.0 A, P_O ≤ 15 W) 7.0 Vdc ≤ V_{in} ≤ 20 Vdc 8.0 Vdc ≤ V_{in} ≤ 20 Vdc	V_O	— 4.65	— 5.0	— 5.35	— 4.75	— 5.0	— 5.25	4.75 —	5.0 —	5.25 —	Vdc
Line Regulation (T_J = +25°C, Note 2) 7.0 Vdc ≤ V_{in} ≤ 25 Vdc 8.0 Vdc ≤ V_{in} ≤ 12 Vdc	Reg_{line}	— —	2.0 1.0	50 25	— —	7.0 2.0	100 50	— —	7.0 2.0	100 50	mV
Load Regulation (T_J = +25°C, Note 2) 5.0 mA ≤ I_O ≤ 1.5 A 250 mA ≤ I_O ≤ 750 mA	Reg_{load}	— —	25 8.0	100 25	— —	40 15	100 50	— —	40 15	100 50	mV
Quiescent Current (T_J = +25°C)	I_B	—	3.2	6.0	—	4.3	8.0	—	4.3	8.0	mA
Quiescent Current Change 7.0 Vdc ≤ V_{in} ≤ 25 Vdc 8.0 Vdc ≤ V_{in} ≤ 25 Vdc 5.0 mA ≤ I_O ≤ 1.0 A	ΔI_B	— — —	— 0.3 0.04	— 0.8 0.5	— — —	— — —	— 1.3 0.5	— — —	— — —	1.3 — 0.5	mA
Ripple Rejection 8.0 Vdc ≤ V_{in} ≤ 18 Vdc, f = 120 Hz	RR	68	75	—	—	68	—	—	68	—	dB
Dropout Voltage (I_O = 1.0 A, T_J = +25°C)	V_{in} - V_O	—	2.0	2.5	—	2.0	—	—	2.0	—	Vdc
Output Noise Voltage (T_A = +25°C) 10 Hz ≤ f ≤ 100 kHz	V_n	—	10	40	—	10	—	—	10	—	$\mu V / V_O$
Output Resistance f = 1.0 kHz	r_O	—	17	—	—	17	—	—	17	—	mΩ
Short-Circuit Current Limit (T_A = +25°C) V_{in} = 35 Vdc	I_{sc}	—	0.2	1.2	—	0.2	—	—	0.2	—	A
Peak Output Current (T_J = +25°C)	I_{max}	1.3	2.5	3.3	—	2.2	—	—	2.2	—	A
Average Temperature Coefficient of Output Voltage	TCV_O	—	±0.6	—	—	-1.1	—	—	-1.1	—	mV/°C

MC7805A, AC

ELECTRICAL CHARACTERISTICS (V_{in} = 10 V, I_O = 1.0 A, T_J = T_{low} to T_{high} [Note 1] unless otherwise noted)

Characteristics	Symbol	MC7805A			MC7805AC			Unit
		Min	Typ	Max	Min	Typ	Max	
Output Voltage (T_J = +25°C)	V_O	4.9	5.0	5.1	4.9	5.0	5.1	Vdc
Output Voltage (5.0 mA ≤ I_O ≤ 1.0 A, P_O ≤ 15 W) 7.5 Vdc ≤ V_{in} ≤ 20 Vdc	V_O	4.8	5.0	5.2	4.8	5.0	5.2	Vdc
Line Regulation (Note 2) 7.5 Vdc ≤ V_{in} ≤ 25 Vdc, I_O = 500 mA 8.0 Vdc ≤ V_{in} ≤ 12 Vdc 8.0 Vdc ≤ V_{in} ≤ 12 Vdc, T_J = +25°C 7.3 Vdc ≤ V_{in} ≤ 20 Vdc, T_J = +25°C	Reg_{line}	— — — —	2.0 3.0 1.0 2.0	10 10 4.0 10	— — — —	7.0 10 2.0 7.0	50 50 25 50	mV
Load Regulation (Note 2) 5.0 mA ≤ I_O ≤ 1.5 A, T_J = +25°C 5.0 mA ≤ I_O ≤ 1.0 A 250 mA ≤ I_O ≤ 750mA, T_J = +25°C 250 mA ≤ I_O ≤ 750 mA	Reg_{load}	— — — —	2.0 2.0 1.0 1.0	25 25 15 25	— — — —	25 25 — 8.0	100 100 — 50	mV
Quiescent Current T_J = +25°C	I_B	— —	— 3.2	5.0 4.0	— —	— 4.3	6.0 6.0	mA
Quiescent Current Change 8.0 Vdc ≤ V_{in} ≤ 25 Vdc, I_O = 500 mA 7.5 Vdc ≤ V_{in} ≤ 20 Vdc, T_J = +25°C 5.0 mA ≤ I_O ≤ 1.0 A	ΔI_B	— — —	0.3 0.2 0.04	0.5 0.5 0.2	— — —	— — —	0.8 0.8 0.5	mA
Ripple Rejection 8.0 Vdc ≤ V_{in} ≤ 18 Vdc, f = 120 Hz, T_J = +25°C 8.0 Vdc ≤ V_{in} ≤ 18 Vdc, f = 120 Hz, I_O = 500 mA	RR	68 68	75 75	— —	— —	— 68	— —	dB
Dropout Voltage (I_O = 1.0 A, T_J = +25°C)	V_{in} - V_O	—	2.0	2.5	—	2.0	—	Vdc
Output Noise Voltage (T_A = +25°C) 10 Hz ≤ f ≤ 100 kHz	V_n	—	10	40	—	10	—	$\mu V / V_O$
Output Resistance (f = 1.0 kHz)	r_O	—	2.0	—	—	17	—	mΩ
Short-Circuit Current Limit (T_A = +25°C) V_{in} = 35 Vdc	I_{sc}	—	0.2	1.2	—	0.2	—	A
Peak Output Current (T_J = +25°C)	I_{max}	1.3	2.5	3.3	—	2.2	—	A
Average Temperature Coefficient of Output Voltage	TCV_O	—	±0.6	—	—	-1.1	—	mV/°C

NOTES: 1. T_{low} = -55°C for MC78XX, A
= 0° for MC78XXC, AC
= -40°C for MC78XXB
T_{high} = +150°C for MC78XX, A
= +125°C for MC78XXC, AC, B

2. Load and line regulation are specified at constant junction temperature. Changes in V_O due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

MC7806, B, C

ELECTRICAL CHARACTERISTICS (V_{in} = 11 V, I_O = 500 mA, T_J = T_{low} to T_{high} [Note 1] unless otherwise noted).

Characteristic	Symbol	MC7806			MC7806B			MC7806C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Output Voltage (T_J = +25°C)	V_O	5.75	6.0	6.25	5.75	6.0	6.25	5.75	6.0	6.25	Vdc
Output Voltage (5.0 mA ≤ I_O ≤ 1.0 A, P_O ≤ 15 W) 8.0 Vdc ≤ V_{in} ≤ 21 Vdc 9.0 Vdc ≤ V_{in} ≤ 21 Vdc	V_O	 — 5.65	 — 6.0	 — 6.35	 — 5.7	 — 6.0	 — 6.3	 5.7 —	 6.0 —	 6.3 —	Vdc
Line Regulation (T_J = +25°C, Note 2) 8.0 Vdc ≤ V_{in} ≤ 25 Vdc 9.0 Vdc ≤ V_{in} ≤ 13 Vdc	Reg_{line}	 — —	 3.0 2.0	 60 30	 — —	 9.0 3.0	 120 60	 — —	 9.0 3.0	 120 60	mV
Load Regulation (T_J = +25°C, Note 2) 5.0 mA ≤ I_O ≤ 1.5 A 250 mA ≤ I_O ≤ 750 mA	Reg_{load}	 — —	 27 9.0	 100 30	 — —	 43 16	 120 60	 — —	 43 16	 120 60	mV
Quiescent Current (T_J = +25°C)	I_B	—	3.2	6.0	—	4.3	8.0	—	4.3	8.0	mA
Quiescent Current Change 8.0 Vdc ≤ V_{in} ≤ 25 Vdc 9.0 Vdc ≤ V_{in} ≤ 25 Vdc 5.0 mA ≤ I_O ≤ 1.0 A	ΔI_B	 — — —	 — 0.3 0.04	 — 0.8 0.5	 — — —	 — — —	 — 1.3 0.5	 — — —	 — — —	 1.3 — 0.5	mA
Ripple Rejection 9.0 Vdc ≤ V_{in} ≤ 19 Vdc, f = 120 Hz	RR	65	73	—	—	65	—	—	65	—	dB
Dropout Voltage (I_O = 1.0 A, T_J = +25°C)	$V_{in}-V_O$	—	2.0	2.5	—	2.0	—	—	2.0	—	Vdc
Output Noise Voltage (T_A = +25°C) 10 Hz ≤ f ≤ 100 kHz	V_n	—	10	40	—	10	—	—	10	—	μV/V_O
Output Resistance f = 1.0 kHz	r_O	—	17	—	—	17	—	—	17	—	mΩ
Short-Circuit Current Limit (T_A = +25°C) V_{in} = 35 Vdc	I_{sc}	—	0.2	1.2	—	0.2	—	—	0.2	—	A
Peak Output Current (T_J = +25°C)	I_{max}	1.3	2.5	3.3	—	2.2	—	—	2.2	—	A
Average Temperature Coefficient of Output Voltage	TCV_O	—	±0.7	—	—	-0.8	—	—	-0.8	—	mV/°C

MC7806AC

ELECTRICAL CHARACTERISTICS (V_{in} = 11 V, I_O = 1.0 A, T_J = T_{low} to T_{high} [Note 1] unless otherwise noted).

Characteristics	Symbol	MC7806AC			Unit
		Min	Typ	Max	
Output Voltage (T_J = +25°C)	V_O	5.88	6.0	6.12	Vdc
Output Voltage (5.0 mA ≤ I_O ≤ 1.0 A, P_O ≤ 15 W) 8.6 Vdc ≤ V_{in} ≤ 21 Vdc	V_O	 5.76	 6.0	 6.24	Vdc
Line Regulation (Note 2) 8.6 Vdc ≤ V_{in} ≤ 25 Vdc, I_O = 500 mA 9.0 Vdc ≤ V_{in} ≤ 13 Vdc 9.0 Vdc ≤ V_{in} ≤ 13 Vdc, T_J = +25°C 8.3 Vdc ≤ V_{in} ≤ 21 Vdc, T_J = +25°C	Reg_{line}	 — — — —	 9.0 11 3.0 9.0	 60 60 30 60	mV
Load Regulation (Note 2) 5.0 mA ≤ I_O ≤ 1.5 A, T_J = +25°C 5.0 mA ≤ I_O ≤ 1.0 A 250 mA ≤ I_O ≤ 750 mA, T_J = +25°C 250 mA ≤ I_O ≤ 750 mA	Reg_{load}	 — — — —	 43 43 — 16	 100 100 — 50	mV
Quiescent Current T_J = +25°C	I_B	 —	 —	 6.0	mA
		—	4.3	6.0	
Quiescent Current Change 9.0 Vdc ≤ V_{in} ≤ 25 Vdc, I_O = 500 mA 8.6 Vdc ≤ V_{in} ≤ 21 Vdc, T_J = +25°C 5.0 mA ≤ I_O ≤ 1.0 A	ΔI_B	 — — —	 — — —	 0.8 0.8 0.5	mA
Ripple Rejection 9.0 Vdc ≤ V_{in} ≤ 19 Vdc, f = 120 Hz, T_J = +25°C 9.0 Vdc ≤ V_{in} ≤ 19 Vdc, f = 120 Hz, I_O = 500 mA	RR	 — —	 — 65	 — —	dB
Dropout Voltage (I_O = 1.0 A, T_J = +25°C)	$V_{in}-V_O$	—	2.0	—	Vdc
Output Noise Voltage (T_A = +25°C) 10 Hz ≤ f ≤ 100 kHz	V_n	—	10	—	μV/V_O
Output Resistance (f = 1.0 kHz)	r_O	—	17	—	mΩ
Short-Circuit Current Limit (T_A = +25°C) V_{in} = 35 Vdc	I_{sc}	—	0.2	—	A
Peak Output Current (T_J = +25°C)	I_{max}	—	2.2	—	A
Average Temperature Coefficient of Output Voltage	TCV_O	—	-0.8	—	mV/°C

NOTES: 1. T_{low} = −55°C for MC78XX; T_{high} = +150°C for MC78XX
= 0° for MC78XXC, AC; = +125°C for MC78XXC, AC, B
= −40°C for MC78XXB

2. Load and line regulation are specified at constant junction temperature. Changes in V_O due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

MC7808, B, C

ELECTRICAL CHARACTERISTICS (V_{in} = 14 V, I_O = 500 mA, T_J = T_{low} to T_{high} [Note 1] unless otherwise noted).

Characteristic	Symbol	MC7808			MC7808B			MC7808C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Output Voltage (T_J = +25°C)	V_O	7.7	8.0	8.3	7.7	8.0	8.3	7.7	8.0	8.3	Vdc
Output Voltage (5.0 mA ≤ I_O ≤ 1.0 A, P_O ≤ 15 W) 10.5 Vdc ≤ V_{in} ≤ 23 Vdc 11.5 Vdc ≤ V_{in} ≤ 23 Vdc	V_O	 — 7.6	 — 8.0	 — 8.4	 — 7.6	 — 8.0	 — 8.4	 7.6 —	 8.0 —	 8.4 —	Vdc
Line Regulation (T_J = +25°C, Note 2) 10.5 Vdc ≤ V_{in} ≤ 25 Vdc 11 Vdc ≤ V_{in} ≤ 17 Vdc	Reg_{line}	 — —	 3.0 2.0	 80 40	 — —	 12 5.0	 160 80	 — —	 12 5.0	 160 80	mV
Load Regulation (T_J = +25°C, Note 2) 5.0 mA ≤ I_O ≤ 1.5 A 250 mA ≤ I_O ≤ 750 mA	Reg_{load}	 — —	 28 9.0	 100 40	 — —	 45 16	 160 80	 — —	 45 16	 160 80	mV
Quiescent Current (T_J = +25°C)	I_B	—	3.2	6.0	—	4.3	8.0	—	4.3	8.0	mA
Quiescent Current Change 10.5 Vdc ≤ V_{in} ≤ 25 Vdc 11.5 Vdc ≤ V_{in} ≤ 25 Vdc 5.0 mA ≤ I_O ≤ 1.0 A	ΔI_B	 — — —	 — 0.3 0.04	 — 0.8 0.5	 — — —	 — — —	 — 1.0 0.5	 — — —	 — — —	 1.0 — 0.5	mA
Ripple Rejection 11.5 Vdc ≤ V_{in} ≤ 21.5 Vdc, f = 120 Hz	RR	62	70	—	—	62	—	—	62	—	dB
Dropout Voltage (I_O = 1.0 A, T_J = +25°C)	V_{in}–V_O	—	2.0	2.5	—	2.0	—	—	2.0	—	Vdc
Output Noise Voltage (T_A = +25°C) 10 Hz ≤ f ≤ 100 kHz	V_n	—	10	40	—	10	—	—	10	—	μV/V_O
Output Resistance f = 1.0 kHz	r_O	—	18	—	—	18	—	—	18	—	mΩ
Short-Circuit Current Limit (T_A = +25°C) V_{in} = 35 Vdc	I_{sc}	—	0.2	1.2	—	0.2	—	—	0.2	—	A
Peak Output Current (T_J = +25°C)	I_{max}	1.3	2.5	3.3	—	2.2	—	—	2.2	—	A
Average Temperature Coefficient of Output Voltage	TCV_O	—	±1.0	—	—	−0.8	—	—	−0.8	—	mV/°C

MC7808AC

ELECTRICAL CHARACTERISTICS (V_{in} = 14 V, I_O = 1.0 A, T_J = T_{low} to T_{high} [Note 1] unless otherwise noted).

Characteristics	Symbol	MC7808AC			Unit
		Min	Typ	Max	
Output Voltage (T_J = +25°C)	V_O	7.84	8.0	8.16	Vdc
Output Voltage (5.0 mA ≤ I_O ≤ 1.0 A, P_O ≤ 15 W) 10.6 Vdc ≤ V_{in} ≤ 23 Vdc	V_O	 7.7	 8.0	 8.3	Vdc
Line Regulation (Note 2) 10.6 Vdc ≤ V_{in} ≤ 25 Vdc, I_O = 500 mA 11 Vdc ≤ V_{in} ≤ 17 Vdc 11 Vdc ≤ V_{in} ≤ 17 Vdc, T_J = +25°C 10.4 Vdc ≤ V_{in} ≤ 23 Vdc, T_J = +25°C	Reg_{line}	 — — — —	 12 15 5.0 12	 80 80 40 80	mV
Load Regulation (Note 2) 5.0 mA ≤ I_O ≤ 1.5 A, T_J = +25°C 5.0 mA ≤ I_O ≤ 1.0 A 250 mA ≤ I_O ≤ 750 mA, T_J = +25°C 250 mA ≤ I_O ≤ 750 mA	Reg_{load}	 — — — —	 45 45 — 16	 100 100 — 50	mV
Quiescent Current T_J = +25°C	I_B	 —	 —	 6.0 6.0	mA
Quiescent Current Change 11 Vdc ≤ V_{in} ≤ 25 Vdc, I_O = 500 mA 10.6 Vdc ≤ V_{in} ≤ 23 Vdc, T_J = +25°C 5.0 mA ≤ I_O ≤ 1.0 A	ΔI_B	 — — —	 — — —	 0.8 0.8 0.5	mA
Ripple Rejection 11.5 Vdc ≤ V_{in} ≤ 21.5 Vdc, f = 120 Hz, T_J = +25°C 11.5 Vdc ≤ V_{in} ≤ 21.5 Vdc, f = 120 Hz, I_O = 500 mA	RR	 — —	 — 62	 — —	dB
Dropout Voltage (I_O = 1.0 A, T_J = +25°C)	V_{in}–V_O	—	2.0	—	Vdc
Output Noise Voltage (T_A = +25°C) 10 Hz ≤ f ≤ 100 kHz	V_n	—	10	—	μV/V_O
Output Resistance (f = 1.0 kHz)	r_O	—	18	—	mΩ
Short-Circuit Current Limit (T_A = +25°C) V_{in} = 35 Vdc	I_{sc}	—	0.2	—	A
Peak Output Current (T_J = +25°C)	I_{max}	—	2.2	—	A
Average Temperature Coefficient of Output Voltage	TCV_O	—	−0.8	—	mV/°C

NOTES: 1. T_{low} = −55°C for MC78XX; T_{high} = +150°C for MC78XX
= 0° for MC78XXC, AC; = +125°C for MC78XXC, AC, B
= −40°C for MC78XXB

2. Load and line regulation are specified at constant junction temperature. Changes in V_O due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

MC7809CT

ELECTRICAL CHARACTERISTICS (V_{in} = 15 V, I_O = 500 mA, T_J = 0°C to +125°C unless otherwise noted).

Characteristic	Symbol	MC7809CT			Unit
		Min	Typ	Max	
Output Voltage (T_J = +25°C)	V_O	8.65	9.0	9.35	Vdc
Output Voltage (5.0 mA ≤ I_O ≤ 1.0 A, P_O ≤ 15 W) 11.5 Vdc ≤ V_{in} ≤ 24 Vdc	V_O	8.55	9.0	9.45	Vdc
Line Regulation (T_J = +25°C, Note 1) 11.5 Vdc ≤ V_{in} ≤ 26 Vdc 11.5 Vdc ≤ V_{in} ≤ 17 Vdc	Reg_{line}	 — —	 12 5.0	 50 25	mV
Load Regulation (T_J = +25°C, Note 1) 5.0 mA ≤ I_O ≤ 1.5 A 250 mA ≤ I_O ≤ 750 mA	Reg_{load}	 — —	 35 12	 50 25	mV
Quiescent Current (T_J = +25°C)	I_B	—	4.3	8.0	mA
Quiescent Current Change 11.5 Vdc ≤ V_{in} ≤ 26 Vdc 5.0 mA ≤ I_O ≤ 1.0 A	ΔI_B	 — —	 — —	 1.0 0.5	mA
Ripple Rejection 11.5 Vdc ≤ V_{in} ≤ 21.5 Vdc, f = 120 Hz	RR	—	61	—	dB
Dropout Voltage (I_O = 1.0 A, T_J = +25°C)	$V_{in} - V_O$	—	2.0	—	Vdc
Output Noise Voltage (T_A = +25°C) 10 Hz ≤ f ≤ 100 kHz	V_n	—	10	—	$\mu V/V_O$
Output Resistance f = 1.0 kHz	r_O	—	18	—	mΩ
Short-Circuit Current Limit (T_A = +25°C) V_{in} = 35 Vdc	I_{sc}	—	0.2	—	A
Peak Output Current (T_J = +25°C)	I_{max}	—	2.2	—	A
Average Temperature Coefficient of Output Voltage	TCV_O	—	-1.0	—	mV/°C

NOTE 1: Load and line regulation are specified at constant junction temperature. Changes in V_O due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

MC7812, B, C

ELECTRICAL CHARACTERISTICS (V_{in} = 19 V, I_O = 500 mA, T_J = T_{low} to T_{high} [Note 1] unless otherwise noted)

Characteristic	Symbol	MC7812			MC7812B			MC7812C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Output Voltage (T_J = +25°C)	V_O	11.5	12	12.5	11.5	12	12.5	11.5	12	12.5	Vdc
Output Voltage (5.0 mA ≤ I_O ≤ 1.0 A, P_O ≤ 15 W) 14.5 Vdc ≤ V_{in} ≤ 27 Vdc 15.5 Vdc ≤ V_{in} ≤ 27 Vdc	V_O	— 11.4	— 12	— 12.6	— 11.4	— 12	— 12.6	11.4 —	12 —	12.6 —	Vdc
Line Regulation (T_J = +25°C, Note 2) 14.5 Vdc ≤ V_{in} ≤ 30 Vdc 16 Vdc ≤ V_{in} ≤ 22 Vdc	Reg_{line}	— —	5.0 3.0	120 60	— —	13 6.0	240 120	— —	13 6.0	240 120	mV
Load Regulation (T_J = +25°C, Note 2) 5.0 mA ≤ I_O ≤ 1.5 A 250 mA ≤ I_O ≤ 750 mA	Reg_{load}	— —	30 10	120 60	— —	46 17	240 120	— —	46 17	240 120	mV
Quiescent Current (T_J = +25°C)	I_B	—	3.4	6.0	—	4.4	8.0	—	4.4	8.0	mA
Quiescent Current Change 14.5 Vdc ≤ V_{in} ≤ 30 Vdc 15 Vdc ≤ V_{in} ≤ 30 Vdc 5.0 mA ≤ I_O ≤ 1.0 A	ΔI_B	— — —	— 0.3 0.04	— 0.8 0.5	— — —	— — —	— 1.0 0.5	— — —	— — —	1.0 — 0.5	mA
Ripple Rejection 15 Vdc ≤ V_{in} ≤ 25 Vdc, f = 120 Hz	RR	61	68	—	—	60	—	—	60	—	dB
Dropout Voltage (I_O = 1.0 A, T_J = +25°C)	V_{in} - V_O	—	2.0	2.5	—	2.0	—	—	2.0	—	Vdc
Output Noise Voltage (T_A = +25°C) 10 Hz ≤ f ≤ 100 kHz	V_n	—	10	40	—	10	—	—	10	—	μV/V_O
Output Resistance f = 1.0 kHz	r_O	—	18	—	—	18	—	—	18	—	mΩ
Short-Circuit Current Limit (T_A = +25°C) V_{in} = 35 Vdc	I_{sc}	—	0.2	1.2	—	0.2	—	—	0.2	—	A
Peak Output Current (T_J = +25°C)	I_{max}	1.3	2.5	3.3	—	2.2	—	—	2.2	—	A
Average Temperature Coefficient of Output Voltage	TCV_O	—	±1.5	—	—	-1.0	—	—	-1.0	—	mV/°C

MC7812A, AC

ELECTRICAL CHARACTERISTICS (V_{in} = 19 V, I_O = 1.0 A, T_J = T_{low} to T_{high} [Note 1] unless otherwise noted)

Characteristics	Symbol	MC7812A			MC7812AC			Unit
		Min	Typ	Max	Min	Typ	Max	
Output Voltage (T_J = +25°C)	V_O	11.75	12	12.25	11.75	12	12.25	Vdc
Output Voltage (5.0 mA ≤ I_O ≤ 1.0 A, P_O ≤ 15 W) 14.8 Vdc ≤ V_{in} ≤ 27 Vdc	V_O	11.5	12	12.5	11.5	12	12.5	Vdc
Line Regulation (Note 2) 14.8 Vdc ≤ V_{in} ≤ 30 Vdc, I_O = 500 mA 16 Vdc ≤ V_{in} ≤ 22 Vdc 16 Vdc ≤ V_{in} ≤ 22 Vdc, T_J = +25°C 14.5 Vdc ≤ V_{in} ≤ 27 Vdc, T_J = +25°C	Reg_{line}	— — — —	5.0 8.0 3.0 5.0	18 30 9.0 18	— — — —	13 16 6.0 13	120 120 60 120	mV
Load Regulation (Note 2) 5.0 mA ≤ I_O ≤ 1.5 A, T_J = +25°C 5.0 mA ≤ I_O ≤ 1.0 A 250 mA ≤ I_O ≤ 750mA, T_J = +25°C 250 mA ≤ I_O ≤ 750 mA	Reg_{load}	— — — —	2.0 2.0 1.0 1.0	25 25 15 25	— — — —	46 46 — 17	100 100 — 50	mV
Quiescent Current T_J = +25°C	I_B	— —	— 3.4	5.0 4.0	— —	— 4.4	6.0 6.0	mA
Quiescent Current Change 15 Vdc ≤ V_{in} ≤ 30 Vdc, I_O = 500 mA 14.8 Vdc ≤ V_{in} ≤ 27 Vdc, T_J = +25°C 5.0 mA ≤ I_O ≤ 1.0 A	ΔI_B	— —	0.3 0.2 0.04	0.5 0.5 0.2	— —	— —	0.8 0.8 0.5	mA
Ripple Rejection 15 Vdc ≤ V_{in} ≤ 25 Vdc, f = 120 Hz, T_J = +25°C 15 Vdc ≤ V_{in} ≤ 25 Vdc, f = 120 Hz, I_O = 500 mA	RR	61 61	68 68	— —	— —	— 60	— —	dB
Dropout Voltage (I_O = 1.0 A, T_J = +25°C)	V_{in} - V_O	—	2.0	2.5	—	2.0	—	Vdc
Output Noise Voltage (T_A = +25°C) 10 Hz ≤ f ≤ 100 kHz	V_n	—	10	40	—	10	—	μV/V_O
Output Resistance (f = 1.0 kHz)	r_O	—	2.0	—	—	18	—	mΩ
Short-Circuit Current Limit (T_A = +25°C) V_{in} = 35 Vdc	I_{sc}	—	0.2	1.2	—	0.2	—	A
Peak Output Current (T_J = +25°C)	I_{max}	1.3	2.5	3.3	—	2.2	—	A
Average Temperature Coefficient of Output Voltage	TCV_O	—	±1.5	—	—	-1.0	—	mV/°C

NOTES: 1. T_{low} = -55°C for MC78XX, A
= 0° for MC78XXC, AC
= -40°C for MC78XXB
T_{high} = +150°C for MC78XX, A
= +125°C for MC78XXC, AC, B

2. Load and line regulation are specified at constant junction temperature. Changes in V_O due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

MC7815, B, C

ELECTRICAL CHARACTERISTICS (V_{in} = 23 V, I_O = 500 mA, T_J = T_{low} to T_{high} [Note 1] unless otherwise noted).

Characteristic	Symbol	MC7815			MC7815B			MC7815C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Output Voltage (T_J = +25°C)	V_O	14.4	15	15.6	14.4	15	15.6	14.4	15	15.6	Vdc
Output Voltage (5.0 mA ≤ I_O ≤ 1.0 A, P_O ≤ 15 W) 17.5 Vdc ≤ V_{in} ≤ 30 Vdc 18.5 Vdc ≤ V_{in} ≤ 30 Vdc	V_O	— 14.25	— 15	— 15.75	— 14.25	— 15	— 15.75	14.25 —	15 —	15.75 —	Vdc
Line Regulation (T_J = +25°C, Note 2) 17.5 Vdc ≤ V_{in} ≤ 30 Vdc 20 Vdc ≤ V_{in} ≤ 26 Vdc	Reg_{line}	— —	6.0 3.0	150 75	— —	13 6.0	300 150	— —	13 6.0	300 150	mV
Load Regulation (T_J = +25°C, Note 2) 5.0 mA ≤ I_O ≤ 1.5 A 250 mA ≤ I_O ≤ 750 mA	Reg_{load}	— —	32 10	150 75	— —	52 20	300 150	— —	52 20	300 150	mV
Quiescent Current (T_J = +25°C)	I_B	—	3.4	6.0	—	4.4	8.0	—	4.4	8.0	mA
Quiescent Current Change 17.5 Vdc ≤ V_{in} ≤ 30 Vdc 18.5 Vdc ≤ V_{in} ≤ 30 Vdc 5.0 mA ≤ I_O ≤ 1.0 A	ΔI_B	— — —	— 0.3 0.04	— 0.8 0.5	— — —	— — —	— 1.0 0.5	— — —	— — —	1.0 — 0.5	mA
Ripple Rejection 18.5 Vdc ≤ V_{in} ≤ 28.5 Vdc, f = 120 Hz	RR	60	66	—	—	58	—	—	58	—	dB
Dropout Voltage (I_O = 1.0 A, T_J = +25°C)	$V_{in} - V_O$	—	2.0	2.5	—	2.0	—	—	2.0	—	Vdc
Output Noise Voltage (T_A = +25°C) 10 Hz ≤ f ≤ 100 kHz	V_n	—	10	40	—	10	—	—	10	—	$\mu V / V_O$
Output Resistance f = 1.0 kHz	r_O	—	19	—	—	19	—	—	19	—	mΩ
Short-Circuit Current Limit (T_A = +25°C) V_{in} = 35 Vdc	I_{sc}	—	0.2	1.2	—	0.2	—	—	0.2	—	A
Peak Output Current (T_J = +25°C)	I_{max}	1.3	2.5	3.3	—	2.2	—	—	2.2	—	A
Average Temperature Coefficient of Output Voltage	TCV_O	—	±1.8	—	—	-1.0	—	—	-1.0	—	mV/°C

MC7815A, AC

ELECTRICAL CHARACTERISTICS (V_{in} = 23 V, I_O = 1.0 A, T_J = T_{low} to T_{high} [Note 1] unless otherwise noted)

Characteristics	Symbol	MC7815A			MC7815AC			Unit
		Min	Typ	Max	Min	Typ	Max	
Output Voltage (T_J = +25°C)	V_O	14.7	15	15.3	14.7	15	15.3	Vdc
Output Voltage (5.0 mA ≤ I_O ≤ 1.0 A, P_O ≤ 15 W) 17.9 Vdc ≤ V_{in} ≤ 30 Vdc	V_O	14.4	15	15.6	14.4	15	15.6	Vdc
Line Regulation (Note 2) 17.9 Vdc ≤ V_{in} ≤ 30 Vdc, I_O = 500 mA 20 Vdc ≤ V_{in} ≤ 26 Vdc 20 Vdc ≤ V_{in} ≤ 26 Vdc, T_J = +25°C 17.5 Vdc ≤ V_{in} ≤ 30 Vdc, T_J = +25°C	Reg_{line}	— — — —	6.0 6.0 3.0 6.0	22 22 10 22	— — — —	13 16 6.0 13	150 150 75 150	mV
Load Regulation (Note 2) 5.0 mA ≤ I_O ≤ 1.5 A, T_J = +25°C 5.0 mA ≤ I_O ≤ 1.0 A 250 mA ≤ I_O ≤ 750mA, T_J = +25°C 250 mA ≤ I_O ≤ 750 mA	Reg_{load}	— — — —	2.0 2.0 1.0 1.0	25 25 15 25	— — — —	52 52 — 20	100 100 — 50	mV
Quiescent Current T_J = +25°C	I_B	— —	— 3.4	5.5 4.5	— —	— 4.4	6.0 6.0	mA
Quiescent Current Change 17.5 Vdc ≤ V_{in} ≤ 30 Vdc, I_O = 500 mA 17.5 Vdc ≤ V_{in} ≤ 30 Vdc, T_J = +25°C 5.0 mA ≤ I_O ≤ 1.0 A	ΔI_B	— — —	0.3 0.2 0.04	0.5 0.5 0.2	— — —	— — —	0.8 0.8 0.5	mA
Ripple Rejection 18.5 Vdc ≤ V_{in} ≤ 28.5 Vdc, f = 120 Hz, T_J = +25°C 18.5 Vdc ≤ V_{in} ≤ 28.5 Vdc, f = 120 Hz, I_O = 500 mA	RR	60 60	66 66	— —	— —	— 58	— —	dB
Dropout Voltage (I_O = 1.0 A, T_J = +25°C)	$V_{in} - V_O$	—	2.0	2.5	—	2.0	—	Vdc
Output Noise Voltage (T_A = +25°C) 10 Hz ≤ f ≤ 100 kHz	V_n	—	10	40	—	10	—	$\mu V / V_O$
Output Resistance (f = 1.0 kHz)	r_O	—	2.0	—	—	19	—	mΩ
Short-Circuit Current Limit (T_A = +25°C) V_{in} = 35 Vdc	I_{sc}	—	0.2	1.2	—	0.2	—	A
Peak Output Current (T_J = +25°C)	I_{max}	1.3	2.5	3.3	—	2.2	—	A
Average Temperature Coefficient of Output Voltage	TCV_O	—	±1.8	—	—	-1.0	—	mV/°C

NOTES: 1. T_{low} = -55°C for MC78XX, A
= 0° for MC78XXC, AC
= -40°C for MC78XXB
T_{high} = +150°C for MC78XX, A
= +125°C for MC78XXC, AC, B

2. Load and line regulation are specified at constant junction temperature. Changes in V_O due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

MC7818, B, C

ELECTRICAL CHARACTERISTICS (V_{in} = 27 V, I_O = 500 mA, T_J = T_{low} to T_{high} [Note 1] unless otherwise noted).

Characteristic	Symbol	MC7818			MC7818B			MC7818C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Output Voltage (T_J = +25°C)	V_O	17.3	18	18.7	17.3	18	18.7	17.3	18	18.7	Vdc
Output Voltage (5.0 mA ≤ I_O ≤ 1.0 A, P_O ≤ 15 W) 21 Vdc ≤ V_{in} ≤ 33 Vdc 22 Vdc ≤ V_{in} ≤ 33 Vdc	V_O	 — 17.1	 — 18	 — 18.9	 — 17.1	 — 18	 — 18.9	 17.1 —	 18 —	 18.9 —	Vdc
Line Regulation (T_J = +25°C, Note 2) 21 Vdc ≤ V_{in} ≤ 33 Vdc 24 Vdc ≤ V_{in} ≤ 30 Vdc	Reg_{line}	 — —	 7.0 4.0	 180 90	 — —	 25 10	 360 180	 — —	 25 10	 360 180	mV
Load Regulation (T_J = +25°C, Note 2) 5.0 mA ≤ I_O ≤ 1.5 A 250 mA ≤ I_O ≤ 750 mA	Reg_{load}	 — —	 35 12	 180 90	 — —	 55 22	 360 180	 — —	 55 22	 360 180	mV
Quiescent Current (T_J = +25°C)	I_B	—	3.5	6.0	—	4.5	8.0	—	4.5	8.0	mA
Quiescent Current Change 21 Vdc ≤ V_{in} ≤ 33 Vdc 22 Vdc ≤ V_{in} ≤ 33 Vdc 5.0 mA ≤ I_O ≤ 1.0 A	ΔI_B	 — — —	 — 0.3 0.04	 — 0.8 0.5	 — — —	 — — —	 — 1.0 0.5	 — — —	 — — —	 1.0 — 0.5	mA
Ripple Rejection 22 Vdc ≤ V_{in} ≤ 33 Vdc, f = 120 Hz	RR	59	65	—	—	57	—	—	57	—	dB
Dropout Voltage (I_O = 1.0 A, T_J = +25°C)	V_{in}–V_O	—	2.0	2.5	—	2.0	—	—	2.0	—	Vdc
Output Noise Voltage (T_A = +25°C) 10 Hz ≤ f ≤ 100 kHz	V_n	—	10	40	—	10	—	—	10	—	μV/V_O
Output Resistance f = 1.0 kHz	r_O	—	19	—	—	19	—	—	19	—	mΩ
Short-Circuit Current Limit (T_A = +25°C) V_{in} = 35 Vdc	I_{sc}	—	0.2	1.2	—	0.2	—	—	0.2	—	A
Peak Output Current (T_J = +25°C)	I_{max}	1.3	2.5	3.3	—	2.2	—	—	2.2	—	A
Average Temperature Coefficient of Output Voltage	TCV_O	—	±2.3	—	—	−1.0	—	—	−1.0	—	mV/°C

MC7818AC

ELECTRICAL CHARACTERISTICS (V_{in} = 27 V, I_O = 1.0 A, T_J = T_{low} to T_{high} [Note 1] unless otherwise noted).

Characteristics	Symbol	MC7818AC			Unit
		Min	Typ	Max	
Output Voltage (T_J = +25°C)	V_O	17.64	18	18.36	Vdc
Output Voltage (5.0 mA ≤ I_O ≤ 1.0 A, P_O ≤ 15 W) 21 Vdc ≤ V_{in} ≤ 33 Vdc	V_O	 17.3	 18	 18.7	Vdc
Line Regulation (Note 2) 21 Vdc ≤ V_{in} ≤ 33 Vdc, I_O = 500 mA 24 Vdc ≤ V_{in} ≤ 30 Vdc 24 Vdc ≤ V_{in} ≤ 30 Vdc, T_J = +25°C 20.6 Vdc ≤ V_{in} ≤ 33 Vdc, T_J = +25°C	Reg_{line}	 — — — —	 25 28 10 25	 180 180 90 180	mV
Load Regulation (Note 2) 5.0 mA ≤ I_O ≤ 1.5 A, T_J = +25°C 5.0 mA ≤ I_O ≤ 1.0 A 250 mA ≤ I_O ≤ 750 mA, T_J = +25°C 250 mA ≤ I_O ≤ 750 mA	Reg_{load}	 — — — —	 55 55 — 22	 100 100 — 50	mV
Quiescent Current T_J = +25°C	I_B	 —	 —	 6.0	mA
		—	4.5	6.0	
Quiescent Current Change 21 Vdc ≤ V_{in} ≤ 33 Vdc, I_O = 500 mA 21 Vdc ≤ V_{in} ≤ 33 Vdc, T_J = +25°C 5.0 mA ≤ I_O ≤ 1.0 A	ΔI_B	 — — —	 — — —	 0.8 0.8 0.5	mA
Ripple Rejection 22 Vdc ≤ V_{in} ≤ 32 Vdc, f = 120 Hz, T_J = +25°C 22 Vdc ≤ V_{in} ≤ 32 Vdc, f = 120 Hz, I_O = 500 mA	RR	 — —	 — 57	 — —	dB
Dropout Voltage (I_O = 1.0 A, T_J = +25°C)	V_{in}–V_O	—	2.0	—	Vdc
Output Noise Voltage (T_A = +25°C) 10 Hz ≤ f ≤ 100 kHz	V_n	—	10	—	μV/V_O
Output Resistance (f = 1.0 kHz)	r_O	—	19	—	mΩ
Short-Circuit Current Limit (T_A = +25°C) V_{in} = 35 Vdc	I_{sc}	—	0.2	—	A
Peak Output Current (T_J = +25°C)	I_{max}	—	2.2	—	A
Average Temperature Coefficient of Output Voltage	TCV_O	—	−1.0	—	mV/°C

NOTES: 1. T_{low} = −55°C for MC78XX
= 0° for MC78XXC, AC
= −40°C for MC78XXB
T_{high} = +150°C for MC78XX
= +125°C for MC78XXC, AC, B

2. Load and line regulation are specified at constant junction temperature. Changes in V_O due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

MC7824, B, C

ELECTRICAL CHARACTERISTICS (V_{in} = 33 V, I_O = 500 mA, T_J = T_{low} to T_{high} [Note 1] unless otherwise noted).

Characteristic	Symbol	MC7824			MC7824B			MC7824C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Output Voltage (T_J = +25°C)	V_O	23	24	25	23	24	25	23	24	25	Vdc
Output Voltage (5.0 mA ≤ I_O ≤ 1.0 A, P_O ≤ 15 W) 27 Vdc ≤ V_{in} ≤ 38 Vdc 28 Vdc ≤ V_{in} ≤ 38 Vdc	V_O	 — 22.8	 — 24	 — 25.2	 — 22.8	 — 24	 — 25.2	 22.8 —	 24 —	 25.2 —	Vdc
Line Regulation (T_J = +25°C, Note 2) 27 Vdc ≤ V_{in} ≤ 38 Vdc 30 Vdc ≤ V_{in} ≤ 36 Vdc	Reg_{line}	 — —	 10 5.0	 240 120	 — —	 31 14	 480 240	 — —	 31 14	 480 240	mV
Load Regulation (T_J = +25°C, Note 2) 5.0 mA ≤ I_O ≤ 1.5 A 250 mA ≤ I_O ≤ 750 mA	Reg_{load}	 — —	 40 15	 240 120	 — —	 60 25	 480 240	 — —	 60 25	 480 240	mV
Quiescent Current (T_J = +25°C)	I_B	—	3.6	6.0	—	4.6	8.0	—	4.6	8.0	mA
Quiescent Current Change 27 Vdc ≤ V_{in} ≤ 38 Vdc 28 Vdc ≤ V_{in} ≤ 38 Vdc 5.0 mA ≤ I_O ≤ 1.0 A	ΔI_B	 — — —	 — 0.3 0.04	 — 0.8 0.5	 — — —	 — — —	 — 1.0 0.5	 — — —	 — — —	 1.0 — 0.5	mA
Ripple Rejection 28 Vdc ≤ V_{in} ≤ 38 Vdc, f = 120 Hz	RR	56	62	—	—	54	—	—	54	—	dB
Dropout Voltage (I_O = 1.0 A, T_J = +25°C)	$V_{in}-V_O$	—	2.0	2.5	—	2.0	—	—	2.0	—	Vdc
Output Noise Voltage (T_A = +25°C) 10 Hz ≤ f ≤ 100 kHz	V_n	—	10	40	—	10	—	—	10	—	μV/V_O
Output Resistance f = 1.0 kHz	r_O	—	20	—	—	20	—	—	20	—	mΩ
Short-Circuit Current Limit (T_A = +25°C) V_{in} = 35 Vdc	I_{sc}	—	0.2	1.2	—	0.2	—	—	0.2	—	A
Peak Output Current (T_J = +25°C)	I_{max}	1.3	2.5	3.3	—	2.2	—	—	2.2	—	A
Average Temperature Coefficient of Output Voltage	TCV_O	—	±3.0	—	—	-1.5	—	—	-1.5	—	mV/°C

MC7824AC

ELECTRICAL CHARACTERISTICS (V_{in} = 33 V, I_O = 1.0 A, T_J = T_{low} to T_{high} [Note 1] unless otherwise noted).

Characteristics	Symbol	MC7824AC			Unit
		Min	Typ	Max	
Output Voltage (T_J = +25°C)	V_O	23.5	24	24.5	Vdc
Output Voltage (5.0 mA ≤ I_O ≤ 1.0 A, P_O ≤ 15 W) 27.3 Vdc ≤ V_{in} ≤ 38 Vdc	V_O	 23	 24	 25	Vdc
Line Regulation (Note 2) 27 Vdc ≤ V_{in} ≤ 38 Vdc, I_O = 500 mA 30 Vdc ≤ V_{in} ≤ 36 Vdc 30 Vdc ≤ V_{in} ≤ 36 Vdc, T_J = +25°C 26.7 Vdc ≤ V_{in} ≤ 38 Vdc, T_J = +25°C	Reg_{line}	 — — — —	 31 35 14 31	 240 240 120 240	mV
Load Regulation (Note 2) 5.0 mA ≤ I_O ≤ 1.5 A, T_J = +25°C 5.0 mA ≤ I_O ≤ 1.0 A 250 mA ≤ I_O ≤ 750 mA, T_J = +25°C 250 mA ≤ I_O ≤ 750 mA	Reg_{load}	 — — — —	 60 60 — 25	 100 100 — 50	mV
Quiescent Current T_J = +25°C	I_B	— —	— 4.6	6.0 6.0	mA
Quiescent Current Change 27.3 Vdc ≤ V_{in} ≤ 38 Vdc, I_O = 500 mA 27.3 Vdc ≤ V_{in} ≤ 38 Vdc, T_J = +25°C 5.0 mA ≤ I_O ≤ 1.0 A	ΔI_B	 — — —	 — — —	 0.8 0.8 0.5	mA
Ripple Rejection 28 Vdc ≤ V_{in} ≤ 38 Vdc, f = 120 Hz, T_J = +25°C 28 Vdc ≤ V_{in} ≤ 38 Vdc, f = 120 Hz, I_O = 500 mA	RR	 — —	 — 54	 — —	dB
Dropout Voltage (I_O = 1.0 A, T_J = +25°C)	$V_{in}-V_O$	—	2.0	—	Vdc
Output Noise Voltage (T_A = +25°C) 10 Hz ≤ f ≤ 100 kHz	V_n	—	10	—	μV/V_O
Output Resistance (f = 1.0 kHz)	r_O	—	20	—	mΩ
Short-Circuit Current Limit (T_A = +25°C) V_{in} = 35 Vdc	I_{sc}	—	0.2	—	A
Peak Output Current (T_J = +25°C)	I_{max}	—	2.2	—	A
Average Temperature Coefficient of Output Voltage	TCV_O	—	-1.5	—	mV/°C

NOTES: 1. T_{low} = −55°C for MC78XX
= 0° for MC78XXC, AC
= −40°C for MC78XXB
T_{high} = +150°C for MC78XX
= +125°C for MC78XXC, AC, B

2. Load and line regulation are specified at constant junction temperature. Changes in V_O due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

TYPICAL CHARACTERISTICS
(T_A = +25°C unless otherwise noted.)

FIGURE 1 – WORST CASE POWER DISSIPATION versus AMBIENT TEMPERATURE (Case 221A)

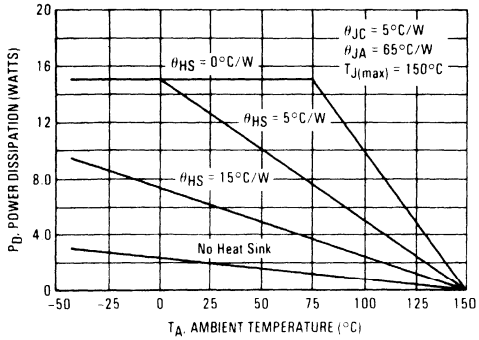


FIGURE 2 – WORST CASE POWER DISSIPATION versus AMBIENT TEMPERATURE (Case 1)

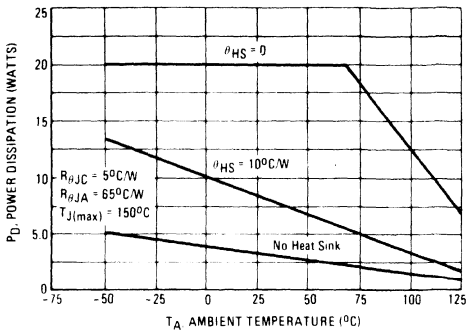


FIGURE 3 – INPUT OUTPUT DIFFERENTIAL AS A FUNCTION OF JUNCTION TEMPERATURE (MC78XXC, AC, B)

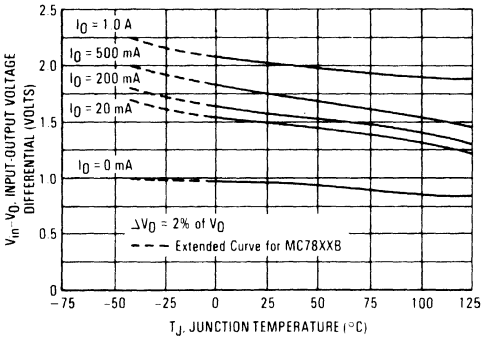


FIGURE 4 – INPUT OUTPUT DIFFERENTIAL AS A FUNCTION OF JUNCTION TEMPERATURE (MC78XX, A)

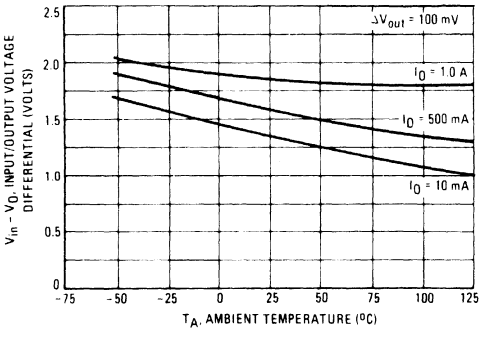


FIGURE 5 – PEAK OUTPUT CURRENT AS A FUNCTION OF INPUT-OUTPUT DIFFERENTIAL VOLTAGE (MC78XXC, AC, B)

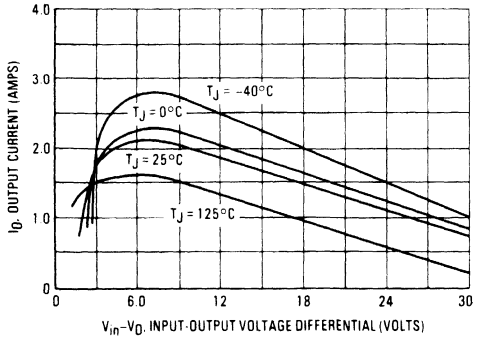
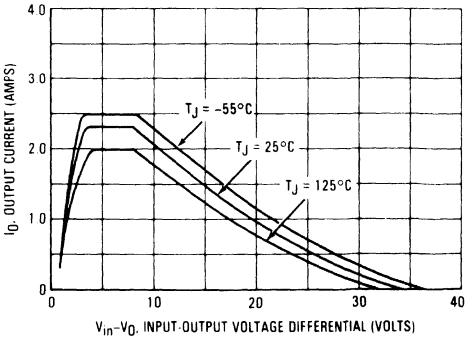


FIGURE 6 – PEAK OUTPUT CURRENT AS A FUNCTION OF INPUT-OUTPUT DIFFERENTIAL VOLTAGE (MC78XX, A)



TYPICAL CHARACTERISTICS (continued)
(T_A = 25°C unless otherwise noted.)

FIGURE 7 – RIPPLE REJECTION AS A FUNCTION OF OUTPUT VOLTAGES (MC78XXC, AC)

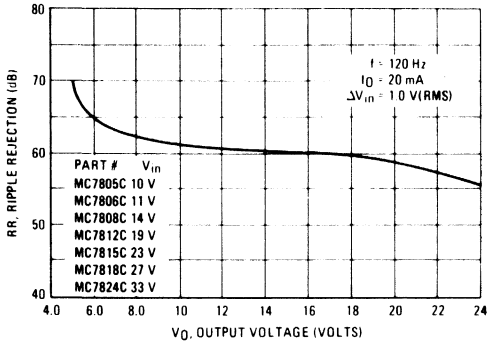


FIGURE 8 – RIPPLE REJECTION AS A FUNCTION OF FREQUENCY (MC78XXC, AC, A)

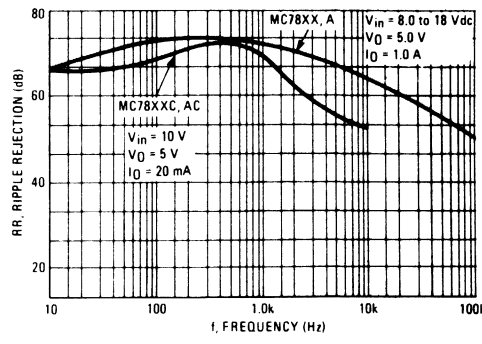


FIGURE 9 – OUTPUT VOLTAGE AS A FUNCTION OF JUNCTION TEMPERATURE (MC78XXC, AC, B)

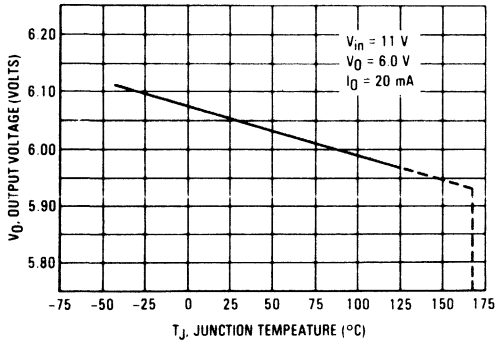


FIGURE 10 – OUTPUT IMPEDANCE AS A FUNCTION OF OUTPUT VOLTAGE (MC78XXC, AC)

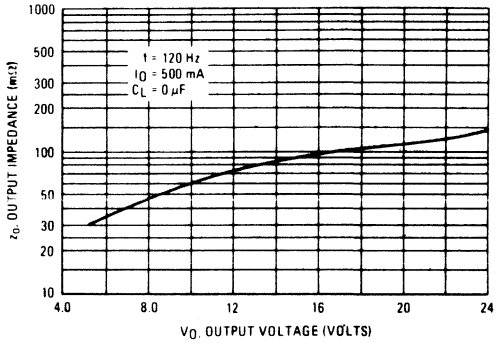


FIGURE 11 – QUIESCENT CURRENT AS A FUNCTION OF TEMPERATURE (MC78XXC, AC, B)

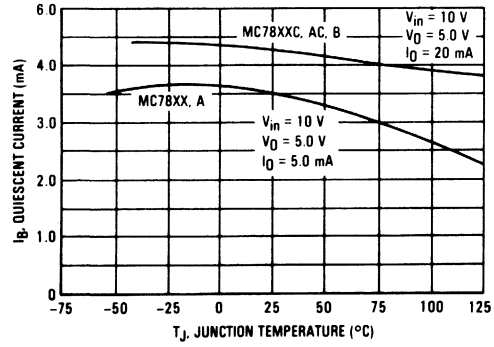
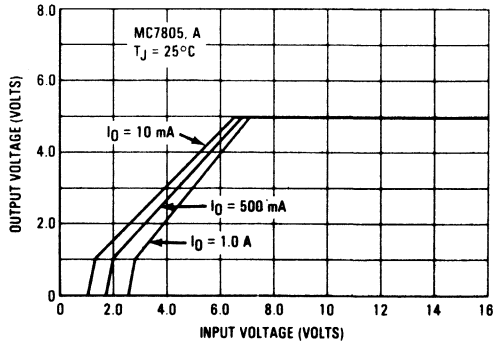


FIGURE 12 – DROPOUT CHARACTERISTICS (MC78XX, A)



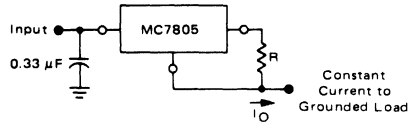
APPLICATIONS INFORMATION

Design Considerations

The MC7800 Series of fixed voltage regulators are designed with Thermal Overload Protection that shuts down the circuit when subjected to an excessive power overload condition, Internal Short-Circuit Protection that limits the maximum current the circuit will pass, and Output Transistor Safe-Area Compensation that reduces the output short-circuit current as the voltage across the pass transistor is increased.

In many low current applications, compensation capacitors are not required. However, it is recommended that the regulator input be bypassed with a capacitor if the regulator is connected to the power supply filter with long wire lengths, or if the output load capacitance is large. An input bypass capacitor should be selected to provide good high-frequency characteristics to insure stable operation under all load conditions. A 0.33 μF or larger tantalum, mylar, or other capacitor having low internal impedance at high frequencies should be chosen. The bypass capacitor should be mounted with the shortest possible leads directly across the regulators input terminals. Normally good construction techniques should be used to minimize ground loops and lead resistance drops since the regulator has no external sense lead.

FIGURE 13 – CURRENT REGULATOR



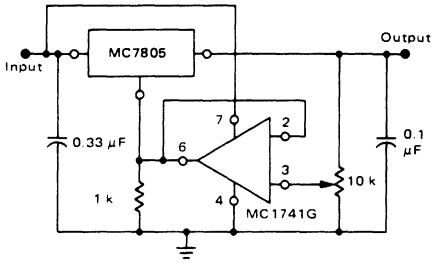
The MC7800 regulators can also be used as a current source when connected as above. In order to minimize dissipation the MC7805C is chosen in this application. Resistor R determines the current as follows:

$$I_O = \frac{5\ V}{R} + I_Q$$

$I_Q \cong 1.5$ mA over line and load changes

For example, a 1-ampere current source would require R to be a 5-ohm, 10-W resistor and the output voltage compliance would be the input voltage less 7 volts.

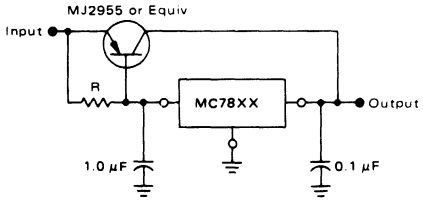
FIGURE 14 – ADJUSTABLE OUTPUT REGULATOR



V_O, 7.0 V to 20 V
V_{IN} $V_O \geq 2.0$ V

The addition of an operational amplifier allows adjustment to higher or intermediate values while retaining regulation characteristics. The minimum voltage obtainable with this arrangement is 2.0 volts greater than the regulator voltage.

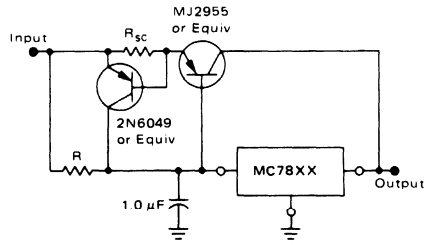
FIGURE 15 – CURRENT BOOST REGULATOR



XX = 2 digits of type number indicating voltage.

The MC7800 series can be current boosted with a PNP transistor. The MJ2955 provides current to 5.0 amperes. Resistor R in conjunction with the V_{BE} of the PNP determines when the pass transistor begins conducting; this circuit is not short-circuit proof. Input-output differential voltage minimum is increased by V_{BE} of the pass transistor.

FIGURE 16 – SHORT-CIRCUIT PROTECTION



XX = 2 digits of type number indicating voltage.

The circuit of Figure 15 can be modified to provide supply protection against short circuits by adding a short-circuit sense resistor, R_{SC}, and an additional PNP transistor. The current sensing PNP must be able to handle the short-circuit current of the three-terminal regulator. Therefore, a four-ampere plastic power transistor is specified.

MOTOROLA

MC78L00,A Series

THREE-TERMINAL LOW CURRENT POSITIVE VOLTAGE REGULATORS

The MC78L00 Series of positive voltage regulators are inexpensive, easy-to-use devices suitable for a multitude of applications that require a regulated supply of up to 100 mA. Like their higher powered MC7800 and MC78M00 Series cousins, these regulators feature internal current limiting and thermal shutdown making them remarkably rugged. No external components are required with the MC78L00 devices in many applications.

These devices offer a substantial performance advantage over the traditional zener diode-resistor combination, as output impedance and quiescent current are substantially reduced.

- Wide Range of Available, Fixed Output Voltages
- Low Cost
- Internal Short Circuit Current Limiting
- Internal Thermal Overload Protection
- No External Components Required
- Complementary Negative Regulators Offered (MC79L00 Series)
- Available in Either ±5% (AC) or ±10% (C) Selections

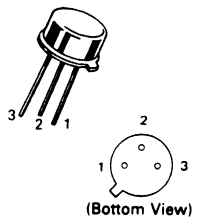
THREE-TERMINAL LOW CURRENT POSITIVE FIXED VOLTAGE REGULATORS

P SUFFIX
CASE 29-04

PIN 1. OUTPUT
2. GROUND
3. INPUT

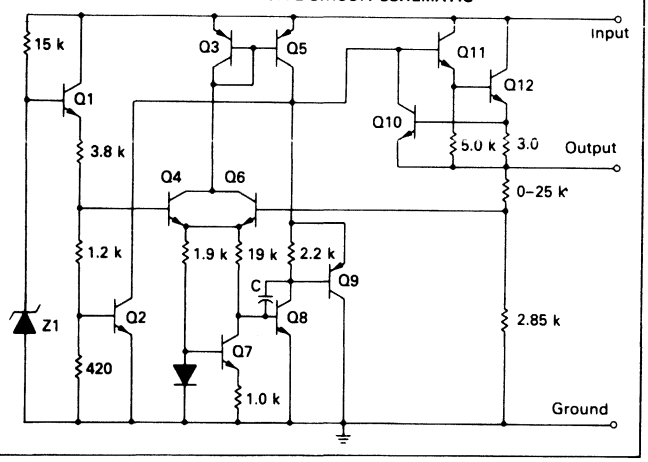
G SUFFIX
CASE 79-05

PIN 1. INPUT
2. OUTPUT
3. GROUND



(Bottom View)
(Case Connected To Pin 3)

REPRESENTATIVE CIRCUIT SCHEMATIC



D SUFFIX
PLASTIC PACKAGE
CASE 751-03
SOP-8

PIN 1. V_{OUT}
2. GND
3. GND
4. NC
5. NC
6. GND
7. GND
8. V_{IN}

SOP-8 is an internally modified SO-8 Package. Pins 2, 3, 6 and 7 are electrically common to the die attach flag. This internal lead frame modification decreases package thermal resistance and increases power dissipation capability when appropriately mounted on a printed circuit board. SOP-8 conforms to all external dimensions of the standard SO-8 Package.

ORDERING INFORMATION

Device	Junction Temperature Range	Package
MC78LXXACD*	T_J = 0°C to +125°C	SOP-8
MC78LXXACG		Metal Can
MC78LXXACP		Plastic Power
MC78LXXCG		Metal Can
MC78LXXCP		Plastic Power
MC78LXXABP#	T_J = −40°C to +125°C	Plastic Power
XX indicates nominal voltage		

#Automotive temperature range selections are available with special test conditions and additional tests in 5, 8, 12 and 15 volts devices. Contact your local Motorola sales office for information.
*Available in 5, 8, 12 and 15 volt devices.

Device No. ±10%	Device No. ±5%	Nominal Voltage
MC78L05C	MC78L05AC	5.0
MC78L08C	MC78L08AC	8.0
MC78L12C	MC78L12AC	12
MC78L15C	MC78L15AC	15
MC78L18C	MC78L18AC	18
MC78L24C	MC78L24AC	24

MC78L00 Series MAXIMUM RATINGS (T_A = +125°C unless otherwise noted.)

Rating	Symbol	Value	Unit
Input Voltage (2.6 V–8.0 V) (12 V–18 V) (24 V)	V_I	30 35 40	Vdc
Storage Junction Temperature Range	T_{stg}	−65 to +150	°C
Operating Junction Temperature Range	T_J	0 to +150	°C

MC78L05C, MC78L05AC ELECTRICAL CHARACTERISTICS (V_I = 10 V, I_O = 40 mA, C_I = 0.33 μF, C_O = 0.1 μF, 0°C < T_J < +125°C unless otherwise noted.)

Characteristic	Symbol	MC78L05AC			MC78L05C			Unit
		Min	Typ	Max	Min	Typ	Max	
Output Voltage (T_J = +25°C)	V_O	4.8	5.0	5.2	4.6	5.0	5.4	Vdc
Line Regulation (T_J = +25°C, I_O = 40 mA) 7.0 Vdc ≤ V_I ≤ 20 Vdc 8.0 Vdc ≤ V_I ≤ 20 Vdc	Reg_{line}	 — —	 55 45	 150 100	 — —	 55 45	 200 150	mV
Load Regulation (T_J = +25°C, 1.0 mA ≤ I_O ≤ 100 mA) (T_J = +25°C, 1.0 mA ≤ I_O ≤ 40 mA)	Reg_{load}	 — —	 11 5.0	 60 30	 — —	 11 5.0	 60 30	mV
Output Voltage (7.0 Vdc ≤ V_I ≤ 20 Vdc, 1.0 mA ≤ I_O ≤ 40 mA) (V_I = 10 V, 1.0 mA ≤ I_O ≤ 70 mA)	V_O	 4.75 4.75	 — —	 5.25 5.25	 4.5 4.5	 — —	 5.5 5.5	Vdc
Input Bias Current (T_J = +25°C) (T_J = +125°C)	I_{IB}	 — —	 3.8 —	 6.0 5.5	 — —	 3.8 —	 6.0 5.5	mA
Input Bias Current Change (8.0 Vdc ≤ V_I ≤ 20 Vdc) (1.0 mA ≤ I_O ≤ 40 mA)	ΔI_{IB}	 — —	 — —	 1.5 0.1	 — —	 — —	 1.5 0.2	mA
Output Noise Voltage (T_A = +25°C, 10 Hz ≤ f ≤ 100 kHz)	V_n	—	40	—	—	40	—	μV
Ripple Rejection (I_O = 40 mA, f = 120 Hz, 8.0 V ≤ V_I ≤ 18 V, T_J = +25°C)	RR	41	49	—	40	49	—	dB
Dropout Voltage (T_J = +25°C)	$V_I - V_O$	—	1.7	—	—	1.7	—	Vdc

MC78L08C, MC78L08AC ELECTRICAL CHARACTERISTICS (V_I = 14 V, I_O = 40 mA, C_I = 0.33 μF, C_O = 0.1 μF, 0°C < T_J < +125°C unless otherwise noted.)

Characteristic	Symbol	MC78L08AC			MC78L08C			Unit
		Min	Typ	Max	Min	Typ	Max	
Output Voltage (T_J = +25°C)	V_O	7.7	8.0	8.3	7.36	8.0	8.64	Vdc
Line Regulation (T_J = +25°C, I_O = 40 mA) 10.5 Vdc ≤ V_I ≤ 23 Vdc 11 Vdc ≤ V_I ≤ 23 Vdc	Reg_{line}	 — —	 20 12	 175 125	 — —	 20 12	 200 150	mV
Load Regulation (T_J = +25°C, 1.0 mA ≤ I_O ≤ 100 mA) (T_J = +25°C, 1.0 mA ≤ I_O ≤ 40 mA)	Reg_{load}	 — —	 15 8.0	 80 40	 — —	 15 6.0	 80 40	mV
Output Voltage (10.5 Vdc ≤ V_I ≤ 23 Vdc, 1.0 mA ≤ I_O ≤ 40 mA) (V_I = 14 V, 1.0 mA ≤ I_O ≤ 70 mA)	V_O	 7.6 7.6	 — —	 8.4 8.4	 7.2 7.2	 — —	 8.8 8.8	Vdc
Input Bias Current (T_J = +25°C) (T_J = +125°C)	I_{IB}	 — —	 3.0 —	 6.0 5.5	 — —	 3.0 —	 6.0 5.5	mA
Input Bias Current Change (11 Vdc ≤ V_I ≤ 23 Vdc) (1.0 mA ≤ I_O ≤ 40 mA)	ΔI_{IB}	 — —	 — —	 1.5 0.1	 — —	 — —	 1.5 0.2	mA
Output Noise Voltage (T_A = +25°C, 10 Hz ≤ f ≤ 100 kHz)	V_n	—	60	—	—	52	—	μV
Ripple Rejection (I_O = 40 mA, f = 120 Hz, 12 V ≤ V_I ≤ 23 V, T_J = +25°C)	RR	37	57	—	36	55	—	dB
Dropout Voltage (T_J = +25°C)	$V_I - V_O$	—	1.7	—	—	1.7	—	Vdc

MC78L12C, MC78L12AC ELECTRICAL CHARACTERISTICS (V_I = 19 V, I_O = 40 mA, C_I = 0.33 μF, C_O = 0.1 μF, 0°C < T_J < +125°C unless otherwise noted.)

Characteristic	Symbol	MC78L12AC			MC78L12C			Unit
		Min	Typ	Max	Min	Typ	Max	
Output Voltage (T_J = +25°C)	V_O	11.5	12	12.5	11.1	12	12.9	Vdc
Line Regulation (T_J = +25°C, I_O = 40 mA) 14.5 Vdc ≤ V_I ≤ 27 Vdc 16 Vdc ≤ V_I ≤ 27 Vdc	Reg_{line}	 — —	 120 100	 250 200	 — —	 120 100	 250 200	mV
Load Regulation (T_J = +25°C, 1.0 mA ≤ I_O ≤ 100 mA) (T_J = +25°C, 1.0 mA ≤ I_O ≤ 40 mA)	Reg_{load}	 — —	 20 10	 100 50	 — —	 20 10	 100 50	mV
Output Voltage (14.5 Vdc ≤ V_I ≤ 27 Vdc, 1.0 mA ≤ I_O ≤ 40 mA) (V_I = 19 V, 1.0 mA ≤ I_O ≤ 70 mA)	V_O	 11.4 11.4	 — —	 12.6 12.6	 10.8 10.8	 — —	 13.2 13.2	Vdc
Input Bias Current (T_J = +25°C) (T_J = +125°C)	I_{IB}	 — —	 4.2 —	 6.5 6.0	 — —	 4.2 —	 6.5 6.0	mA
Input Bias Current Change (16 Vdc ≤ V_I ≤ 27 Vdc) (1.0 mA ≤ I_O ≤ 40 mA)	ΔI_{IB}	 — —	 — —	 1.5 0.1	 — —	 — —	 1.5 0.2	mA
Output Noise Voltage (T_A = +25°C, 10 Hz ≤ f ≤ 100 kHz)	V_n	—	80	—	—	80	—	μV
Ripple Rejection (I_O = 40 mA, f = 120 Hz, 15 V ≤ V_I ≤ 25 V, T_J = +25°C)	RR	37	42	—	36	42	—	dB
Dropout Voltage (T_J = +25°C)	V_I-V_O	—	1.7	—	—	1.7	—	Vdc

MC78L15C, MC78L15AC ELECTRICAL CHARACTERISTICS (V_I = 23 V, I_O = 40 mA, C_I = 0.33 μF, C_O = 0.1 μF, 0°C < T_J < +125°C unless otherwise noted.)

Characteristic	Symbol	MC78L15AC			MC78L15C			Unit
		Min	Typ	Max	Min	Typ	Max	
Output Voltage (T_J = +25°C)	V_O	14.4	15	15.6	13.8	15	16.2	Vdc
Line Regulation (T_J = +25°C, I_O = 40 mA) 17.5 Vdc ≤ V_I ≤ 30 Vdc 20 Vdc ≤ V_I ≤ 30 Vdc	Reg_{line}	 — —	 130 110	 300 250	 — —	 130 110	 300 250	mV
Load Regulation (T_J = +25°C, 1.0 mA ≤ I_O ≤ 100 mA) (T_J = +25°C, 1.0 mA ≤ I_O ≤ 40 mA)	Reg_{load}	 — —	 25 12	 150 75	 — —	 25 12	 150 75	mV
Output Voltage (17.5 Vdc ≤ V_I ≤ 30 Vdc, 1.0 mA ≤ I_O ≤ 40 mA) (V_I = 23 V, 1.0 mA ≤ I_O ≤ 70 mA)	V_O	 14.25 14.25	 — —	 15.75 15.75	 13.5 13.5	 — —	 16.5 16.5	Vdc
Input Bias Current (T_J = +25°C) (T_J = +125°C)	I_{IB}	 — —	 4.4 —	 6.5 6.0	 — —	 4.4 —	 6.5 6.0	mA
Input Bias Current Change (20 Vdc ≤ V_I ≤ 30 Vdc) (1.0 mA ≤ I_O ≤ 40 mA)	ΔI_{IB}	 — —	 — —	 1.5 0.1	 — —	 — —	 1.5 0.2	mA
Output Noise Voltage (T_A = +25°C, 10 Hz ≤ f ≤ 100 kHz)	V_n	—	90	—	—	90	—	μV
Ripple Rejection (I_O = 40 mA, f = 120 Hz, 18.5 V ≤ V_I ≤ 28.5 V, T_J = +25°C)	RR	34	39	—	33	39	—	dB
Dropout Voltage (T_J = +25°C)	V_I-V_O	—	1.7	—	—	1.7	—	Vdc

MC78L18C, MC78L18AC ELECTRICAL CHARACTERISTICS (V_I = 27 V, I_O = 40 mA, C_I = 0.33 μF, C_O = 0.1 μF, 0°C < T_J < +125°C unless otherwise noted.)

Characteristic	Symbol	MC78L18AC			MC78L18C			Unit
		Min	Typ	Max	Min	Typ	Max	
Output Voltage (T_J = +25°C)	V_O	17.3	18	18.7	16.6	18	19.4	Vdc
Line Regulation (T_J = +25°C, I_O = 40 mA) 21.4 Vdc ≤ V_I ≤ 33 Vdc 20.7 Vdc ≤ V_I ≤ 33 Vdc 22 Vdc ≤ V_I ≤ 33 Vdc 21 Vdc ≤ V_I ≤ 33 Vdc	Reg_{line}	 — —	 45 35	 325 275	 — —	 32 27	 325 275	mV
Load Regulation (T_J = +25°C, 1.0 mA ≤ I_O ≤ 100 mA) (T_J = +25°C, 1.0 mA ≤ I_O ≤ 40 mA)	Reg_{load}	 — —	 30 15	 170 85	 — —	 30 15	 170 85	mV
Output Voltage (21.4 Vdc ≤ V_I ≤ 33 Vdc, 1.0 mA ≤ I_O ≤ 40 mA) (20.7 Vdc ≤ V_I ≤ 33 Vdc, 1.0 mA ≤ I_O ≤ 40 mA) (V_I = 27 V, 1.0 mA ≤ I_O ≤ 70 mA) (V_I = 27 V, 1.0 mA ≤ I_O ≤ 70 mA)	V_O	 17.1 17.1	 — —	 18.9 18.9	 16.2 16.2 	 — —	 19.8 19.8 	Vdc
Input Bias Current (T_J = +25°C) (T_J = +125°C)	I_{IB}	 — —	 3.1 —	 6.5 6.0	 — —	 3.1 —	 6.5 6.0	mA
Input Bias Current Change (22 Vdc ≤ V_I ≤ 33 Vdc) (21 Vdc ≤ V_I = 33 Vdc) (1.0 mA ≤ I_O ≤ 40 mA)	ΔI_{IB}	 — —	 — —	 1.5 0.1	 — —	 — —	 1.5 0.2	mA
Output Noise Voltage (T_A = +25°C, 10 Hz ≤ f ≤ 100 kHz)	V_n	—	150	—	—	150	—	μV
Ripple Rejection (I_O = 40 mA, f = 120 Hz, 23 V ≤ V_I ≤ 33 V, T_J = +25°C)	RR	33	48	—	32	46	—	dB
Dropout Voltage (T_J = +25°C)	V_I-V_O	—	1.7	—	—	1.7	—	Vdc

MC78L24C, MC78L24AC ELECTRICAL CHARACTERISTICS (V_I = 33 V, I_O = 40 mA, C_I = 0.33 μF, C_O = 0.1 μF, 0°C < T_J < +125°C unless otherwise noted.)

Characteristic	Symbol	MC78L24AC			MC78L24C			Unit
		Min	Typ	Max	Min	Typ	Max	
Output Voltage (T_J = +25°C)	V_O	23	24	25	22.1	24	25.9	Vdc
Line Regulation (T_J = +25°C, I_O = 40 mA) 27.5 Vdc ≤ V_I ≤ 38 Vdc 28 Vdc ≤ V_I ≤ 80 Vdc 27 Vdc ≤ V_I ≤ 38 Vdc	Reg_{line}	 — — —	 — 50 60	 — 300 350	 — — —	 35 30 —	 350 300 —	mV
Load Regulation (T_J = +25°C, 1.0 mA ≤ I_O ≤ 100 mA) (T_J = +25°C, 1.0 mA ≤ I_O ≤ 40 mA)	Reg_{load}	 — —	 40 20	 200 100	 — —	 40 20	 200 100	mV
Output Voltage (28 Vdc ≤ V_I ≤ 38 Vdc, 1.0 mA ≤ I_O ≤ 40 mA) (27 Vdc ≤ V_I ≤ 38 Vdc, 1.0 mA ≤ I_O ≤ 40 mA) (28 Vdc ≤ V_I = 33 V, 1.0 mA ≤ I_O ≤ 70 mA) (27 Vdc ≤ V_I ≤ 33 V, 1.0 mA ≤ I_O ≤ 70 mA)	V_O	 22.8 22.8	 — —	 25.2 25.2	 21.6 21.6 	 — —	 26.4 26.4 	Vdc
Input Bias Current (T_J = +25°C) (T_J = +125°C)	I_{IB}	 — —	 3.1 —	 6.5 6.0	 — —	 3.1 —	 6.5 6.0	mA
Input Bias Current Change (28 Vdc ≤ V_I ≤ 38 Vdc) (1.0 mA ≤ I_O ≤ 40 mA)	ΔI_{IB}	 — —	 — —	 1.5 0.1	 — —	 — —	 1.5 0.2	mA
Output Noise Voltage (T_A = +25°C, 10 Hz ≤ f ≤ 100 kHz)	V_n	—	200	—	—	200	—	μV
Ripple Rejection (I_O = 40 mA, f = 120 Hz, 29 V ≤ V_I ≤ 35 V, T_J = +25°C)	RR	31	45	—	30	43	—	dB
Dropout Voltage (T_J = +25°C)	V_I-V_O	—	1.7	—	—	1.7	—	Vdc

TYPICAL CHARACTERISTICS

(T_A = +25°C unless otherwise noted.)

FIGURE 1 – DROPOUT CHARACTERISTICS

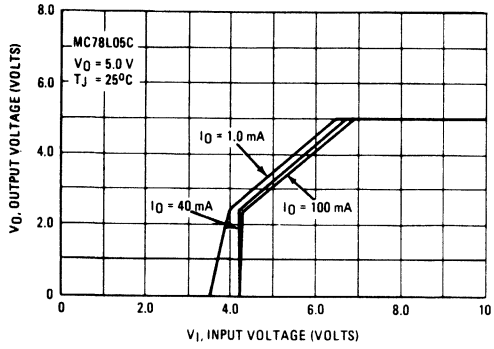


FIGURE 2 – DROPOUT VOLTAGE versus JUNCTION TEMPERATURE

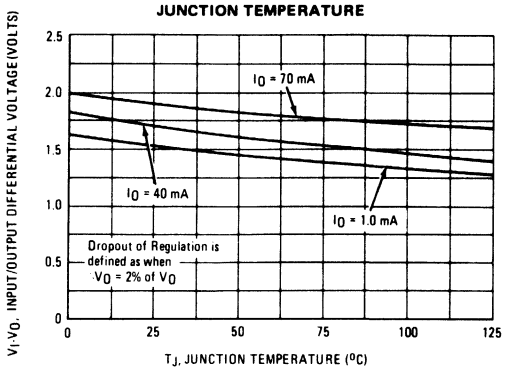


FIGURE 3 – INPUT BIAS CURRENT versus AMBIENT TEMPERATURE

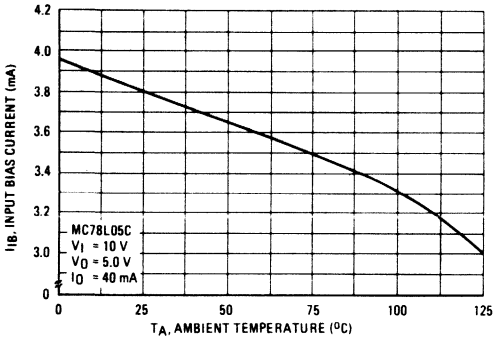


FIGURE 4 – INPUT BIAS CURRENT versus INPUT VOLTAGE

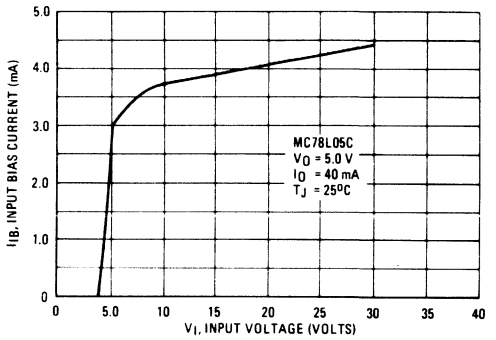


FIGURE 5 – MAXIMUM AVERAGE POWER DISSIPATION versus AMBIENT TEMPERATURE – TO-92 Type Package

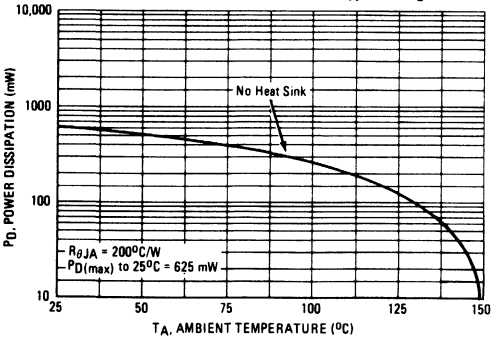
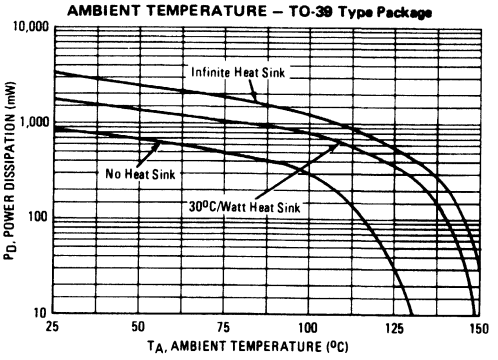


FIGURE 6 – MAXIMUM AVERAGE POWER DISSIPATION versus AMBIENT TEMPERATURE – TO-39 Type Package



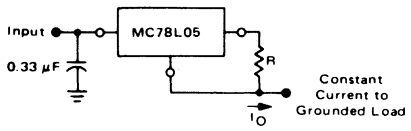
APPLICATIONS INFORMATION

Design Considerations

The MC78L00 Series of fixed voltage regulators are designed with Thermal Overload Protection that shuts down the circuit when subjected to an excessive power overload condition. Internal Short-Circuit Protection limits the maximum current the circuit will pass.

In many low current applications, compensation capacitors are not required. However, it is recommended that the regulator input be bypassed with a capacitor if the regulator is connected to the power supply filter with long wire lengths, or if the output load capacitance is large. The input bypass capacitor should be selected to provide good high-frequency characteristics to insure stable operation under all load conditions. A 0.33 μF or larger tantalum, mylar, or other capacitor having low internal impedance at high frequencies should be chosen. The bypass capacitor should be mounted with the shortest possible leads directly across the regulators input terminals. Good construction techniques should be used to minimize ground loops and lead resistance drops since the regular has no external sense lead. Bypassing the output is also recommended.

FIGURE 7 – CURRENT REGULATOR



The MC78L00 regulators can also be used as a current source when connected as above. In order to minimize dissipation the MC78L05C is chosen in this application. Resistor R determines the current as follows:

$$I_O = \frac{5\ V}{R} + I_{IB}$$

I_{IB} = 3.8 mA over line and load changes

For example, a 100 mA current source would require R to be a 50-ohm, 1/2-W resistor and the output voltage compliance would be the input voltage less 7 volts.

FIGURE 8 – ±15 V TRACKING VOLTAGE REGULATOR

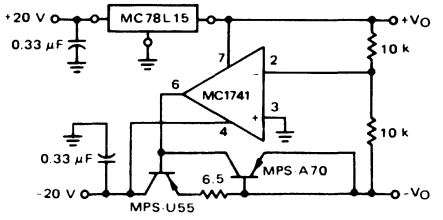
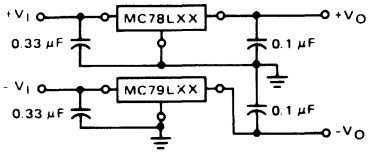
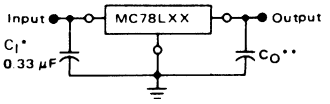


FIGURE 9 – POSITIVE AND NEGATIVE REGULATOR



STANDARD APPLICATION



A common ground is required between the input and the output voltages. The input voltage must remain typically 2.0 V above the output voltage even during the low point on the input ripple voltage.

* = C_I is required if regulator is located an appreciable distance from power supply filter.

** = C_O is not needed for stability; however, it does improve transient response.

MOTOROLA

MC78M00 Series

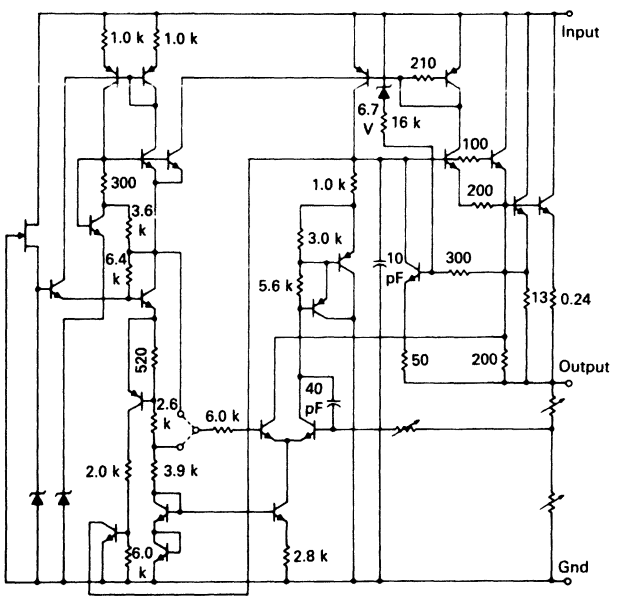
THREE-TERMINAL MEDIUM CURRENT POSITIVE VOLTAGE REGULATORS

The MC78M00 Series positive voltage regulators are identical to the popular MC7800 Series devices, except that they are specified for only half the output current. Like the MC7800 devices, the MC78M00 three-terminal regulators are intended for local, on-card voltage regulation.

Internal current limiting, thermal shutdown circuitry and safe-area compensation for the internal pass transistor combine to make these devices remarkably rugged under most operating conditions. Maximum output current, with adequate heatsinking is 500 mA.

- No External Components Required
- Internal Thermal Overload Protection
- Internal Short-Circuit Current Limiting
- Output Transistor Safe-Area Compensation

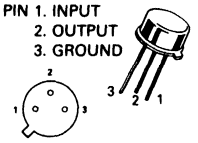
EQUIVALENT SCHEMATIC DIAGRAM



TYPE NO./VOLTAGE		
MC78M05B,C 5.0 Volts	MC78M12B,C 12 Volts	MC78M20B,C 20 Volts
MC78M06B,C 6.0 Volts	MC78M15B,C 15 Volts	MC78M24B,C 24 Volts
MC78M08B,C 8.0 Volts	MC78M18B,C 18 Volts	

THREE-TERMINAL MEDIUM CURRENT POSITIVE FIXED VOLTAGE REGULATORS

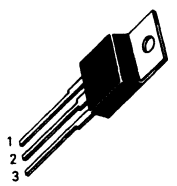
PIN 1. INPUT
2. OUTPUT
3. GROUND



(Bottom View)

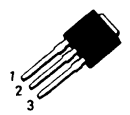
G SUFFIX
METAL PACKAGE
CASE 79-05
(Case connected to Pin 3)

T SUFFIX
PLASTIC PACKAGE
CASE 221A-04



(All 3 Plastic Types)
PIN 1. INPUT
2. GROUND
3. OUTPUT
(Heatsink surface connected to Pin 2)

DT SUFFIX
PLASTIC PACKAGE
CASE 369A-03
DPAK



DT-1 SUFFIX
PLASTIC PACKAGE
CASE 369-03
DPAK

ORDERING INFORMATION		
Device	Tested Operating Junction Temp. Range	Package
MC78MXXCG*	T_J = 0°C to +125°C	Metal Can
MC78MXXCDT**		DPAK
MC78MXXCDT-1**		
MC78MXXCT		Plastic Power
MC78MXXBT#	T_J = −40°C to +125°C	Plastic Power

XX Indicates nominal voltage.
* Available in 5, 8, 12 and 15 volt devices.
** Available in 5, 12 and 15 volt devices.
\# Automotive temperature range selections are available with special test conditions and additional tests in 5, 8, 12 and 15 volt devices. Contact your local Motorola sales office for information.

MAXIMUM RATINGS (T_A = +25°C unless otherwise noted.)

Rating	Symbol	Value	Unit
Input Voltage (5.0 V–18 V) (20 V–24 V)	V_I	35 40	Vdc
Power Dissipation (Package Limitation) Plastic Package T_A = 25°C Derate above T_A = 25°C T_C = 25°C Derate above T_C = 110°C Metal Package T_A = 25°C Derate above T_A = 25°C T_C = 25°C Derate above T_C = 85°C	 P_D θ_{JA} P_D θ_{JC} P_D θ_{JA} P_D θ_{JC}	 Internally Limited 70 Internally Limited 5.0 Internally Limited 185 Internally Limited 25	 °C/W °C/W °C/W °C/W
Operating Junction Temperature Range MC78MXXC MC78MXXB	T_J	0 to +150 −40 to +150	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C

MC78M05B,C ELECTRICAL CHARACTERISTICS (V_I = 10 V, I_O = 350 mA, 0°C < T_J < +125°C, $P_D \leq$ 5.0 W unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Output Voltage (T_J = +25°C)	V_O	4.8	5.0	5.2	Vdc
Line Regulation (T_J = +25°C, 7.0 Vdc ≤ V_I ≤ 25 Vdc, I_O = 200 mA)	Reg_{line}	—	3.0	50	mV
Load Regulation (T_J = +25°C, 5.0 mA ≤ I_O ≤ 500 mA) (T_J = +25°C, 5.0 mA ≤ I_O ≤ 200 mA)	Reg_{load}	 — —	 20 10	 100 50	mV
Output Voltage (7.0 Vdc ≤ V_I ≤ 25 Vdc, 5.0 mA ≤ I_O ≤ 200 mA) (7.0 Vdc ≤ V_I ≤ 20 Vdc, 5.0 mA ≤ I_O ≤ 350 mA)	V_O	4.75	—	5.25	Vdc
Input Bias Current (T_J = +25°C)	I_{IB}	—	3.2	6.0	mA
Quiescent Current Change (8.0 Vdc ≤ V_I ≤ 25 Vdc, I_O = 200 mA) (5.0 mA ≤ I_O ≤ 350 mA)	ΔI_{IB}	 — —	 — —	 0.8 0.5	mA
Output Noise Voltage (T_A = +25°C, 10 Hz ≤ f ≤ 100 kHz)	V_n	—	40	—	μV
Ripple Rejection (T, DT and DT-1 suffixes only) (I_O = 100 mA, f = 120 Hz, 8.0 V ≤ V_I ≤ 18 V) (I_O = 300 mA, f = 120 Hz, 8.0 ≤ V_I ≤ 18 V, T_J = 25°C)	RR	 62 62	 — 80	 — —	dB
Dropout Voltage (T_J = +25°C)	V_I-V_O	—	2.0	—	Vdc
Short Circuit Current Limit (T_J = +25°C, V_I = 35 V)	I_{OS}	—	50	—	mA
Average Temperature Coefficient of Output Voltage (I_O = 5.0 mA)	$\Delta V_O/\Delta T$	—	±0.2	—	mV/°C
Peak Output Current (T_J = 25°C)	I_O	—	700	—	mA

MC78M06C ELECTRICAL CHARACTERISTICS (V_I = 11 V, I_O = 350 mA, 0°C < T_J < +125°C, P_D ≤ 5.0 W unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Output Voltage (T_J = +25°C)	V_O	5.75	6.0	6.25	Vdc
Line Regulation (T_J = +25°C, 8.0 Vdc ≤ V_I ≤ 25 Vdc, I_O = 200 mA)	Reg_{line}	—	5.0	50	mV
Load Regulation (T_J = +25°C, 5.0 mA ≤ I_O ≤ 500 mA) (T_J = +25°C, 5.0 mA ≤ I_O ≤ 200 mA)	Reg_{load}	 — —	 20 10	 120 60	mV
Output Voltage (8.0 Vdc ≤ V_I ≤ 25 Vdc, 5.0 mA ≤ I_O ≤ 200 mA) (8.0 Vdc ≤ V_I ≤ 21 Vdc, 5.0 mA ≤ I_O ≤ 350 mA)	V_O	5.7	—	6.3	Vdc
Input Bias Current (T_J = +25°C)	I_{IB}	—	3.2	6.0	mA
Quiescent Current Change (9.0 Vdc ≤ V_I ≤ 25 Vdc, I_O = 200 mA) (5.0 mA ≤ I_O ≤ 350 mA)	ΔI_{IB}	 — —	 — —	 0.8 0.5	mA
Output Noise Voltage (T_A = +25°C, 10 Hz ≤ f ≤ 100 kHz)	V_n	—	45	—	μV
Ripple Rejection (T suffix only) (I_O = 100 mA, f = 120 Hz, 9.0 V ≤ V_I ≤ 19 V) (I_O = 300 mA, f = 120 Hz, 9.0 V ≤ V_I ≤ 19 V, T_J = 25°C)	RR	 59 59	 — 80	 — —	dB
Dropout Voltage (T_J = +25°C)	V_I-V_O	—	2.0	—	Vdc
Short Circuit Current Limit (T_J = +25°C, V_I = 35 V)	I_{OS}	—	50	—	mA
Average Temperature Coefficient of Output Voltage (I_O = 5.0 mA)	$\Delta V_O/\Delta T$	—	±0.2	—	mV/°C
Peak Output Current (T_J = 25°C)	I_O	—	700	—	mA

MC78M08B,C ELECTRICAL CHARACTERISTICS (V_I = 14 V, I_O = 350 mA, 0°C < T_J < +125°C, P_D ≤ 5.0 W unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Output Voltage (T_J = +25°C)	V_O	7.7	8.0	8.3	Vdc
Line Regulation (T_J = +25°C, 10.5 Vdc ≤ V_I ≤ 25 Vdc, I_O = 200 mA)	Reg_{line}	—	6.0	50	mV
Load Regulation (T_J = +25°C, 5.0 mA ≤ I_O ≤ 500 mA) (T_J = +25°C, 5.0 mA ≤ I_O ≤ 200 mA)	Reg_{load}	 — —	 25 10	 160 80	mV
Output Voltage (10.5 Vdc ≤ V_I ≤ 25 Vdc, 5.0 mA ≤ I_O ≤ 200 mA) (10.5 Vdc ≤ V_I ≤ 23 Vdc, 5.0 mA ≤ I_O ≤ 350 mA)	V_O	7.6	—	8.4	Vdc
Input Bias Current (T_J = +25°C)	I_{IB}	—	3.2	6.0	mA
Quiescent Current Change (10.5 Vdc ≤ V_I ≤ 25 Vdc, I_O = 200 mA) (5.0 mA ≤ I_O ≤ 350 mA)	ΔI_{IB}	 — —	 — —	 0.8 0.5	mA
Output Noise Voltage (T_A = +25°C, 10 Hz ≤ f ≤ 100 kHz)	V_n	—	52	—	μV
Ripple Rejection (T suffix only) (I_O = 100 mA, f = 120 Hz, 11.5 V ≤ V_I ≤ 21.5 V) (I_O = 300 mA, f = 120 Hz, 11.5 V ≤ V_I ≤ 21.5 V, T_J = 25°C)	RR	 56 56	 — 80	 — —	dB
Dropout Voltage (T_J = +25°C)	V_I-V_O	—	2.0	—	Vdc
Short Circuit Current Limit (T_J = +25°C, V_I = 35 V)	I_{OS}	—	50	—	mA
Average Temperature Coefficient of Output Voltage (I_O = 5.0 mA)	$\Delta V_O/\Delta T$	—	±0.2	—	mV/°C
Peak Output Current (T_J = 25°C)	I_O	—	700	—	mA

MC78M12B,C ELECTRICAL CHARACTERISTICS (V_I = 19 V, I_O = 350 mA, 0°C < T_J < +125°C, $P_D \leq$ 5.0 W unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Output Voltage (T_J = +25°C)	V_O	11.5	12	12.5	Vdc
Line Regulation (T_J = +25°C, 14.5 Vdc ≤ V_I ≤ 30 Vdc, I_O = 200 mA)	Reg_{line}	—	8.0	50	mV
Load Regulation (T_J = +25°C, 5.0 mA ≤ I_O ≤ 500 mA) (T_J = +25°C, 5.0 mA ≤ I_O ≤ 200 mA)	Reg_{load}	 — —	 25 10	 240 120	mV
Output Voltage (14.5 Vdc ≤ V_I ≤ 27 Vdc, 5.0 mA ≤ I_O ≤ 350 mA)	V_O	11.4	—	12.6	Vdc
Input Bias Current (T_J = +25°C)	I_{IB}	—	3.2	6.0	mA
Quiescent Current Change (14.5 Vdc ≤ V_I ≤ 30 Vdc, I_O = 200 mA) (5.0 mA ≤ I_O ≤ 350 mA)	ΔI_{IB}	 — —	 — —	 0.8 0.5	mA
Output Noise Voltage (T_A = +25°C, 10 Hz ≤ f ≤ 100 kHz)	V_n	—	75	—	μV
Ripple Rejection (T, DT and DT-1 suffixes only) (I_O = 100 mA, f = 120 Hz, 15 V ≤ V_I ≤ 25 V) (I_O = 300 mA, f = 120 Hz, 15 V ≤ V_I ≤ 25 V, T_J = 25°C)	RR	 55 55	 — 80	 — —	dB
Dropout Voltage (T_J = +25°C)	V_I-V_O	—	2.0	—	Vdc
Short Circuit Current Limit (T_J = +25°C, V_I = 35 V)	I_{OS}	—	50	—	mA
Average Temperature Coefficient of Output Voltage (I_O = 5.0 mA)	$\Delta V_O/\Delta T$	—	±0.3	—	mV/°C
Peak Output Current (T_J = 25°C)	I_O	—	700	—	mA

MC78M15B,C ELECTRICAL CHARACTERISTICS (V_I = 23 V, I_O = 350 mA, 0°C < T_J < +125°C, $P_D \leq$ 5.0 W unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Output Voltage (T_J = +25°C)	V_O	14.4	15	15.6	Vdc
Input Regulation (T_J = +25°C, 17.5 Vdc ≤ V_I ≤ 30 Vdc, I_O = 200 mA)	Reg_{line}	—	10	50	mV
Load Regulation (T_J = +25°C, 5.0 mA ≤ I_O ≤ 500 mA) (T_J = +25°C, 5.0 mA ≤ I_O ≤ 200 mA)	Reg_{load}	 — —	 25 10	 300 150	mV
Output Voltage (17.5 Vdc ≤ V_I ≤ 30 Vdc, 5.0 mA ≤ I_O ≤ 350 mA)	V_O	14.25	—	15.75	Vdc
Input Bias Current (T_J = +25°C)	I_{IB}	—	3.2	6.0	mA
Quiescent Current Change (17.5 Vdc ≤ V_I ≤ 30 Vdc, I_O = 200 mA) (5.0 mA ≤ I_O ≤ 350 mA)	ΔI_{IB}	 — —	 — —	 0.8 0.5	mA
Output Noise Voltage (T_A = +25°C, 10 Hz ≤ f ≤ 100 kHz)	V_n	—	90	—	μV
Ripple Rejection (T, DT and DT-1 suffixes only) (I_O = 100 mA, f = 120 Hz, 18.5 V ≤ V_I ≤ 28.5 V) (I_O = 300 mA, f = 120 Hz, 18.5 V ≤ V_I ≤ 28.5 V, T_J = 25°C)	RR	 54 54	 — 70	 — —	dB
Dropout Voltage (T_J = +25°C)	V_I-V_O	—	2.0	—	Vdc
Short Circuit Current Limit (T_J = +25°C, V_I = 35 V)	I_{OS}	—	50	—	mA
Average Temperature Coefficient of Output Voltage (I_O = 5.0 mA)	$\Delta V_O/\Delta T$	—	±0.3	—	mV/°C
Peak Output Current (T_J = 25°C)	I_O	—	700	—	mA

MC78M18C ELECTRICAL CHARACTERISTICS (V_I = 27 V, I_O = 350 mA, 0°C < T_J < +125°C, P_D ≤ 5.0 W unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Output Voltage (T_J = +25°C)	V_O	17.3	18	18.7	Vdc
Line Regulation (T_J = +25°C, 21 Vdc ≤ V_I ≤ 33 Vdc, I_O = 200 mA)	Reg_{line}	—	10	50	mV
Load Regulation (T_J = +25°C, 5.0 mA ≤ I_O ≤ 500 mA) (T_J = +25°C, 5.0 mA ≤ I_O ≤ 200 mA)	Reg_{load}	 — —	 30 10	 360 180	mV
Output Voltage (21 Vdc ≤ V_I ≤ 33 Vdc, 5.0 mA ≤ I_O ≤ 350 mA)	V_O	17.1	—	18.9	Vdc
Input Bias Current (T_J = +25°C)	I_{IB}	—	3.2	6.5	mA
Quiescent Current Change (21 Vdc ≤ V_I ≤ 33 Vdc, I_O = 200 mA) (5.0 mA ≤ I_O ≤ 350 mA)	ΔI_{IB}	 — —	 — —	 0.8 0.5	mA
Output Noise Voltage (T_A = +25°C, 10 Hz ≤ f ≤ 100 kHz)	V_n	—	100	—	μV
Ripple Rejection (T suffix only) (I_O = 100 mA, f = 120 Hz, 22 V ≤ V_I ≤ 32 V) (I_O = 300 mA, f = 120 Hz, 22 V ≤ V_I ≤ 32 V, T_J = 25°C)	RR	 53 53	 — 70	 — —	dB
Dropout Voltage (T_J = +25°C)	V_I-V_O	—	2.0	—	Vdc
Short Circuit Current Limit (T_J = +25°C, V_I = 35 V)	I_{OS}	—	50	—	mA
Average Temperature Coefficient of Output Voltage (I_O = 5.0 mA)	$\Delta V_O/\Delta T$	—	±0.3	—	mV/°C
Peak Output Current (T_J = 25°C)	I_O	—	700	—	mA

MC78M20C ELECTRICAL CHARACTERISTICS (V_I = 29 V, I_O = 350 mA, 0°C < T_J < +125°C, P_D ≤ 5.0 W unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Output Voltage (T_J = +25°C)	V_O	19.2	20	20.8	Vdc
Line Regulation (T_J = +25°C, 23 Vdc ≤ V_I ≤ 35 Vdc, I_O = 200 mA)	Reg_{line}	—	10	50	mV
Load Regulation (T_J = +25°C, 5.0 mA ≤ I_O ≤ 500 mA) (T_J = +25°C, 5.0 mA ≤ I_O ≤ 200 mA)	Reg_{load}	 — —	 30 10	 400 200	mV
Output Voltage (23 Vdc ≤ V_I ≤ 35 Vdc, 5.0 mA ≤ I_O ≤ 350 mA)	V_O	19	—	21	Vdc
Input Bias Current (T_J = +25°C)	I_{IB}	—	3.2	6.5	mA
Quiescent Current Change (23 Vdc ≤ V_I ≤ 35 Vdc, I_O = 200 mA) (5.0 mA ≤ I_O ≤ 350 mA)	ΔI_{IB}	 — —	 — —	 0.8 0.5	mA
Output Noise Voltage (T_A = +25°C, 10 Hz ≤ f ≤ 100 kHz)	V_n	—	110	—	μV
Ripple Rejection (T suffix only) (I_O = 100 mA, f = 120 Hz, 24 V ≤ V_I ≤ 34 V) (I_O = 300 mA, f = 120 Hz, 24 V ≤ V_I ≤ 34 V, T_J = 25°C)	RR	 52 52	 — 70	 — —	dB
Dropout Voltage (T_J = +25°C)	V_I-V_O	—	2.0	—	Vdc
Short Circuit Current Limit (T_J = +25°C, V_I = 35 V)	I_{OS}	—	50	—	mA
Average Temperature Coefficient of Output Voltage (I_O = 5.0 mA)	$\Delta V_O/\Delta T$	—	±0.5	—	mV/°C
Peak Output Current (T_J = 25°C)	I_O	—	700	—	mA

MC78M24C ELECTRICAL CHARACTERISTICS (V_I = 33 V, I_O = 350 mA, 0°C < T_J < +125°C, P_D ≤ 5.0 W unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Output Voltage (T_J = +25°C)	V_O	23	24	25	Vdc
Line Regulation (T_J = +25°C, 27 Vdc ≤ V_I ≤ 38 Vdc, I_O = 200 mA)	Reg_{line}	—	10	50	mV
Load Regulation (T_J = +25°C, 5.0 mA ≤ I_O ≤ 500 mA) (T_J = +25°C, 5.0 mA ≤ I_O ≤ 200 mA)	Reg_{load}	— —	30 10	480 240	mV
Output Voltage (27 Vdc ≤ V_I ≤ 38 Vdc, 5.0 mA ≤ I_O ≤ 350 mA)	V_O	22.8	—	25.2	Vdc
Input Bias Current (T_J = +25°C)	I_{IB}	—	3.2	7.0	mA
Quiescent Current Change (27 Vdc ≤ V_I ≤ 38 Vdc, I_O = 200 mA) (5.0 mA ≤ I_O ≤ 350 mA)	ΔI_{IB}	— —	— —	0.8 0.5	mA
Output Noise Voltage (T_A = +25°C, 10 Hz ≤ f ≤ 100 kHz)	V_n	—	170	—	μV
Ripple Rejection (T suffix only) (I_O = 100 mA, f = 120 Hz, 28 V ≤ V_I ≤ 38 V) (I_O = 300 mA, f = 120 Hz, 28 V ≤ V_I ≤ 38 V, T_J = 25°C)	RR	50 50	— 70	— —	dB
Dropout Voltage (T_J = +25°C)	V_I-V_O	—	2.0	—	Vdc
Short Circuit Current Limit (T_J = +25°C)	I_{OS}	—	50	—	mA
Average Temperature Coefficient of Output Voltage (I_O = 5.0 mA)	$\Delta V_O/\Delta T$	—	±0.5	—	mV/°C
Peak Output Current (T_J = 25°C)	I_O	—	700	—	mA

DEFINITIONS

Line Regulation — The change in output voltage for a change in the input voltage. The measurement is made under conditions of low dissipation or by using pulse techniques such that the average chip temperature is not significantly affected.

Load Regulation — The change in output voltage for a change in load current at constant chip temperature.

Maximum Power Dissipation — The maximum total device dissipation for which the regulator will operate within specifications.

Input Bias Current — That part of the input current that is not delivered to the load.

Output Noise Voltage — The rms ac voltage at the output, with constant load and no input ripple, measured over a specified frequency range.

Long Term Stability — Output voltage stability under accelerated life test conditions with the maximum rated voltage listed in the devices' electrical characteristics and maximum power dissipation.

TYPICAL PERFORMANCE CURVES

FIGURE 1 — WORST CASE POWER DISSIPATION versus AMBIENT TEMPERATURE TO-220AB (CASE 221A)

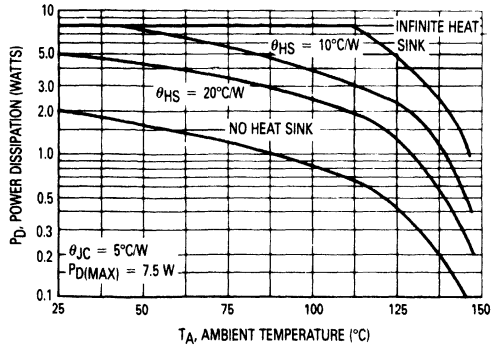
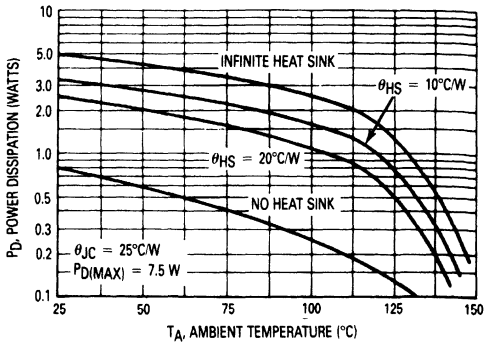


FIGURE 2 — WORST CASE POWER DISSIPATION versus AMBIENT TEMPERATURE (CASE 79)



TYPICAL PERFORMANCE CURVES

FIGURE 3 — PEAK OUTPUT CURRENT versus DROPOUT VOLTAGE

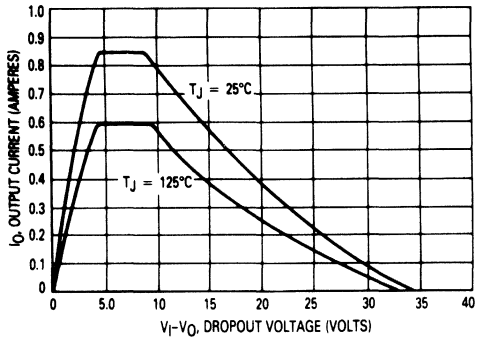


FIGURE 4 — DROPOUT VOLTAGE versus JUNCTION TEMPERATURE

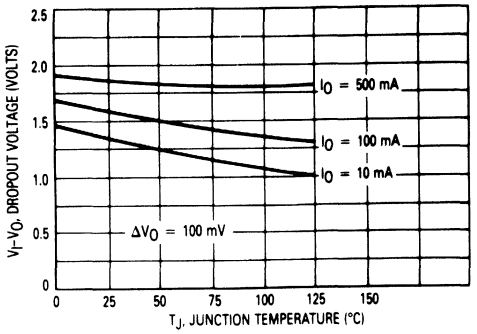


FIGURE 5 — RIPPLE REJECTION versus FREQUENCY

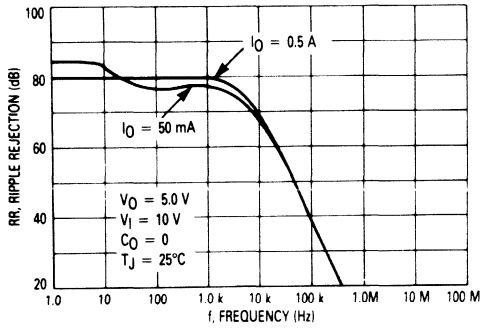


FIGURE 6 — RIPPLE REJECTION versus OUTPUT CURRENT

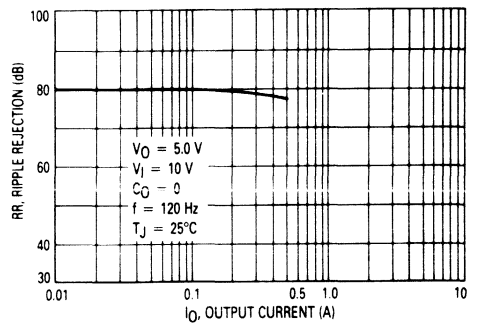


FIGURE 7 — BIAS CURRENT versus INPUT VOLTAGE

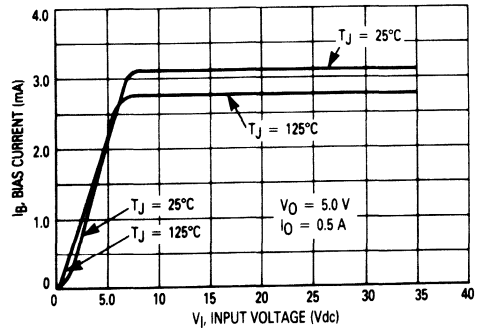
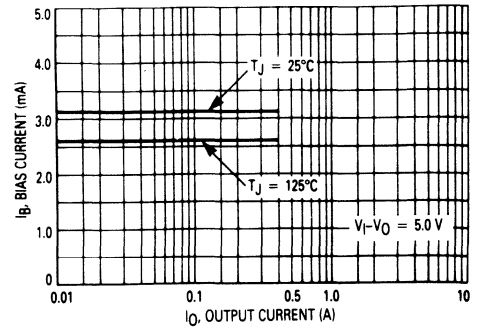


FIGURE 8 — BIAS CURRENT versus OUTPUT CURRENT



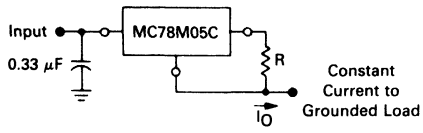
APPLICATIONS INFORMATION

DESIGN CONSIDERATIONS

The MC78M00 Series of fixed voltage regulators are designed with Thermal Overload Protection that shuts down the circuit when subjected to an excessive power overload condition, Internal Short Circuit Protection that limits the maximum current the circuit will pass, and Output Transistor Safe-Area Compensation that reduces the output short circuit current as the voltage across the pass transistor is increased.

In many low current applications, compensation capacitors are not required. However, it is recommended that the regulator input be bypassed with a capacitor if the regulator is connected to the power supply filter with long wire lengths, or if the output load capacitance is large. An input bypass capacitor should be selected to provide good high frequency characteristics to insure stable operation under all load conditions. A 0.33 μF or larger tantalum, mylar, or other capacitor having low internal impedance at high frequencies should be chosen. The bypass capacitor should be mounted with the shortest possible leads directly across the regulators input terminals. Normally good construction techniques should be used to minimize ground loops and lead resistance drops since the regulator has no external sense lead.

FIGURE 9 — CURRENT REGULATOR



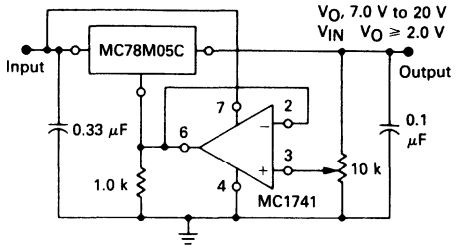
The MC78M00 regulators can also be used as a current source when connected as above. In order to minimize dissipation the MC78M05C is chosen in this application. Resistor R determines the current as follows:

$$I_O = \frac{5.0\ V}{R} + I_{IB}$$

I_{IB} = 1.5 mA over line and load changes

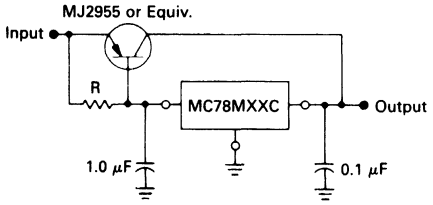
For example, a 500 mA current source would require R to be a 10 ohm, 10 W resistor and the output voltage compliance would be the input voltage less 7.0 volts.

FIGURE 10 — ADJUSTABLE OUTPUT REGULATOR



The addition of an operational amplifier allows adjustment to higher or intermediate values while retaining regulation characteristics. The minimum voltage obtainable with this arrangement is 2.0 volts greater than the regulator voltage.

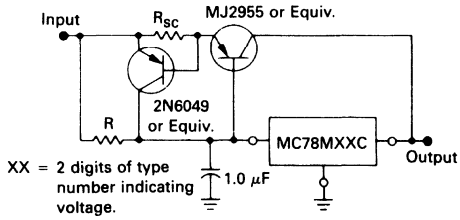
FIGURE 11 — CURRENT BOOST REGULATOR



XX = 2 digits of type number indicating voltage.

The MC78M00 series can be current boosted with a PNP transistor. The MJ2955 provides current to 5.0 amperes. Resistor R in conjunction with the V_{BE} of the PNP determines when the pass transistor begins conducting; this circuit is not short circuit proof. Input output differential voltage minimum is increased by V_{BE} of the pass transistor.

FIGURE 12 — CURRENT BOOST WITH SHORT-CIRCUIT PROTECTION



The circuit of Figure 7 can be modified to provide supply protection against short circuits by adding a short circuit sense resistor, R_{SC}, and an additional PNP transistor. The current sensing PNP must be able to handle the short-circuit current of the three-terminal regulator. Therefore, a two-ampere plastic power transistor is specified.

MOTOROLA

MC78T00 Series

Specifications and Applications Information

THREE-AMPERE POSITIVE VOLTAGE REGULATORS

This family of fixed voltage regulators are monolithic integrated circuits capable of driving loads in excess of 3.0 amperes. These three-terminal regulators employ internal current limiting, thermal shutdown, and safe-area compensation. Devices are available with improved specifications, including a 2% output voltage tolerance, on AC-suffix 5.0, 12 and 15 volt device types.

Although designed primarily as a fixed voltage regulator, these devices can be used with external components to obtain adjustable voltages and currents. This series of devices can be used with a series-pass transistor to supply up to 15 amperes at the nominal output voltage.

- Output Current in Excess of 3.0 Amperes
- Power Dissipation: 30 W (K-Suffix), 25 W (T-Suffix)
- No External Components Required
- Output Voltage Offered in 2% and 4% Tolerance*
- Thermal Regulation is Specified
- Internal Thermal Overload Protection
- Internal Short-Circuit Current Limiting
- Output Transistor Safe-Area Compensation

MAXIMUM RATINGS (T_A = +25°C unless otherwise noted.)

Rating	Symbol	Value	Unit
Input Voltage (5.0 V–12 V) (15 V)	V_{in}	35 40	Vdc
Power Dissipation and Thermal Characteristics Plastic Package (Note 1) T_A = +25°C Thermal Resistance, Junction to Air T_C = +25°C Thermal Resistance, Junction to Case Metal Package (Note 1) T_A = +25°C Thermal Resistance, Junction to Air T_C = +25°C Thermal Resistance, Junction to Case	 P_D $R_{\theta JA}$ P_D $R_{\theta JC}$ P_D $R_{\theta JA}$ P_D $R_{\theta JC}$	 Internally Limited 65 Internally Limited 2.5 Internally Limited 35 Internally Limited 2.5	 °C/W °C/W °C/W °C/W
Storage Junction Temperature Range	T_{stg}	−65 to +150	°C
Operating Junction Temperature Range MC78T00C, AC	T_J	0 to +150	°C

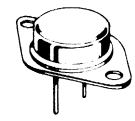
NOTE:
1. Although power dissipation is internally limited, specifications apply only for $P_D \leq P_{max}$.
   P_{max} = 30 W for K package P_{max} = 25 W for T package.

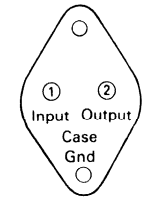
TYPE NO./VOLTAGE			
MC78T05	5.0 Volts	MC78T12	12 Volts
MC78T08	8.0 Volts	MC78T15	15 Volts

THREE-AMPERE POSITIVE FIXED VOLTAGE REGULATORS

SILICON MONOLITHIC INTEGRATED CIRCUIT

K SUFFIX
METAL PACKAGE
CASE 1-03

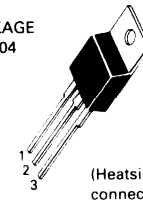




(Bottom View)

PIN 1. INPUT
2. OUTPUT
CASE GROUND

T SUFFIX
PLASTIC PACKAGE
CASE 221A-04



(Heatsink surface connected to Pin 2)

PIN 1. INPUT
2. GROUND
3. OUTPUT

ORDERING INFORMATION

Device	Output Voltage Tolerance	Tested Operating Junction Temp. Range	Package
MC78TXXCK MC78TXXACK	4% 2%*	0 to +125°C	Metal Power
MC78TXXCT MC78TXXACT	4% 2%*	0 to +125°C	Plastic Power
MC78TXXBT# MC78TXXABT#	4% 2%*	−40 to +125°C	Plastic Power

XX Indicates nominal voltage.
* 2% regulators are available in 5, 12 and 15 volt devices.
#Automotive temperature range selections are available with special test conditions and additional tests. Contact your local Motorola sales office for information.

MC78T05AC, C

ELECTRICAL CHARACTERISTICS (V_{in} = 10 V, I_O = 3.0 A, 0°C ≤ T_J ≤ 125°C, P_O ≤ P_{max} [Note 1], unless otherwise noted.)

Characteristic	Symbol	MC78T05AC			MC78T05C			Unit
		Min	Typ	Max	Min	Typ	Max	
Output Voltage (5.0 mA ≤ I_O ≤ 3.0 A, T_J = +25°C) (5.0 mA ≤ I_O ≤ 3.0 A; 5.0 mA ≤ I_O ≤ 2.0 A, 7.3 Vdc ≤ V_{in} ≤ 20 Vdc)	V_O	 4.9 4.8	 5.0 5.0	 5.1 5.2	 4.8 4.75	 5.0 5.0	 5.2 5.25	Vdc
Line Regulation (Note 2) (7.2 Vdc ≤ V_{in} ≤ 35 Vdc, I_O = 5.0 mA, T_J = +25°C; 7.2 Vdc ≤ V_{in} ≤ 35 Vdc, I_O = 1.0 A, T_J = +25°C; 8.0 Vdc ≤ V_{in} ≤ 12 Vdc, I_O = 3.0 A, T_J = +25°C; 7.5 Vdc ≤ V_{in} ≤ 20 Vdc, I_O = 1.0 A)	Reg_{line}	—	3.0	25	—	3.0	25	mV
Load Regulation (Note 2) (5.0 mA ≤ I_O ≤ 3.0 A, T_J = +25°C) (5.0 mA ≤ I_O ≤ 3.0 A)	Reg_{load}	 —	 10 15	 30 80	 —	 10 15	 30 80	mV
Thermal Regulation (Pulse = 10 ms, P = 20 W, T_A = +25°C)	Reg_{therm}	—	0.001	0.01	—	0.002	0.03	%V_O/W
Quiescent Current (5.0 mA ≤ I_O ≤ 3.0 A, T_J = +25°C) (5.0 mA ≤ I_O ≤ 3.0 A)	I_B	 —	 3.5 4.0	 5.0 6.0	 —	 3.5 4.0	 5.0 6.0	mA
Quiescent Current Change (7.2 Vdc ≤ V_{in} ≤ 35 Vdc, I_O = 5.0 mA, T_J = +25°C; 5.0 mA ≤ I_O ≤ 3.0 A, T_J = +25°C; 7.5 Vdc ≤ V_{in} ≤ 20 Vdc, I_O = 1.0 A)	ΔI_B	—	0.3	1.0	—	0.3	1.0	mA
Ripple Rejection (8.0 Vdc ≤ V_{in} ≤ 18 Vdc, f = 120 Hz, I_O = 2.0 A, T_J = 25°C)	RR	62	75	—	62	75	—	dB
Dropout Voltage (I_O = 3.0 A, T_J = +25°C)	V_{in}–V_O	—	2.2	2.5	—	2.2	2.5	Vdc
Output Noise Voltage (10 Hz ≤ f ≤ 100 kHz, T_J = +25°C)	V_n	—	10	—	—	10	—	μV/V_O
Output Resistance (f = 1.0 kHz)	R_O	—	2.0	—	—	2.0	—	mΩ
Short Circuit Current Limit (V_{in} = 35 Vdc, T_J = +25°C)	I_{SC}	—	1.5	—	—	1.5	—	A
Peak Output Current (T_J = +25°C)	I_{max}	—	5.0	—	—	5.0	—	A
Average Temperature Coefficient of Output Voltage (I_O = 5.0 mA)	TCV_O	—	0.2	—	—	0.2	—	mV/°C

NOTES:

1. Although power dissipation is internally limited, specifications apply only for P_O ≤ P_{max}.
   P_{max} = 30 W for K package P_{max} = 25 W for T package
2. Line and load regulation are specified at constant junction temperature. Changes in V_O due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

MC78T08C

ELECTRICAL CHARACTERISTICS (V_{in} = 13 V, I_O = 3.0 A, 0°C ≤ T_J ≤ 125°C, P_O ≤ P_{max} [Note 1], unless otherwise noted.)

Characteristic	Symbol	MC78T08C Min	MC78T08C Typ	MC78T08C Max	Unit
Output Voltage (5.0 mA ≤ I_O ≤ 3.0 A, T_J = +25°C) (5.0 mA ≤ I_O ≤ 3.0 A; 5.0 mA ≤ I_O ≤ 2.0 A, 10.4 Vdc ≤ V_{in} ≤ 23 Vdc)	V_O	 7.7 7.6	 8.0 8.0	 8.3 8.4	Vdc
Line Regulation (Note 2) (10.3 Vdc ≤ V_{in} ≤ 35 Vdc, I_O = 5.0 mA, T_J = +25°C; 10.3 Vdc ≤ V_{in} ≤ 35 Vdc, I_O = 1.0 A, T_J = +25°C; 11 Vdc ≤ V_{in} ≤ 17 Vdc, I_O = 3.0 A, T_J = +25°C; 10.7 Vdc ≤ V_{in} ≤ 23 Vdc, I_O = 1.0 A)	Reg_{line}	—	4.0	35	mV
Load Regulation (Note 2) (5.0 mA ≤ I_O ≤ 3.0 A, T_J = +25°C) (5.0 mA ≤ I_O ≤ 3.0 A)	Reg_{load}	 — —	 10 15	 30 80	mV
Thermal Regulation (Pulse = 10 ms, P = 20 W, T_A = +25°C)	Reg_{therm}	—	0.002	0.03	%V_O/W
Quiescent Current (5.0 mA ≤ I_O ≤ 3.0 A, T_J = +25°C) (5.0 mA ≤ I_O ≤ 3.0 A)	I_B	 — —	 3.5 4.0	 5.0 6.0	mA
Quiescent Current Change (10.3 Vdc ≤ V_{in} ≤ 35 Vdc, I_O = 5.0 mA, T_J = +25°C; 5.0 mA ≤ I_O ≤ 3.0 A, T_J = +25°C; 10.7 Vdc ≤ V_{in} ≤ 23 Vdc, I_O = 1.0 A)	ΔI_B	—	0.3	1.0	mA
Ripple Rejection (11 Vdc ≤ V_{in} ≤ 21 Vdc, f = 120 Hz, I_O = 2.0 A, T_J = 25°C)	RR	60	71	—	dB
Dropout Voltage (I_O = 3.0 A, T_J = +25°C)	V_{in}–V_O	—	2.2	2.5	Vdc
Output Noise Voltage (10 Hz ≤ f ≤ 100 kHz, T_J = +25°C)	V_n	—	10	—	μV/V_O
Output Resistance (f = 1.0 kHz)	R_O	—	2.0	—	mΩ
Short Circuit Current Limit (V_{in} = 35 Vdc, T_J = +25°C)	I_{SC}	—	1.5	—	A
Peak Output Current (T_J = +25°C)	I_{max}	—	5.0	—	A
Average Temperature Coefficient of Output Voltage (I_O = 5.0 mA)	TCV_O	—	0.3	—	mV/°C

NOTES:
1. Although power dissipation is internally limited, specifications apply only for P_O ≤ P_{max}.
   P_{max} = 30 W for K package P_{max} = 25 W for T package
2. Line and load regulation are specified at constant junction temperature. Changes in V_O due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

MC78T12AC, C

ELECTRICAL CHARACTERISTICS (V_{in} = 17 V, I_O = 3.0 A, 0°C ≤ T_J ≤ 125°C, P_O ≤ P_{max} [Note 1], unless otherwise noted.)

Characteristic	Symbol	MC78T12AC			MC78T12C			Unit
		Min	Typ	Max	Min	Typ	Max	
Output Voltage (5.0 mA ≤ I_O ≤ 3.0 A, T_J = +25°C) (5.0 mA ≤ I_O ≤ 3.0 A; 5.0 mA ≤ I_O ≤ 2.0 A, 14.5 Vdc ≤ V_{in} ≤ 27 Vdc)	V_O	 11.75 11.5	 12 12	 12.25 12.5	 11.5 11.4	 12 12	 12.5 12.6	Vdc
Line Regulation (Note 2) (14.5 Vdc ≤ V_{in} ≤ 35 Vdc, I_O = 5.0 mA, T_J = +25°C; 14.5 Vdc ≤ V_{in} ≤ 35 Vdc, I_O = 1.0 A, T_J = +25°C; 16 Vdc ≤ V_{in} ≤ 22 Vdc, I_O = 3.0 A, T_J = +25°C; 14.9 Vdc ≤ V_{in} ≤ 27 Vdc, I_O = 1.0 A)	Reg_{line}	—	6.0	45	—	6.0	45	mV
Load Regulation (Note 2) (5.0 mA ≤ I_O ≤ 3.0 A, T_J = +25°C) (5.0 mA ≤ I_O ≤ 3.0 A)	Reg_{load}	 — —	 10 15	 30 80	 — —	 10 15	 30 80	mV
Thermal Regulation (Pulse = 10 ms, P = 20 W, T_A = +25°C)	Reg_{therm}	—	0.001	0.01	—	0.002	0.03	%V_O/W
Quiescent Current (5.0 mA ≤ I_O ≤ 3.0 A, T_J = +25°C) (5.0 mA ≤ I_O ≤ 3.0 A)	I_B	 — —	 3.5 4.0	 5.0 6.0	 — —	 3.5 4.0	 5.0 6.0	mA
Quiescent Current Change (14.5 Vdc ≤ V_{in} ≤ 35 Vdc, I_O = 5.0 mA, T_J = +25°C; 5.0 mA ≤ I_O ≤ 3.0 A, T_J = +25°C; 14.9 Vdc ≤ V_{in} ≤ 27 Vdc, I_O = 1.0 A)	ΔI_B	—	0.3	1.0	—	0.3	1.0	mA
Ripple Rejection (15 Vdc ≤ V_{in} ≤ 25 Vdc, f = 120 Hz, I_O = 2.0 A, T_J = 25°C)	RR	57	67	—	57	67	—	dB
Dropout Voltage (I_O = 3.0 A, T_J = +25°C)	V_{in}–V_O	—	2.2	2.5	—	2.2	2.5	Vdc
Output Noise Voltage (10 Hz ≤ f ≤ 100 kHz, T_J = +25°C)	V_n	—	10	—	—	10	—	μV/V_O
Output Resistance (f = 1.0 kHz)	R_O	—	2.0	—	—	2.0	—	mΩ
Short Circuit Current Limit (V_{in} = 35 Vdc, T_J = +25°C)	I_{SC}	—	1.5	—	—	1.5	—	A
Peak Output Current (T_J = +25°C)	I_{max}	—	5.0	—	—	5.0	—	A
Average Temperature Coefficient of Output Voltage (I_O = 5.0 mA)	TCV_O	—	0.5	—	—	0.5	—	mV/°C

NOTES:

1. Although power dissipation is internally limited, specifications apply only for P_O ≤ P_{max}.
   P_{max} = 30 W for K package P_{max} = 25 W for T package
2. Line and load regulation are specified at constant junction temperature. Changes in V_O due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

MC78T15AC, C

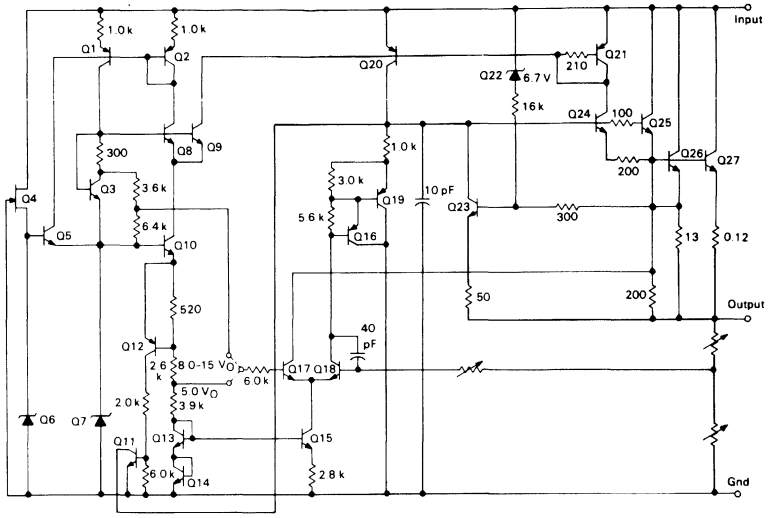
ELECTRICAL CHARACTERISTICS (V_{in} = 20 V, I_O = 3.0 A, 0°C ≤ T_J ≤ 125°C, P_O ≤ P_{max} [Note 1], unless otherwise noted.)

Characteristic	Symbol	MC78T15AC			MC78T15C			Unit
		Min	Typ	Max	Min	Typ	Max	
Output Voltage (5.0 mA ≤ I_O ≤ 3.0 A, T_J = +25°C) (5.0 mA ≤ I_O ≤ 3.0 A; 5.0 mA ≤ I_O ≤ 2.0 A, 17.5 Vdc ≤ V_{in} ≤ 30 Vdc)	V_O	 14.7 14.4	 15 15	 15.3 15.6	 14.4 14.25	 15 15	 15.6 15.75	Vdc
Line Regulation (Note 2) (17.6 Vdc ≤ V_{in} ≤ 40 Vdc, I_O = 5.0 mA, T_J = +25°C; 17.6 Vdc ≤ V_{in} ≤ 40 Vdc, I_O = 1.0 A, T_J = +25°C; 20 Vdc ≤ V_{in} ≤ 26 Vdc, I_O = 3.0 A, T_J = +25°C; 18 Vdc ≤ V_{in} ≤ 30 Vdc, I_O = 1.0 A)	Reg_{line}	—	7.5	55	—	7.5	55	mV
Load Regulation (Note 2) (5.0 mA ≤ I_O ≤ 3.0 A, T_J = +25°C) (5.0 mA ≤ I_O ≤ 3.0 A)	Reg_{load}	 — —	 10 15	 30 80	 — —	 10 15	 30 80	mV
Thermal Regulation (Pulse = 10 ms, P = 20 W, T_A = +25°C)	Reg_{therm}	—	0.001	0.01	—	0.002	0.03	%V_O/W
Quiescent Current (5.0 mA ≤ I_O ≤ 3.0 A, T_J = +25°C) (5.0 mA ≤ I_O ≤ 3.0 A)	I_B	 — —	 3.5 4.0	 5.0 6.0	 — —	 3.5 4.0	 5.0 6.0	mA
Quiescent Current Change (17.6 Vdc ≤ V_{in} ≤ 40 Vdc, I_O = 5.0 mA, T_J = +25°C; 5.0 mA ≤ I_O ≤ 3.0 A, T_J = +25°C; 18 Vdc ≤ V_{in} ≤ 30 Vdc, I_O = 1.0 A)	ΔI_B	—	0.3	1.0	—	0.3	1.0	mA
Ripple Rejection (18.5 Vdc ≤ V_{in} ≤ 28.5 Vdc, f = 120 Hz, I_O = 2.0 A, T_J = 25°C)	RR	55	65	—	55	65	—	dB
Dropout Voltage (I_O = 3.0 A, T_J = +25°C)	V_{in}–V_O	—	2.2	2.5	—	2.2	2.5	Vdc
Output Noise Voltage (10 Hz ≤ f ≤ 100 kHz, T_J = +25°C)	V_n	—	10	—	—	10	—	μV/V_O
Output Resistance (f = 1.0 kHz)	R_O	—	2.0	—	—	2.0	—	mΩ
Short Circuit Current Limit (V_{in} = 40 Vdc, T_J = +25°C)	I_{SC}	—	1.0	—	—	1.0	—	A
Peak Output Current (T_J = +25°C)	I_{max}	—	5.0	—	—	5.0	—	A
Average Temperature Coefficient of Output Voltage (I_O = 5.0 mA)	TCV_O	—	0.6	—	—	0.6	—	mV/°C

NOTES:

1. Although power dissipation is internally limited, specifications apply only for P_O ≤ P_{max}.
   P_{max} = 30 W for K package P_{max} = 25 W for T package
2. Line and load regulation are specified at constant junction temperature. Changes in V_O due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

SCHEMATIC DIAGRAM



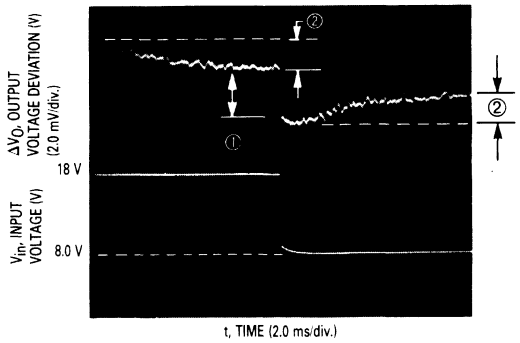
VOLTAGE REGULATOR PERFORMANCE

The performance of a voltage regulator is specified by its immunity to changes in load, input voltage, power dissipation, and temperature. Line and load regulation are tested with a pulse of short duration (< 100 μs) and are strictly a function of electrical gain. However, pulse widths of longer duration (> 1.0 ms) are sufficient to affect temperature gradients across the die. These temperature gradients can cause a change in the output voltage, in addition to changes caused by line and load regulation. Longer pulse widths and thermal gradients make it desirable to specify thermal regulation.

Thermal regulation is defined as the change in output voltage caused by a change in dissipated power for a specified time, and is expressed as a percentage output voltage change per watt. The change in dissipated power can be caused by a change in either the input voltage or the load current. Thermal regulation is a function of I.C. layout and die attach techniques, and usually occurs within 10 ms of a change in power dissipation. After 10 ms, additional changes in the output voltage are due to the temperature coefficient of the device.

Figure 1 shows the line and thermal regulation response of a typical MC78T05AC to a 20 watt input pulse. The variation of the output voltage due to line regulation is labeled ① and the thermal regulation component is labeled ②. Figure 2 shows the load and thermal regulation response of a typical MC78T05AC to a 20 watt load pulse. The output voltage variation due to load regulation is labeled ① and the thermal regulation component is labeled ②.

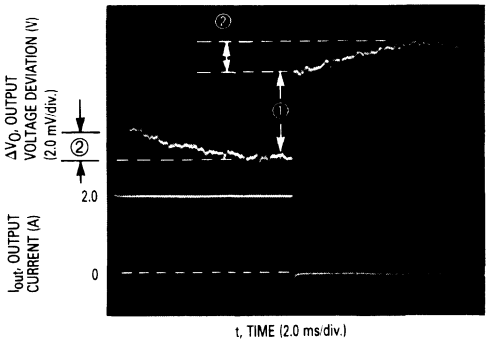
FIGURE 1 — LINE AND THERMAL REGULATION



MC78T05AC
V_O = 5.0 V
V_{in} = 8.0 V → 18 V → 8.0 V
I_{out} = 2.0 A

① = Reg_{line} = 2.4 mV
② = Reg_{therm} = 0.0015%V_O/W

FIGURE 2 — LOAD AND THERMAL REGULATION



MC78T05AC
V_O = 5.0 V
V_{in} = 15
I_{out} = 0 A → 2.0 A → 0 A

① = Reg_{load} = 4.4 mV
② = Reg_{therm} = 0.0015%V_O/W

FIGURE 3 — TEMPERATURE STABILITY

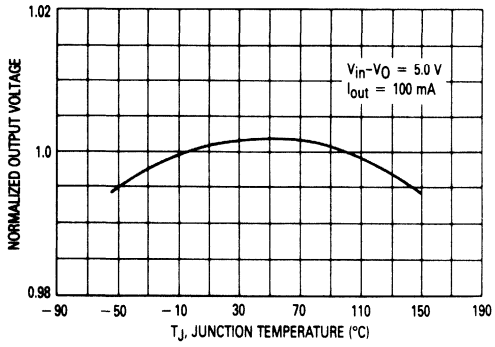


FIGURE 4 — OUTPUT IMPEDANCE

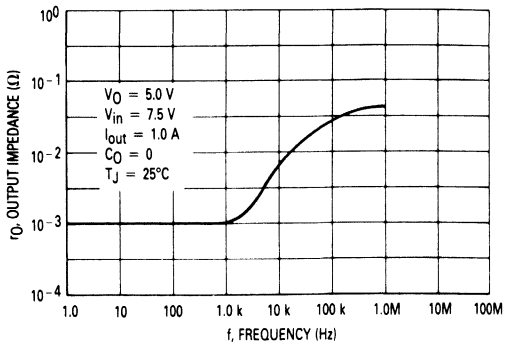


FIGURE 5 — RIPPLE REJECTION versus FREQUENCY

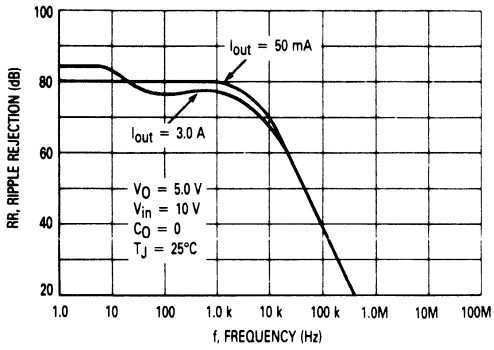


FIGURE 6 — RIPPLE REJECTION versus OUTPUT CURRENT

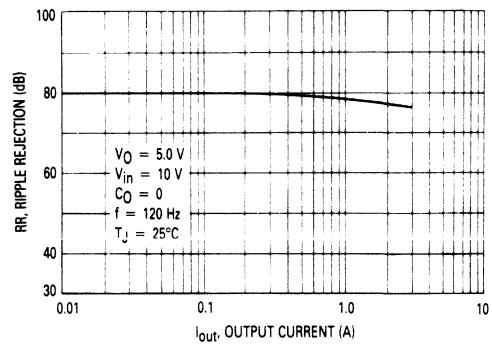


FIGURE 7 — QUIESCENT CURRENT versus INPUT VOLTAGE

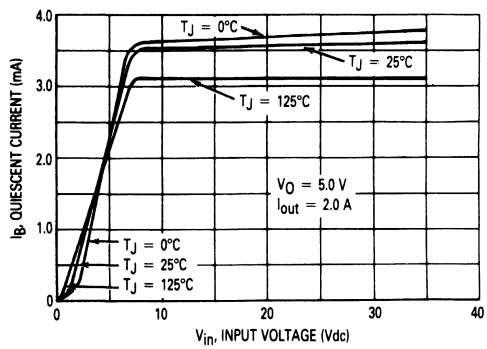


FIGURE 8 — QUIESCENT CURRENT versus OUTPUT CURRENT

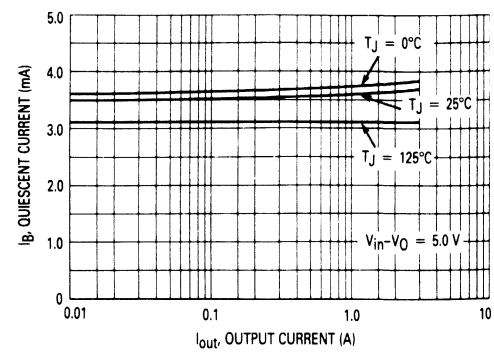


FIGURE 9 — DROPOUT VOLTAGE

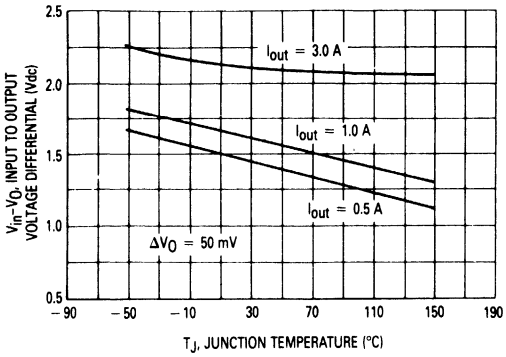


FIGURE 10 — PEAK OUTPUT CURRENT

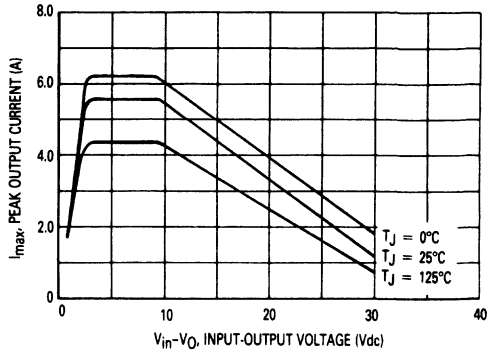


FIGURE 11 — LINE TRANSIENT RESPONSE

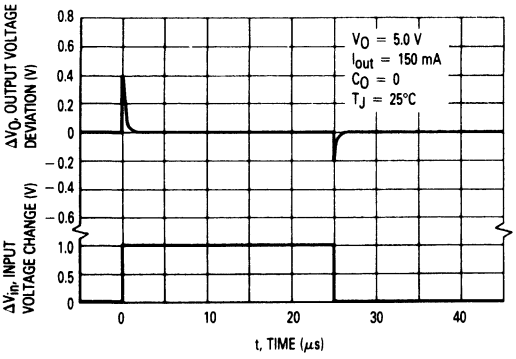


FIGURE 12 — LOAD TRANSIENT RESPONSE

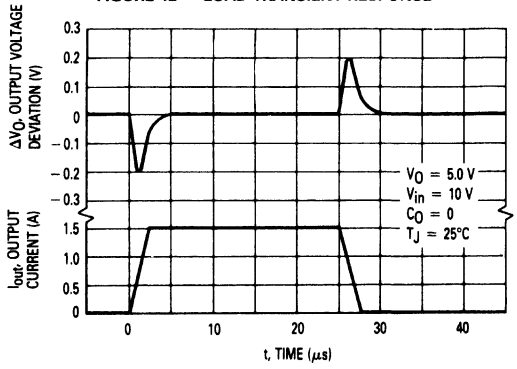


FIGURE 13 — MAXIMUM AVERAGE POWER DISSIPATION FOR MC78T00CK, ACK

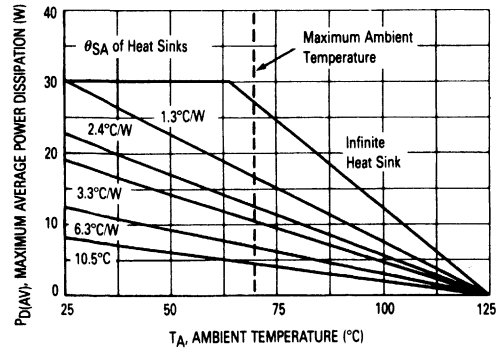
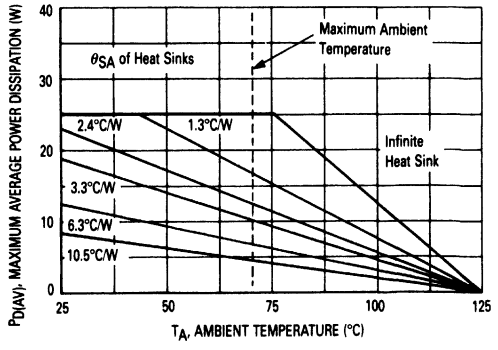


FIGURE 14 — MAXIMUM AVERAGE POWER DISSIPATION FOR MC78T00CT, ACT



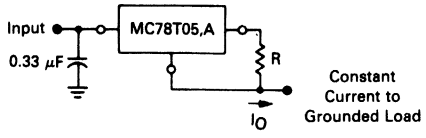
APPLICATIONS INFORMATION

DESIGN CONSIDERATIONS

The MC78T00,A Series of fixed voltage regulators are designed with Thermal Overload Protection that shuts down the circuit when subjected to an excessive power overload condition, Internal Short-Circuit Protection that limits the maximum current the circuit will pass, and Output Transistor Safe-Area Compensation that reduces the output short circuit current as the voltage across the pass transistor is increased.

In many low current applications, compensation capacitors are not required. However, it is recommended that the regulator input be bypassed with a capacitor if the regulator is connected to the power supply filter with long wire lengths, or if the output load capacitance is large. An input bypass capacitor should be selected to provide good high frequency characteristics to insure stable operation under all load conditions. A 0.33 μF or larger tantalum, mylar, or other capacitor having low internal impedance at high frequencies should be chosen. The bypass capacitor should be mounted with the shortest possible leads directly across the regulator's input terminals. Normally good construction techniques should be used to minimize ground loops and lead resistance drops since the regulator has no external sense lead.

FIGURE 15 — CURRENT REGULATOR



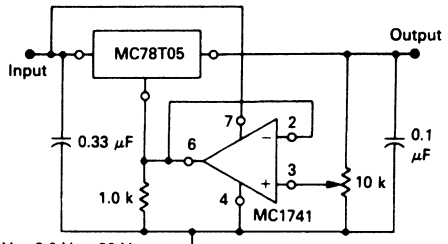
The MC78T05 regulator can also be used as a current source when connected as above. In order to minimize dissipation, the MC78T05 is chosen in this application. Resistor R determines the current as follows:

$$I_O = \frac{5.0\ V}{R} + I_B$$

$\Delta I_B \cong 0.7$ mA over line, load and temperature changes
$I_B \cong 3.5$ mA

For example, a 2-ampere current source would require R to be a 2.5 ohm, 15 W resistor and the output voltage compliance would be the input voltage less 7.5 volts.

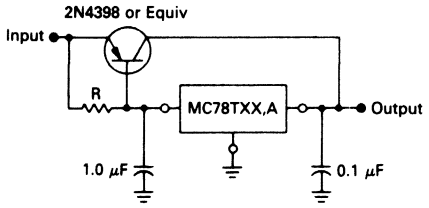
FIGURE 16 — ADJUSTABLE OUTPUT REGULATOR



V_O, 8.0 V to 20 V
$V_{in}-V_O \geq 2.5$ V

The addition of an operational amplifier allows adjustment to higher or intermediate values while retaining regulation characteristics. The minimum voltage obtainable with this arrangement is 3.0 volts greater than the regulator voltage.

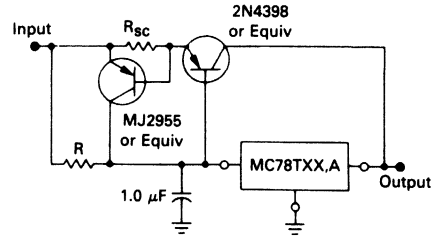
FIGURE 17 — CURRENT BOOST REGULATOR



XX = 2 digits of type number indicating voltage.

The MC78T00,A series can be current boosted with a PNP transistor. The 2N4398 provides current to 15 amperes. Resistor R in conjunction with the V_{BE} of the PNP determines when the pass transistor begins conducting; this circuit is not short-circuit proof. Input-output differential voltage minimum is increased by the V_{BE} of the pass transistor.

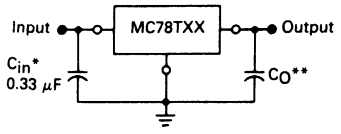
FIGURE 18 — CURRENT BOOST WITH SHORT-CIRCUIT PROTECTION



XX = 2 digits of type number indicating voltage.

The circuit of Figure 17 can be modified to provide supply protection against short circuits by adding a short-circuit sense resistor, R_{SC}, and an additional PNP transistor. The current sensing PNP must be able to handle the short-circuit current of the three-terminal regulator. Therefore, an eight-ampere power transistor is specified.

STANDARD APPLICATION



A common ground is required between the input and the output voltages. The input voltage must remain typically 2.2 V above the output voltage even during the low point on the input ripple voltage.

XX = these two digits of the type number indicate voltage.

* = C_{in} is required if regulator is located an appreciable distance from power supply filter. (See Applications Information for details.)

** = C_O is not needed for stability; however, it does improve transient response.

MOTOROLA

MC7900 Series

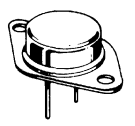
THREE-TERMINAL NEGATIVE VOLTAGE REGULATORS

The MC7900 Series of fixed output negative voltage regulators are intended as complements to the popular MC7800 Series devices. These negative regulators are available in the same seven-voltage options as the MC7800 devices. In addition, one extra voltage option commonly employed in MECL systems is also available in the negative MC7900 Series.

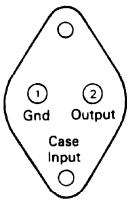
Available in fixed output voltage options from −5.0 to −24 volts, these regulators employ current limiting, thermal shutdown, and safe-area compensation — making them remarkably rugged under most operating conditions. With adequate heatsinking they can deliver output currents in excess of 1.0 ampere.

- No External Components Required
- Internal Thermal Overload Protection
- Internal Short-Circuit Current Limiting
- Output Transistor Safe-Area Compensation
- Available in 2% Voltage Tolerance (See Ordering Information)

THREE-TERMINAL NEGATIVE FIXED VOLTAGE REGULATORS



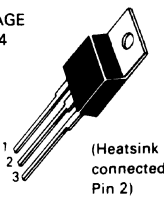
K SUFFIX
METAL PACKAGE
CASE 1-03



(Bottom View)

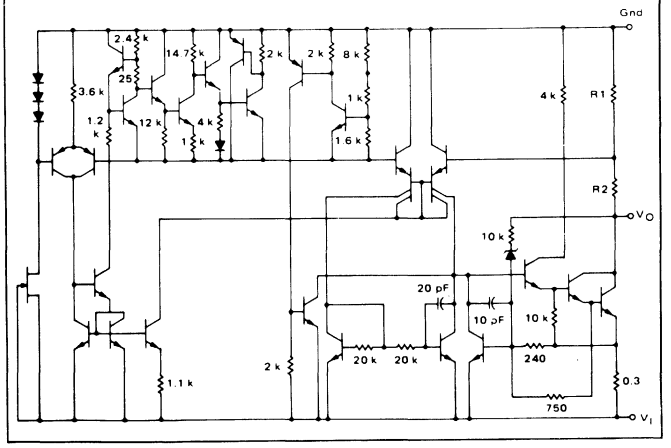
T SUFFIX
PLASTIC PACKAGE
CASE 221A-04

PIN 1. GROUND
2. INPUT
3. OUTPUT

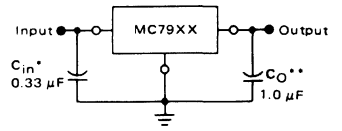


(Heatsink surface connected to Pin 2)

SCHEMATIC DIAGRAM



STANDARD APPLICATION



A common ground is required between the input and the output voltages. The input voltage must remain typically 2.0 V more negative even during the high point on the input ripple voltage.

XX = these two digits of the type number indicate voltage.

* = C_{in} is required if regulator is located an appreciable distance from power supply filter.

** = C_O improves stability and transient response.

ORDERING INFORMATION

Device	Output Voltage Tolerance	Tested Operating Junction Temp. Range	Package
MC79XXCK	4%	T_J = 0°C to +125°C	Metal Power**
MC79XXACK*	2%		
MC79XXCT	4%		Plastic Power
MC79XXACT*	2%		
MC79XXBT#	4%	T_J = −40°C to +125°C	

XX indicates nominal voltage.

*2% output voltage tolerance available in 5, 12 and 15 volt devices.

**Metal power package available in 5, 12 and 15 volt devices.

#Automotive temperature range selections are available with special test conditions and additional tests in 5, 12 and 15 volt devices. Contact your local Motorola sales office for information.

DEVICE TYPE/NOMINAL OUTPUT VOLTAGE			
MC7905	5.0 Volts	MC7912	12 Volts
MC7905.2	5.2 Volts	MC7915	15 Volts
MC7906	6.0 Volts	MC7918	18 Volts
MC7908	8.0 Volts	MC7924	24 Volts

MAXIMUM RATINGS (T_A = +25°C unless otherwise noted.)

Rating	Symbol	Value	Unit
Input Voltage (-5.0 V ≥ V_o ≥ -18 V) (24 V)	V_I	-35 -40	Vdc
Power Dissipation Plastic Package T_A = +25°C Derate above T_A = +25°C T_C = +25°C Derate above T_C = +95°C (See Figure 1) Metal Package T_A = +25°C Derate above T_A = +25°C T_C = +25°C Derate above T_C = +65°C	 P_D $1/R_{\theta JA}$ P_D $1/R_{\theta JC}$ P_D $1/R_{\theta JA}$ P_D $1/R_{\theta JC}$	 Internally Limited 15.4 Internally Limited 200 Internally Limited 22.2 Internally Limited 182	 Watts mW/°C Watts mW/°C Watts mW/°C Watts mW/°C
Storage Junction Temperature Range	T_{stg}	-65 to +150	°C
Junction Temperature Range	T_J	0 to +150	°C

THERMAL CHARACTERISTICS

Characteristic		Symbol	Max	Unit
Thermal Resistance, Junction to Ambient	— Plastic Package — Metal Package	$R_{\theta JA}$	65 45	°C/W
Thermal Resistance, Junction to Case	— Plastic Package — Metal Package	$R_{\theta JC}$	5.0 5.5	°C/W

MC7905C ELECTRICAL CHARACTERISTICS (V_I = -10 V, I_O = 500 mA, 0°C < T_J < +125°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Output Voltage (T_J = +25°C)	V_O	-4.8	-5.0	-5.2	Vdc
Line Regulation (Note 1) (T_J = +25°C, I_O = 100 mA) -7.0 Vdc ≥ V_I ≥ -25 Vdc -8.0 Vdc ≥ V_I ≥ -12 Vdc (T_J = +25°C, I_O = 500 mA) -7.0 Vdc ≥ V_I ≥ -25 Vdc -8.0 Vdc ≥ V_I ≥ -12 Vdc	Reg_{line}	 — — — —	 7.0 2.0 35 8.0	 50 25 100 50	mV
Load Regulation (T_J = +25°C) (Note 1) 5.0 mA ≤ I_O ≤ 1.5 A 250 mA ≤ I_O ≤ 750 mA	Reg_{load}	 — —	 11 4.0	 100 50	mV
Output Voltage -7.0 Vdc ≥ V_I ≥ -20 Vdc, 5.0 mA ≤ I_O ≤ 1.0 A, P ≤ 15 W	V_O	-4.75	--	-5.25	Vdc
Input Bias Current (T_J = +25°C)	I_{IB}	—	4.3	8.0	mA
Input Bias Current Change -7.0 Vdc ≥ V_I ≥ -25 Vdc 5.0 mA ≤ I_O ≤ 1.5 A	ΔI_{IB}	 — —	 — —	 1.3 0.5	mA
Output Noise Voltage (T_A = +25°C, 10 Hz ≤ f ≤ 100 kHz)	e_{on}	—	40	—	μV
Ripple Rejection (I_O = 20 mA, f = 120 Hz)	RR	—	70	—	dB
Dropout Voltage I_O = 1.0 A, T_J = +25°C	V_I-V_O	—	2.0	—	Vdc
Average Temperature Coefficient of Output Voltage I_O = 5.0 mA, 0°C ≤ T_J ≤ +125°C	$\Delta V_O/\Delta T$	—	-1.0	—	mV/°C

Note:
1. Load and line regulation are specified at constant junction temperature. Changes in V_O due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

MC7905AC ELECTRICAL CHARACTERISTICS (V_I = -10 V, I_O = 500 mA, 0°C < T_J < +125°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Output Voltage (T_J = +25°C)	V_O	-4.9	-5.0	-5.1	Vdc
Line Regulation (Note 1) -8.0 Vdc ≥ V_I ≥ -12 Vdc; I_O = 1.0 A, T_J = 25°C -8.0 Vdc ≥ V_I ≥ -12 Vdc; I_O = 1.0 A -7.5 Vdc ≥ V_I ≥ -25 Vdc; I_O = 500 mA -7.0 Vdc ≥ V_I ≥ -20 Vdc; I_O = 1.0 A, T_J = +25°C	Reg_{line}	 — — — —	 2.0 7.0 7.0 6.0	 25 50 50 50	mV
Load Regulation (Note 1) 5.0 mA ≤ I_O ≤ 1.5 A, T_J = +25°C 250 mA ≤ I_O ≤ 750 mA 5.0 mA ≤ I_O ≤ 1.0 A	Reg_{load}	 — — —	 11 4.0 9.0	 .100 50 100	mV
Output Voltage -7.5 Vdc ≥ V_I ≥ -20 Vdc, 5.0 mA ≤ I_O ≤ 1.0 A, P ≤ 15 W	V_O	-4.80	—	-5.20	Vdc
Input Bias Current	I_{IB}	—	4.4	8.0	mA
Input Bias Current Change -7.5 Vdc ≥ V_I ≥ -25 Vdc 5.0 mA ≤ I_O ≤ 1.0 A 5.0 mA ≤ I_O ≤ 1.5 A, T_J = 25°C	ΔI_{IB}	 — — —	 — — —	 1.3 0.5 0.5	mA
Output Noise Voltage (T_A = +25°C, 10 Hz ≤ f ≤ 100 kHz)	e_{on}	—	40	—	μV
Ripple Rejection (I_O = 20 mA, f = 120 Hz)	RR	—	70	—	dB
Dropout Voltage I_O = 1.0 A, T_J = +25°C	V_I-V_O	—	2.0	—	Vdc
Average Temperature Coefficient of Output Voltage I_O = 5.0 mA, 0°C ≤ T_J ≤ +125°C	$\Delta V_O/\Delta T$	—	-1.0	—	mV/°C

MC7905.2C ELECTRICAL CHARACTERISTICS (V_I = -10 V, I_O = 500 mA, 0°C < T_J < +125°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Output Voltage (T_J = +25°C)	V_O	-5.0	-5.2	-5.4	Vdc
Line Regulation (Note 1) (T_J = +25°C, I_O = 100 mA) -7.2 Vdc ≥ V_I ≥ -25 Vdc -8.0 Vdc ≥ V_I ≥ -12 Vdc (T_J = +25°C, I_O = 500 mA) -7.2 Vdc ≥ V_I ≥ -25 Vdc -8.0 Vdc ≥ V_I ≥ -12 Vdc	Reg_{line}	 — — — —	 8.0 2.2 37 8.5	 52 27 105 52	mV
Load Regulation (T_J = +25°C) (Note 1) 5.0 mA ≤ I_O ≤ 1.5 A 250 mA ≤ I_O ≤ 750 mA	Reg_{load}	 — —	 12 4.5	 105 52	mV
Output Voltage -7.2 Vdc ≥ V_I ≥ -20 Vdc, 5.0 mA ≤ I_O ≤ 1.0 A, P ≤ 15 W	V_O	-4.95	—	-5.45	Vdc
Input Bias Current (T_J = +25°C)	I_{IB}	—	4.3	8.0	mA
Input Bias Current Change -7.2 Vdc ≥ V_I ≥ -25 Vdc 5.0 mA ≤ I_O ≤ 1.5 A	ΔI_{IB}	 — —	 — —	 1.3 0.5	mA
Output Noise Voltage (T_A = +25°C 10 Hz ≤ f ≤ 100 kHz)	e_{on}	—	42	—	μV
Ripple Rejection (I_O = 20 mA, f = 120 Hz)	RR	—	68	—	dB
Dropout Voltage I_O = 1.0 A, T_J = +25°C	V_I-V_O	—	2.0	—	Vdc
Average Temperature Coefficient of Output Voltage I_O = 5.0 mA, 0°C ≤ T_J ≤ +125°C	$\Delta V_O/\Delta T$	—	-1.0	—	mV/°C

Note:
1. Load and line regulation are specified at constant junction temperature. Changes in V_O due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

MC7906C ELECTRICAL CHARACTERISTICS (V_I = -11 V, I_O = 500 mA, 0°C < T_J < +125°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Output Voltage (T_J = +25°C)	V_O	-5.75	-6.0	-6.25	Vdc
Line Regulation (Note 1) (T_J = +25°C, I_O = 100 mA) -8.0 Vdc ≥ V_I ≥ -25 Vdc -9.0 Vdc ≥ V_I ≥ -13 Vdc (T_J = +25°C, I_O = 500 mA) -8.0 Vdc ≥ V_I ≥ -25 Vdc -9.0 Vdc ≥ V_I ≥ -13 Vdc	Reg_{line}	 — — — —	 9.0 3.0 43 10	 60 30 120 60	mV
Load Regulation (T_J = +25°C) (Note 1) 5.0 mA ≤ I_O ≤ 1.5 A 250 mA ≤ I_O ≤ 750 mA	Reg_{load}	 — —	 13 5.0	 120 60	mV
Output Voltage -8.0 Vdc ≥ V_I ≥ -21 Vdc, 5.0 mA ≤ I_O ≤ 1.0 A, P ≤ 15 W	V_O	-5.7	—	-6.3	Vdc
Input Bias Current (T_J = +25°C)	I_{IB}	—	4.3	8.0	mA
Input Bias Current Change -8.0 Vdc ≥ V_I ≥ -25 Vdc 5.0 mA ≤ I_O ≤ 1.5 A	ΔI_{IB}	 — —	 — —	 1.3 0.5	mA
Output Noise Voltage (T_A = +25°C, 10 Hz ≤ f ≤ 100 kHz)	e_{on}	—	45	—	μV
Ripple Rejection (I_O = 20 mA, f = 120 Hz)	RR	—	65	—	dB
Dropout Voltage I_O = 1.0 A, T_J = +25°C	V_I-V_O	—	2.0	—	Vdc
Average Temperature Coefficient of Output Voltage I_O = 5.0 mA, 0°C ≤ T_J ≤ +125°C	$\Delta V_O/\Delta T$	—	-1.0	—	mV/°C

MC7908C ELECTRICAL CHARACTERISTICS (V_I = -14 V, I_O = 500 mA, 0°C < T_J < +125°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Output Voltage (T_J = +25°C)	V_O	-7.7	-8.0	-8.3	Vdc
Line Regulation (Note 1) (T_J = +25°C, I_O = 100 mA) -10.5 Vdc ≥ V_I ≥ -25 Vdc -11 Vdc ≥ V_I ≥ -17 Vdc (T_J = +25°C, I_O = 500 mA) -10.5 Vdc ≥ V_I ≥ -25 Vdc -11 Vdc ≥ V_I ≥ -17 Vdc	Reg_{line}	 — — — —	 12 5.0 50 22	 80 40 160 80	mV
Load Regulation (T_J = +25°C) (Note 1) 5.0 mA ≤ I_O ≤ 1.5 A 250 mA ≤ I_O ≤ 750 mA	Reg_{load}	 — —	 26 9.0	 160 80	mV
Output Voltage -10.5 Vdc ≥ V_I ≥ -23 Vdc, 5.0 mA ≤ I_O ≤ 1.0 A, P ≤ 15 W	V_O	-7.6	—	-8.4	Vdc
Input Bias Current (T_J = +25°C)	I_{IB}	—	4.3	8.0	mA
Input Bias Current Change -10.5 Vdc ≥ V_I ≥ -25 Vdc 5.0 mA ≤ I_O ≤ 1.5 A	ΔI_{IB}	 — —	 — —	 1.0 0.5	mA
Output Noise Voltage (T_A = +25°C, 10 Hz ≤ f ≤ 100 kHz)	e_{on}	—	52	—	μV
Ripple Rejection (I_O = 20 mA, f = 120 Hz)	RR	—	62	—	dB
Dropout Voltage I_O = 1.0 A, T_J = +25°C	V_I-V_O	—	2.0	—	Vdc
Average Temperature Coefficient of Output Voltage I_O = 5.0 mA, 0°C ≤ T_J ≤ +125°C	$\Delta V_O/\Delta T$	—	-1.0	—	mV/°C

Note:
1. Load and line regulation are specified at constant junction temperature. Changes in V_O due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

MC7915C ELECTRICAL CHARACTERISTICS (V_I = -23 V, I_O = 500 mA, 0°C < T_J < +125°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Output Voltage (T_J = +25°C)	V_O	-14.4	-15	-15.6	Vdc
Line Regulation (Note 1)	Reg_{line}				mV
(T_J = +25°C, I_O = 100 mA)					
-17.5 Vdc ≥ V_I ≥ -30 Vdc		—	14	150	
-20 Vdc ≥ V_I ≥ -26 Vdc		—	6.0	75	
(T_J = +25°C, I_O = 500 mA)					
-17.5 Vdc ≥ V_I ≥ -30 Vdc		—	57	300	
-20 Vdc ≥ V_I ≥ -26 Vdc		—	27	150	
Load Regulation (T_J = +25°C) (Note 1)	Reg_{load}				mV
5.0 mA ≤ I_O ≤ 1.5 A		—	68	300	
250 mA ≤ I_O ≤ 750 mA		—	25	150	
Output Voltage	V_O	-14 25	—	-15.75	Vdc
-17.5 Vdc ≥ V_I ≥ -30 Vdc, 5.0 mA ≤ I_O ≤ 1.0 A, P ≤ 15 W					
Input Bias Current (T_J = +25°C)	I_{IB}	—	4.4	8.0	mA
Input Bias Current Change	ΔI_{IB}				mA
-17.5 Vdc ≥ V_I ≥ -30 Vdc		—	—	1.0	
5.0 mA ≤ I_O ≤ 1.5 A		—	—	0.5	
Output Noise Voltage (T_A = +25°C, 10 Hz ≤ f ≤ 100 kHz)	e_{on}	—	90	—	μV
Ripple Rejection (I_O = 20 mA, f = 120 Hz)	RR	—	60	—	dB
Dropout Voltage	V_I-V_O	—	2.0	—	Vdc
I_O = 1.0 A, T_J = +25°C					
Average Temperature Coefficient of Output Voltage	$\Delta V_O/\Delta T$	—	-1.0	—	mV/°C
I_O = 5.0 mA, 0°C ≤ T_J ≤ +125°C					

MC7915AC ELECTRICAL CHARACTERISTICS (V_I = -23 V, I_O = 500 mA, 0°C < T_J < +125°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Output Voltage (T_J = +25°C)	V_O	-14.7	-15	-15.3	Vdc
Line Regulation (Note 1)	Reg_{line}				mV
-20 Vdc ≥ V_I ≥ -26 Vdc; I_O = 1.0 A, T_J = 25°C		—	27	75	
-20 Vdc ≥ V_I ≥ -26 Vdc; I_O = 1.0 A,		—	57	150	
-17.9 Vdc ≥ V_I ≥ -30 Vdc; I_O = 500 mA		—	57	150	
-17.5 Vdc ≥ V_I ≥ -30 Vdc; I_O = 1.0 A, T_J = 25°C		—	57	150	
Load Regulation (Note 1)	Reg_{load}				mV
5.0 mA ≤ I_O ≤ 1.5 A, T_J = 25°C		—	68	150	
250 mA ≤ I_O ≤ 750 mA		—	25	75	
5.0 mA ≤ I_O ≤ 1.0 A		—	40	150	
Output Voltage	V_O	-14.4	—	-15.6	Vdc
-17.9 Vdc ≥ V_I ≥ -30 Vdc, 5.0 mA ≤ I_O ≤ 1.0 A, P ≤ 15 W					
Input Bias Current	I_{IB}	—	4.4	8.0	mA
Input Bias Current Change	ΔI_{IB}				mA
-17.5 Vdc ≥ V_I ≥ -30 Vdc		—	—	0.8	
5.0 mA ≤ I_O ≤ 1.0 A		—	—	0.5	
5.0 mA ≤ I_O ≤ 1.5 A, T_J = 25°C		—	—	0.5	
Output Noise Voltage (T_A = +25°C, 10 Hz ≤ f ≤ 100 kHz)	e_{on}	—	90	—	μV
Ripple Rejection (I_O = 20 mA, f = 120 Hz)	RR	—	60	—	dB
Dropout Voltage	V_I-V_O	—	2.0	—	Vdc
I_O = 1.0 A, T_J = +25°C					
Average Temperature Coefficient of Output Voltage	$\Delta V_O/\Delta T$	—	-1.0	—	mV/°C
I_O = 5.0 mA, 0°C ≤ T_J ≤ +125°C					

Note:
1. Load and line regulation are specified at constant junction temperature. Changes in V_O due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

MC7912C ELECTRICAL CHARACTERISTICS (V_I = -19 V, I_O = 500 mA, 0°C < T_J < +125°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Output Voltage (T_J = +25°C)	V_O	-11.5	-12	-12.5	Vdc
Line Regulation (Note 1) (T_J = +25°C, I_O = 100 mA) -14.5 Vdc ≥ V_I ≥ -30 Vdc -16 Vdc ≥ V_I ≥ -22 Vdc (T_J = +25°C, I_O = 500 mA) -14.5 Vdc ≥ V_I ≥ -30 Vdc -16 Vdc ≥ V_I ≥ -22 Vdc	Reg_{line}	 — — — —	 13 6.0 55 24	 120 60 240 120	mV
Load Regulation (T_J = +25°C) (Note 1) 5.0 mA ≤ I_O ≤ 1.5 A 250 mA ≤ I_O ≤ 750 mA	Reg_{load}	 — —	 46 17	 240 120	mV
Output Voltage -14.5 Vdc ≥ V_I ≥ -27 Vdc, 5.0 mA ≤ I_O ≤ 1.0 A, P ≤ 15 W	V_O	-11.4	—	-12.6	Vdc
Input Bias Current (T_J = +25°C)	I_{IB}	—	4.4	8.0	mA
Input Bias Current Change -14.5 Vdc ≥ V_I ≥ -30 Vdc 5.0 mA ≤ I_O ≤ 1.5 A	ΔI_{IB}	 — —	 — —	 1.0 0.5	mA
Output Noise Voltage (T_A = +25°C, 10 Hz ≤ f ≤ 100 kHz)	e_{on}	—	75	—	μV
Ripple Rejection (I_O = 20 mA, f = 120 Hz)	RR	—	61	—	dB
Dropout Voltage I_O = 1.0 A, T_J = +25°C	V_I-V_O	—	2.0	—	Vdc
Average Temperature Coefficient of Output Voltage I_O = 5.0 mA, 0°C ≤ T_J ≤ +125°C	$\Delta V_O/\Delta T$	—	-1.0	—	mV/°C

MC7912AC ELECTRICAL CHARACTERISTICS (V_I = -19 V, I_O = 500 mA, 0°C < T_J < +125°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Output Voltage (T_J = +25°C)	V_O	-11.75	-12	-12.25	Vdc
Line Regulation (Note 1) -16 Vdc ≥ V_I ≥ -22 Vdc; I_O = 1.0 A, T_J = 25°C -16 Vdc ≥ V_I ≥ -22 Vdc; I_O = 1.0 A, -14.8 Vdc ≥ V_I ≥ -30 Vdc; I_O = 500 mA -14.5 Vdc ≥ V_I ≥ -27 Vdc; I_O = 1.0 A, T_J = 25°C	Reg_{line}	 — — — —	 6.0 24 24 13	 60 120 120 120	mV
Load Regulation (Note 1) 5.0 mA ≤ I_O ≤ 1.5 A, T_J = 25°C 250 mA ≤ I_O ≤ 750 mA 5.0 mA ≤ I_O ≤ 1.0 A	Reg_{load}	 — — —	 46 17 35	 150 75 150	mV
Output Voltage -14.8 Vdc ≥ V_I ≥ -27 Vdc, 5.0 mA ≤ I_O ≤ 1.0 A, P ≤ 15 W	V_O	-11.5	—	-12.5	Vdc
Input Bias Current	I_{IB}	—	4.4	8.0	mA
Input Bias Current Change -15 Vdc ≥ V_I ≥ -30 Vdc 5.0 mA ≤ I_O ≤ 1.0 A 5.0 mA ≤ I_O ≤ 1.5 A, T_J = 25°C	ΔI_{IB}	 — — —	 — — —	 0.8 0.5 0.5	mA
Output Noise Voltage (T_A = +25°C, 10 Hz ≤ f ≤ 100 kHz)	e_{on}	—	75	—	μV
Ripple Rejection (I_O = 20 mA, f = 120 Hz)	RR	—	61	—	dB
Dropout Voltage I_O = 1.0 A, T_J = +25°C	V_I-V_O	—	2.0	—	Vdc
Average Temperature Coefficient of Output Voltage I_O = 5.0 mA, 0°C ≤ T_J ≤ +125°C	$\Delta V_O/\Delta T$	—	-1.0	—	mV/°C

Note:
1. Load and line regulation are specified at constant junction temperature. Changes in V_O due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

MC7918C ELECTRICAL CHARACTERISTICS (V_I = -27 V, I_O = 500 mA, 0°C < T_J < +125°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Output Voltage (T_J = +25°C)	V_O	-17.3	-18	-18.7	Vdc
Line Regulation (Note 1)	Reg_{line}				mV
(T_J = +25°C, I_O = 100 mA)					
-21 Vdc ≥ V_I ≥ -33 Vdc		—	25	180	
-24 Vdc ≥ V_I ≥ -30 Vdc		—	10	90	
(T_J = +25°C, I_O = 500 mA)					
-21 Vdc ≥ V_I ≥ -33 Vdc		—	90	360	
-24 Vdc ≥ V_I ≥ -30 Vdc		—	50	180	
Load Regulation (T_J = +25°C) (Note 1)	Reg_{load}				mV
5.0 mA ≤ I_O ≤ 1.5 A		—	110	360	
250 mA ≤ I_O ≤ 750 mA		—	55	180	
Output Voltage	V_O	-17.1	—	-18.9	Vdc
-21 Vdc ≥ V_I ≥ -33 Vdc, 5.0 mA ≤ I_O ≤ 1.0 A, P ≤ 15 W					
Input Bias Current (T_J = +25°C)	I_{IB}	—	4.5	8.0	mA
Input Bias Current Change	ΔI_{IB}				mA
-21 Vdc ≥ V_I ≥ -33 Vdc		—	—	1.0	
5.0 mA ≤ I_O ≤ 1.5 A		—	—	0.5	
Output Noise Voltage (T_A = +25°C, 10 Hz ≤ f ≤ 100 kHz)	e_{on}	—	110	—	μV
Ripple Rejection (I_O = 20 mA, f = 120 Hz)	RR	—	59	—	dB
Dropout Voltage	V_I-V_O	—	2.0	—	Vdc
I_O = 1.0 A, T_J = +25°C					
Average Temperature Coefficient of Output Voltage	$\Delta V_O/\Delta T$	—	-1.0	—	mV/°C
I_O = 5.0 mA, 0°C ≤ T_J ≤ +125°C					

MC7924C ELECTRICAL CHARACTERISTICS (V_I = -33 V, I_O = 500 mA, 0°C < T_J < +125°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Output Voltage (T_J = +25°C)	V_O	-23	-24	-25	Vdc
Line Regulation (Note 1)	Reg_{line}				mV
(T_J = +25°C, I_O = 100 mA)					
-27 Vdc ≥ V_I ≥ -38 Vdc		—	31	240	
-30 Vdc ≥ V_I ≥ -36 Vdc		—	14	120	
(T_J = +25°C, I_O = 500 mA)					
-27 Vdc ≥ V_I ≥ -38 Vdc		—	118	480	
-30 Vdc ≥ V_I ≥ -36 Vdc		—	70	240	
Load Regulation (T_J = +25°C) (Note 1)	Reg_{load}				mV
5.0 mA ≤ I_O ≤ 1.5 A		—	150	480	
250 mA ≤ I_O ≤ 750 mA		—	85	240	
Output Voltage	V_O	-22.8	—	-25.2	Vdc
-27 Vdc ≥ V_I ≥ -38 Vdc, 5.0 mA ≤ I_O ≤ 1.0 A, P ≤ 15 W					
Input Bias Current (T_J = +25°C)	I_{IB}	—	4.6	8.0	mA
Input Bias Current Change	ΔI_{IB}				mA
-27 Vdc ≥ V_I ≥ -38 Vdc		—	—	1.0	
5.0 mA ≤ I_O ≤ 1.5 A		—	—	0.5	
Output Noise Voltage (T_A = +25°C, 10 Hz ≤ f ≤ 100 kHz)	e_{on}	—	170	—	μV
Ripple Rejection (I_O = 20 mA, f = 120 Hz)	RR	—	56	—	dB
Dropout Voltage	V_I-V_O	—	2.0	—	Vdc
I_O = 1.0 A, T_J = +25°C					
Average Temperature Coefficient of Output Voltage	$\Delta V_O/\Delta T$	—	-1.0	—	mV/°C
I_O = 5.0 mA, 0°C ≤ T_J ≤ +125°C					

Note:

1. Load and line regulation are specified at constant junction temperature. Changes in V_O due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

TYPICAL CHARACTERISTICS
(T_A = +25°C unless otherwise noted.)

FIGURE 1 – WORST CASE POWER DISSIPATION AS A FUNCTION OF AMBIENT TEMPERATURE

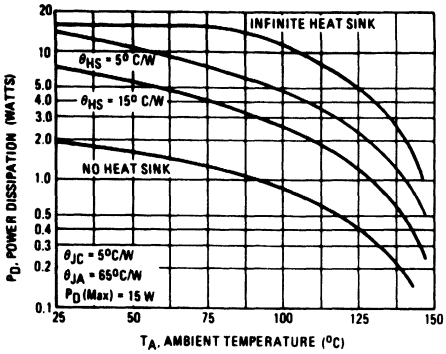


FIGURE 2 – WORST CASE POWER DISSIPATION AS A FUNCTION OF AMBIENT TEMPERATURE

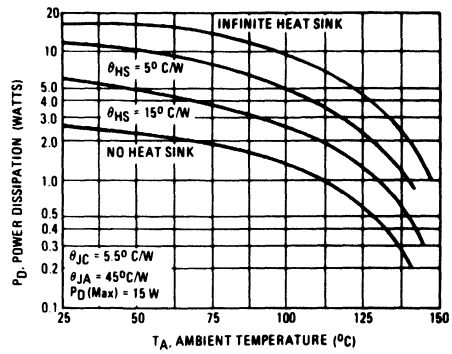


FIGURE 3 – PEAK OUTPUT CURRENT AS A FUNCTION OF INPUT-OUTPUT DIFFERENTIAL VOLTAGE

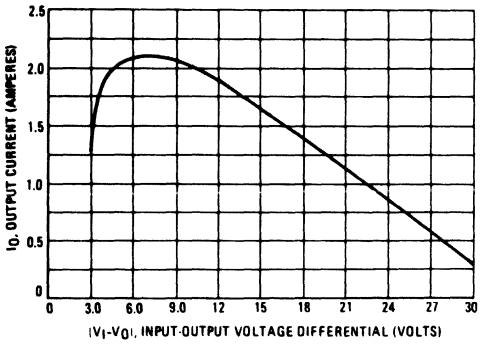


FIGURE 4 – RIPPLE REJECTION AS A FUNCTION OF FREQUENCY

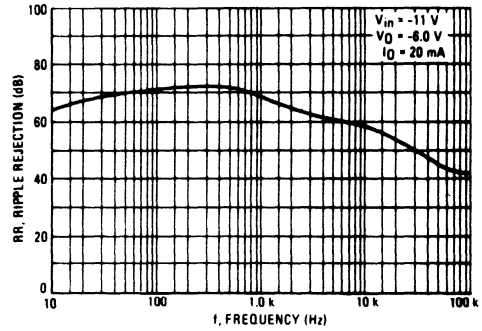


FIGURE 5 – RIPPLE REJECTION AS A FUNCTION OF OUTPUT VOLTAGES

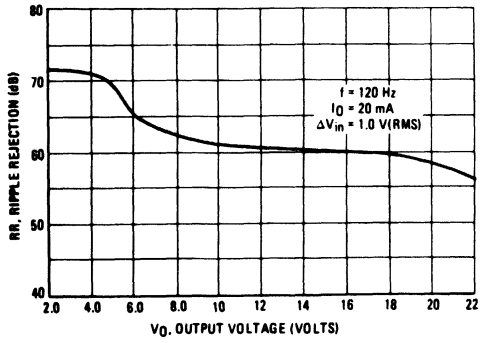
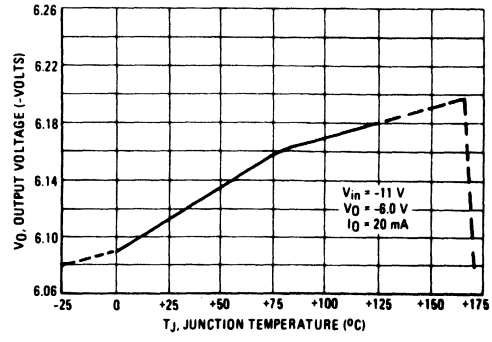
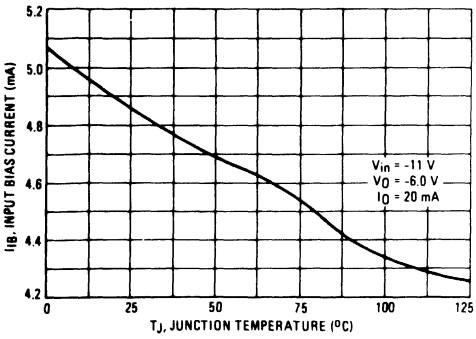


FIGURE 6 – OUTPUT VOLTAGE AS A FUNCTION OF JUNCTION TEMPERATURE



TYPICAL CHARACTERISTICS (continued)

FIGURE 7 – QUIESCENT CURRENT AS A FUNCTION OF TEMPERATURE



DEFINITIONS

Line Regulation – The change in output voltage for a change in the input voltage. The measurement is made under conditions of low dissipation or by using pulse techniques such that the average chip temperature is not significantly affected.

Load Regulation – The change in output voltage for a change in load current at constant chip temperature.

Maximum Power Dissipation – The maximum total device dissipation for which the regulator will operate within specifications.

Input Bias Current – That part of the input current that is not delivered to the load.

Output Noise Voltage – The rms ac voltage at the output, with constant load and no input ripple, measured over a specified frequency range.

Long Term Stability – Output voltage stability under accelerated life test conditions with the maximum rated voltage listed in the devices' electrical characteristics and maximum power dissipation.

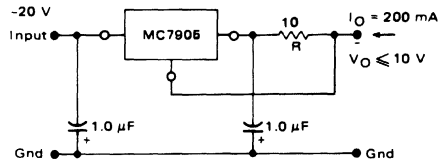
APPLICATIONS INFORMATION

Design Considerations

The MC7900 Series of fixed voltage regulators are designed with Thermal Overload Protection that shuts down the circuit when subjected to an excessive power overload condition, Internal Short-Circuit Protection that limits the maximum current the circuit will pass, and Output Transistor Safe-Area Compensation that reduces the output short-circuit current as the voltage across the pass transistor is increased.

In many low current applications, compensation capacitors are not required. However, it is recommended that the regulator input be bypassed with a capacitor if the regulator is connected to the power supply filter with long wire lengths, or if the output load capacitance is large. An input bypass capacitor should be selected to provide good high-frequency characteristics to insure stable operation under all load conditions. A 0.33 μF or larger tantalum, mylar, or other capacitor having low internal impedance at high frequencies should be chosen. The bypass capacitor should be mounted with the shortest possible leads directly across the regulators input terminals. Normally good construction techniques should be used to minimize ground loops and lead resistance drops since the regulator has no external sense lead. Bypassing the output is also recommended.

FIGURE 8 – CURRENT REGULATOR

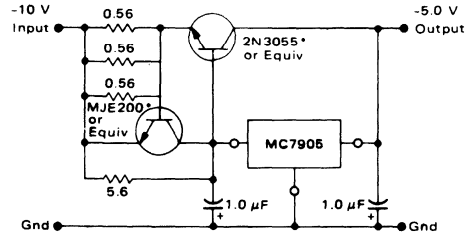


The MC7905,-5.0 V regulator can be used as a constant current source when connected as above. The output current is the sum of resistor R current and quiescent bias current as follows:

$$I_O = \frac{5.0\ V}{R} + I_B$$

The quiescent current for this regulator is typically 4.3 mA. The 5.0 volt regulator was chosen to minimize dissipation and to allow the output voltage to operate to within 6.0 V below the input voltage.

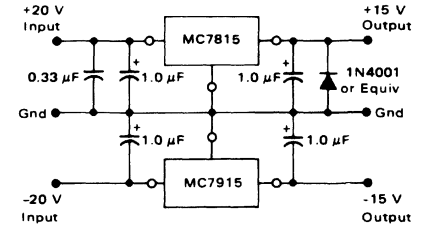
FIGURE 9 – CURRENT BOOST REGULATOR
(-5.0 V @ 4.0 A, with 5.0 A current limiting)



*Mounted on common heat sink, Motorola MS-10 or equivalent.

When a boost transistor is used, short-circuit currents are equal to the sum of the series pass and regulator limits, which are measured at 3.2 A and 1.8 A respectively in this case. Series pass limiting is approximately equal to 0.6 V/R_{SC}. Operation beyond this point to the peak current capability of the MC7905C is possible if the regulator is mounted on a heat sink; otherwise thermal shutdown will occur when the additional load current is picked up by the regulator.

FIGURE 10 – OPERATIONAL AMPLIFIER SUPPLY
(±15 V @ 1.0 A)



The MC7815 and MC7915 positive and negative regulators may be connected as shown to obtain a dual power supply for operational amplifiers. A clamp diode should be used at the output of the MC7815 to prevent potential latch-up problems whenever the output of the positive regulator (MC7815) is drawn below ground with an output current greater than 200 mA.

MOTOROLA

MC79L00,A Series

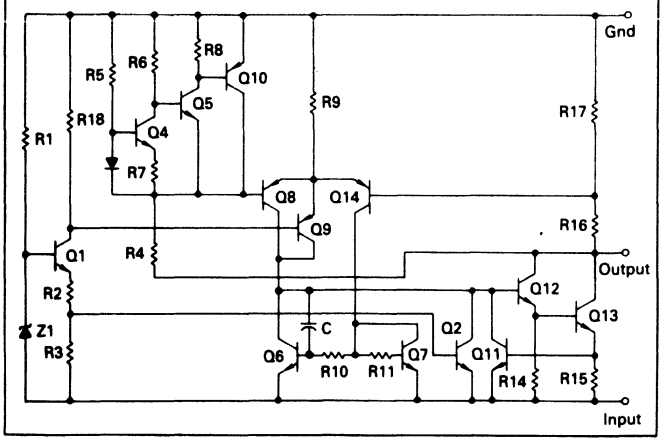
THREE-TERMINAL LOW CURRENT NEGATIVE VOLTAGE REGULATORS

The MC79L00 Series negative voltage regulators are inexpensive, easy-to-use devices suitable for numerous applications requiring up to 100 mA. Like the higher powered MC7900 Series negative regulators, this series features thermal shutdown and current limiting, making them remarkably rugged. In most applications, no external components are required for operation.

The MC79L00 devices are useful for on-card regulation or any other application where a regulated negative voltage at a modest current level is needed. These regulators offer substantial advantage over the common resistor/zener diode approach.

- No External Components Required
- Internal Short-Circuit Current Limiting
- Internal Thermal Overload Protection
- Low Cost
- Complementary Positive Regulators Offered (MC78L00 Series)
- Available in Either ±5% (AC) or ±10% (C) Selections

REPRESENTATIVE CIRCUIT SCHEMATIC



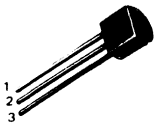
Device No. ±10%	Device No. ±5%	Nominal Voltage
MC79L05C	MC79L05AC	−5.0
MC79L12C	MC79L12AC	−12
MC79L15C	MC79L15AC	−15
MC79L18C	MC79L18AC	−18
MC79L24C	MC79L24AC	−24

#Automotive temperature range selections are available with special test conditions and additional tests in 5, 12 and 15 volt devices. Contact your local Motorola sales office for information.

THREE-TERMINAL LOW CURRENT NEGATIVE FIXED VOLTAGE REGULATORS

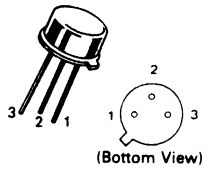
P SUFFIX
PLASTIC PACKAGE
CASE 29-04

PIN 1. GROUND
2. INPUT
3. OUTPUT



G SUFFIX
METAL PACKAGE
CASE 79-05

PIN 1. GROUND
2. OUTPUT
3. INPUT



(Bottom View)
(Case Connected To Pin 3)

D SUFFIX
PLASTIC PACKAGE
CASE 751-03
SOP-8

PIN 1. V_{OUT}
2. V_{IN}
3. V_{IN}
4. NC
5. GND
6. V_{IN}
7. V_{IN}
8. NC

SOP-8 is an internally modified SO-8 Package. Pins 2, 3, 6 and 7 are electrically common to the die attach flag. This internal lead frame modification decreases package thermal resistance and increases power dissipation capability when appropriately mounted on a printed circuit board. SOP-8 conforms to all external dimensions of the standard SO-8 Package.

ORDERING INFORMATION

Device	Tested Operating Temperature Range	Package
MC79LXXACD*	T_J = 0°C to +125°C	SOP-8
MC79LXXACG*		Metal Can
MC79LXXACP		Plastic Power
MC79LXXCG*		Metal Can
MC79LXXCP		Plastic Power
MC79LXXABP#	T_J = −40°C to +125°C	

XX indicates nominal voltage
*Available in 5, 12 and 15 volt devices

MAXIMUM RATINGS (T_A = +25°C unless otherwise noted.)

Rating	Symbol	Value	Unit
Input Voltage (−5 V) (−12, −15, −18 V) (−24 V)	V_I	−30 −35 −40	Vdc
Storage Temperature Range	T_{stg}	−65 to +150	°C
Junction Temperature Range	T_J	0 to +150	°C

MC79L05C, AC Series ELECTRICAL CHARACTERISTICS (V_I = -10 V, I_O = 40 mA, C_I = 0.33 μF, C_O = 0.1 μF, 0°C < T_J < +125°C unless otherwise noted.)

Characteristic	Symbol	MC79L05C			MC79L05AC			Unit
		Min	Typ	Max	Min	Typ	Max	
Output Voltage (T_J = +25°C)	V_O	-4.6	-5.0	-5.4	-4.8	-5.0	-5.2	Vdc
Input Regulation (T_J = +25°C) -7.0 Vdc ≥ V_I ≥ -20 Vdc -8.0 Vdc ≥ V_I ≥ -20 Vdc	Reg_{line}	 – –	 – –	 200 150	 – –	 – –	 150 100	mV
Load Regulation T_J = +25°C, 1.0 mA ≤ I_O ≤ 100 mA 1.0 mA ≤ I_O ≤ 40 mA	Reg_{load}	 – –	 – –	 60 30	 – –	 – –	 60 30	mV
Output Voltage -7.0 Vdc ≥ V_I ≥ -20 Vdc, 1.0 mA ≤ I_O ≤ 40 mA V_I = -10 Vdc, 1.0 mA ≤ I_O ≤ 70 mA	V_O	 -4.5 -4.5	 – –	 -5.5 -5.5	 -4.75 -4.75	 – –	 -5.25 -5.25	Vdc
Input Bias Current (T_J = +25°C) (T_J = +125°C)	I_{IB}	 – –	 – –	 6.0 5.5	 – –	 – –	 6.0 5.5	mA
Input Bias Current Change -8.0 Vdc ≥ V_I ≥ -20 Vdc 1.0 mA ≤ I_O ≤ 40 mA	ΔI_{IB}	 – –	 – –	 1.5 0.2	 – –	 – –	 1.5 0.1	mA
Output Noise Voltage (T_A = +25°C, 10 Hz ≤ f ≤ 100 kHz)	V_n	–	40	–	–	40	–	μV
Ripple Rejection (-8.0 ≥ V_I ≥ 18 Vdc, f = 120 Hz, T_J = 25°C)	RR	40	49	–	41	49	–	dB
Dropout Voltage I_O = 40 mA, T_J = +25°C	$\lvert V_I - V_O \rvert$	–	1.7	–	–	1.7	–	Vdc

MC79L12C, AC ELECTRICAL CHARACTERISTICS (V_I = -19 V, I_O = 40 mA, C_I = 0.33 μF, C_O = 0.1 μF, 0°C < T_J < +125°C unless otherwise noted.)

Characteristic	Symbol	MC79L12C			MC79L12AC			Unit
		Min	Typ	Max	Min	Typ	Max	
Output Voltage (T_J = +25°C)	V_O	-11.1	-12	-12.9	-11.5	-12	-12.5	Vdc
Input Regulation (T_J = +25°C) -14.5 Vdc ≥ V_I ≥ -27 Vdc -16 Vdc ≥ V_I ≥ -27 Vdc	Reg_{line}	 – –	 – –	 250 200	 – –	 – –	 250 200	mV
Load Regulation T_J = +25°C, 1.0 mA ≤ I_O ≤ 100 mA 1.0 mA ≤ I_O ≤ 40 mA	Reg_{load}	 – –	 – –	 100 50	 – –	 – –	 100 50	mV
Output Voltage -14.5 Vdc ≥ V_I ≥ -27 Vdc, 1.0 mA ≤ I_O ≤ 40 mA V_I = -19 Vdc, 1.0 mA ≤ I_O ≤ 70 mA	V_O	 -10.8 -10.8	 – –	 -13.2 -13.2	 -11.4 -11.4	 – –	 -12.6 -12.6	Vdc
Input Bias Current (T_J = +25°C) (T_J = +125°C)	I_{IB}	 – –	 – –	 6.5 6.0	 – –	 – –	 6.5 6.0	mA
Input Bias Current Change -16 Vdc ≥ V_I ≥ -27 Vdc 1.0 mA ≤ I_O ≤ 40 mA	ΔI_{IB}	 – –	 – –	 1.5 0.2	 – –	 – –	 1.5 0.1	mA
Output Noise Voltage (T_A = +25°C, 10 Hz ≤ f ≤ 100 kHz)	V_n	–	80	–	–	80	–	μV
Ripple Rejection (-15 ≤ V_I ≤ -25 Vdc, f = 120Hz, T_J = +25°C)	RR	36	42	–	37	42	–	dB
Dropout Voltage I_O = 40 mA, T_J = +25°C	$\lvert V_I - V_O \rvert$	–	1.7	–	–	1.7	–	Vdc

MC79L15C, AC ELECTRICAL CHARACTERISTICS (V_I = -23 V, I_O = 40 mA, C_I = 0.33 μF, C_O = 0.1 μF, $0^oC < T_J < +125^oC$ unless otherwise noted.)

Characteristic	Symbol	MC79L15C			MC79L15AC			Unit
		Min	Typ	Max	Min	Typ	Max	
Output Voltage (T_J = +25°C)	V_O	-13.8	-15	-16.2	-14.4	-15	-15.6	Vdc
Input Regulation (T_J = +25°C)	Reg_{line}							mV
-17.5 Vdc ≥ V_I ≥ -30 Vdc		–	–	300	–	–	300	
-20 Vdc ≥ V_I ≥ -30 Vdc		–	–	250	–	–	250	
Load Regulation	Reg_{load}							mV
T_J = +25°C, 1.0 mA ≤ I_O ≤ 100 mA		–	–	150	–	–	150	
1.0 mA ≤ I_O ≤ 40 mA		–	–	75	–	–	75	
Output Voltage	V_O							Vdc
-17.5 Vdc ≥ V_I ≥ -30 Vdc, 1.0 mA ≤ I_O ≤ 40 mA		-13.5	–	-16.5	-14.25	–	-15.75	
V_I = -23 Vdc, 1.0 mA ≤ I_O ≤ 70 mA		-13.5	–	-16.5	-14.25	–	-15.75	
Input Bias Current	I_{IB}							mA
(T_J = +25°C)		–	–	6.5	–	–	6.5	
(T_J = +125°C)		–	–	6.0	–	–	6.0	
Input Bias Current Change	ΔI_{IB}							mA
-20 Vdc ≥ V_I ≥ -30 Vdc		–	–	1.5	–	–	1.5	
1.0 mA ≤ I_O ≤ 40 mA		–	–	0.2	–	–	0.1	
Output Noise Voltage (T_A = +25°C, 10 Hz ≤ f ≤ 100 kHz)	V_n	–	90	–	–	90	–	μV
Ripple Rejection (-18.5 ≤ V_I ≤ -28.5 Vdc, f = 120 Hz)	RR	33	39	–	34	39	–	dB
Dropout Voltage I_O = 40 mA, T_J = +25°C	$\|V_I-V_O\|$	–	1.7	–	–	1.7	–	Vdc

MC79L18C, AC ELECTRICAL CHARACTERISTICS (V_I = -27 V, I_O = 40 mA, C_I = 0.33 μF, C_O = 0.1 μF, $0^oC < T_J < +125^oC$ unless otherwise noted.)

Characteristic	Symbol	MC79L18C			MC79L18AC			Unit
		Min	Typ	Max	Min	Typ	Max	
Output Voltage (T_J = +25°C)	V_O	-16.6	-18	-19.4	-17.3	-18	-18.7	Vdc
Input Regulation (T_J = +25°C)	Reg_{line}							mV
-20.7 Vdc ≥ V_I ≥ -33 Vdc		–	–	–	–	–	325	
-21.4 Vdc ≥ V_I ≥ -33 Vdc		–	–	325	–	–	–	
-22 Vdc ≥ V_I ≥ -33 Vdc		–	–	275	–	–	–	
-21 Vdc ≥ V_I ≥ -33 Vdc		–	–	–	–	–	275	
Load Regulation	Reg_{load}							mV
T_J = +25°C, 1.0 mA ≤ I_O ≤ 100 mA		–	–	170	–	–	170	
1.0 mA ≤ I_O ≤ 40 mA		–	–	85	–	–	85	
Output Voltage	V_O							Vdc
-20.7 Vdc ≥ V_I ≥ -33 Vdc, 1.0 mA ≤ I_O ≤ 40 mA		–	–	–	-17.1	–	-18.9	
-21.4 Vdc ≥ V_I ≥ -33 Vdc, 1.0 mA ≤ I_O ≤ 40 mA		-16.2	–	-19.8	–	–	–	
V_I = -27 Vdc, 1.0 mA ≤ I_O ≤ 70 mA		-16.2	–	-19.8	-17.1	–	-18.9	
Input Bias Current	I_{IB}							mA
(T_J = +25°C)		–	–	6.5	–	–	6.5	
(T_J = +125°C)		–	–	6.0	–	–	6.0	
Input Bias Current Change	ΔI_{IB}							mA
-21 Vdc ≥ V_I ≥ -33 Vdc		–	–	–	–	–	1.5	
-27 Vdc ≥ V_I ≥ -33 Vdc		–	–	1.5	–	–	–	
1.0 mA ≤ I_O ≤ 40 mA		–	–	0.2	–	–	0.1	
Output Noise Voltage (T_A = +25°C, 10 Hz ≤ f ≤ 100 kHz)	V_n	–	150	–	–	150	–	μV
Ripple Rejection (-23 ≤ V_I ≤ -33 Vdc, f = 120 Hz, T_J = +25°C)	RR	32	46	–	33	48	–	dB
Dropout Voltage I_O = 40 mA, T_J = +25°C	$\|V_I-V_O\|$	–	1.7	–	–	1.7	–	Vdc

MC79L24C, AC ELECTRICAL CHARACTERISTICS (V_I = -33 V, I_O = 40 mA, C_I = 0.33 μF, C_O = 0.1 μF, 0°C < T_J < +125°C unless otherwise noted.)

Characteristic	Symbol	MC79L24C			MC79L24AC			Unit
		Min	Typ	Max	Min	Typ	Max	
Output Voltage (T_J = +25°C)	V_O	-22.1	-24	-25.9	-23	-24	-25	Vdc
Input Regulation (T_J = +25°C)	Reg_{line}							mV
-27 Vdc ≥ V_I ≥ -38 V		–	–	–	–	–	350	
-27.5 Vdc ≥ V_I ≥ -38 Vdc		–	–	350	–	–	–	
-28 Vdc ≥ V_I ≥ -38 Vdc		–	–	300	–	–	300	
Load Regulation	Reg_{load}							mV
T_J = +25°C, 1.0 mA ≤ I_O ≤ 100 mA		–	–	200	–	–	200	
1.0 mA ≤ I_O ≤ 40 mA		–	–	100	–	–	100	
Output Voltage	V_O							Vdc
-27 Vdc ≥ V_I ≥ -38 V, 1.0 mA ≤ I_O ≤ 40 mA		–	–	–	-22.8	–	-25.2	
-28 Vdc ≥ V_I ≥ -38 Vdc, 1.0 mA ≤ I_O ≤ 40 mA		-21.4	–	-26.4	–	–	–	
V_I = -33 Vdc, 1.0 mA ≤ I_O ≤ 70 mA		-21.4	–	-26.4	-22.8	–	-25.2	
Input Bias Current	I_{IB}							mA
(T_J = +25°C)		–	–	6.5	–	–	6.5	
(T_J = +125°C)		–	–	6.0	–	–	6.0	
Input Bias Current Change	ΔI_{IB}							mA
-28 Vdc ≥ V_I ≥ -38 Vdc		–	–	1.5	–	–	1.5	
1.0 mA ≤ I_O ≤ 40 mA		–	–	0.2	–	–	0.1	
Output Noise Voltage (T_A = +25°C, 10 Hz ≤ f ≤ 100 kHz)	V_n	–	200	–	–	200	–	μV
Ripple Rejection (-29 ≤ V_I ≤ -35 Vdc, f = 120 Hz, T_J = 25°C)	RR	30	43	–	31	47	–	dB
Dropout Voltage I_O = 40 mA, T_J = +25°C	$\|V_I - V_O\|$	–	1.7	–	–	1.7	–	Vdc

APPLICATIONS INFORMATION

Design Considerations

The MC79L00 Series of fixed voltage regulators are designed with Thermal Overload Protection that shuts down the circuit when subjected to an excessive power overload condition, Internal Short-Circuit Protection that limits the maximum current the circuit will pass.

In many low current applications, compensation capacitors are not required. However, it is recommended that the regulator input be bypassed with a capacitor if the regulator is connected to the power supply filter with long wire lengths, or if the output load capacitance is large. An input bypass capacitor should be selected to provide good high-frequency characteristics to insure stable operation under all load conditions. A 0.33 μF or larger tantalum, mylar, or other capacitor having low internal impedance at high frequencies should be chosen. The bypass capacitor should be mounted with the shortest possible leads directly across the regulator's input terminals. Normally good construction techniques should be used to minimize ground loops and lead resistance drops since the regulator has no external sense lead. Bypassing the output is also recommended.

FIGURE 1 — POSITIVE AND NEGATIVE REGULATOR

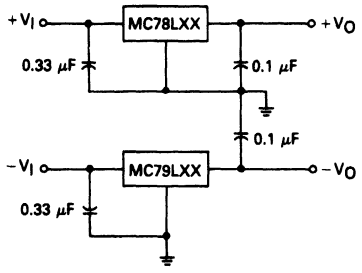
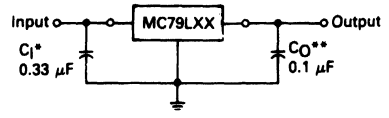


FIGURE 2 — STANDARD APPLICATION



A common ground is required between the input and the output voltages. The input voltage must remain typically 2.0 V above the output voltage even during the low point on the input ripple voltage.

* = C_I is required if regulator is located an appreciable distance from power supply filter.

** = C_O improves stability and transient response.

TYPICAL CHARACTERISTICS

(T_A = +25°C unless otherwise noted.)

FIGURE 3 — DROPOUT CHARACTERISTICS

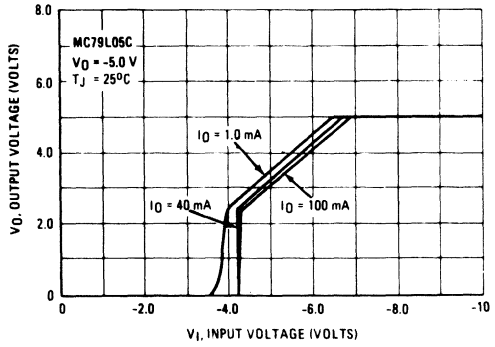


FIGURE 4 — DROPOUT VOLTAGE versus JUNCTION TEMPERATURE

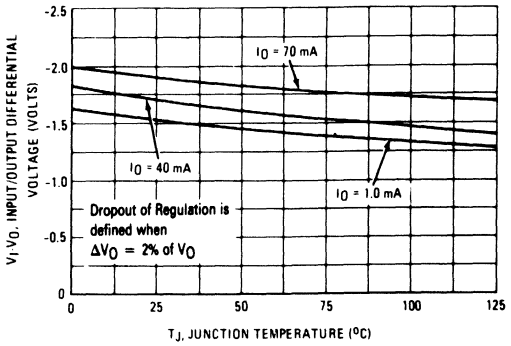


FIGURE 5 — INPUT BIAS CURRENT versus AMBIENT TEMPERATURE

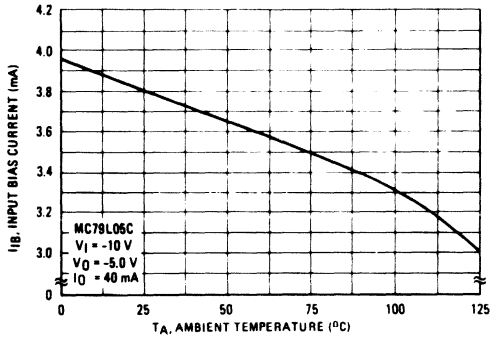


FIGURE 6 — INPUT BIAS CURRENT versus INPUT VOLTAGE

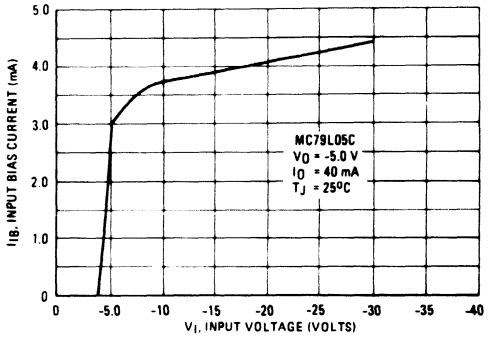


FIGURE 7 — MAXIMUM AVERAGE POWER DISSIPATION versus AMBIENT TEMPERATURE — TO-92 Type Package

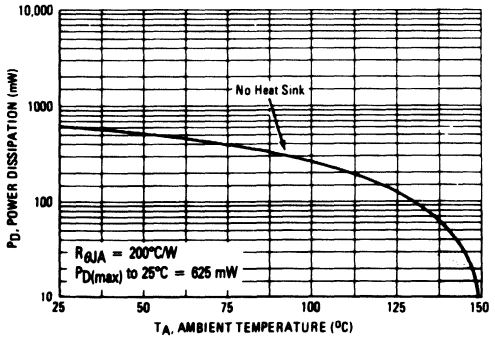
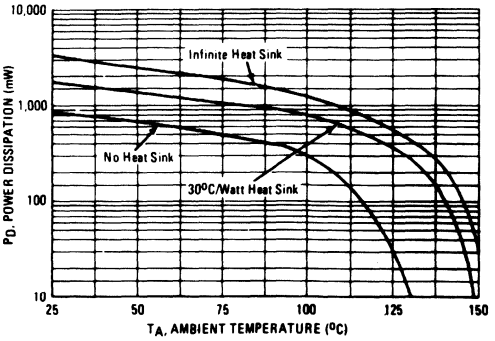


FIGURE 8 — MAXIMUM AVERAGE POWER DISSIPATION versus AMBIENT TEMPERATURE — TO-39 Type Package



MOTOROLA

MC79M00 Series

THREE-TERMINAL NEGATIVE VOLTAGE REGULATORS

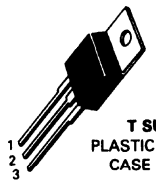
The MC79M00 Series of fixed output negative voltage regulators are intended as complements to the popular MC78M00 Series devices.

Available in fixed output voltage options of −5.0, −12 and −15 volts, these regulators employ current limiting, thermal shutdown, and safe-area compensation — making them remarkably rugged under most operating conditions. With adequate heatsinking they can deliver output currents in excess of 0.5 ampere.

- No External Components Required
- Internal Thermal Overload Protection
- Internal Short-Circuit Current Limiting
- Output Transistor Safe-Area Compensation

THREE-TERMINAL NEGATIVE FIXED VOLTAGE REGULATORS

SILICON MONOLITHIC INTEGRATED CIRCUITS

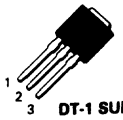


T SUFFIX
PLASTIC PACKAGE
CASE 221A-04

PIN 1. GROUND
2. INPUT
3. OUTPUT

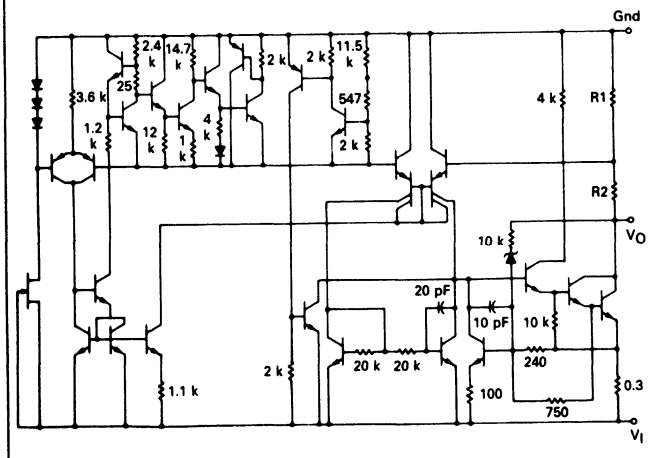
(Heatsink surface connected to Pin 2)

DT SUFFIX
PLASTIC PACKAGE
CASE 369A-03
DPAK

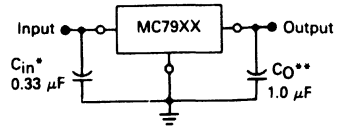


DT-1 SUFFIX
PLASTIC PACKAGE
CASE 369-03
DPAK

EQUIVALENT SCHEMATIC DIAGRAM



STANDARD APPLICATION



A common ground is required between the input and the output voltages. The input voltage must remain typically 1.1 V more negative even during the high point on the input ripple voltage.

XX = these two digits of the type number indicate voltage.

* = C_{in} is required if regulator is located an appreciable distance from power supply filter.

** = C_O improves stability and transient response.

ORDERING INFORMATION

Device	Output Voltage	Tested Operating Junction Temp. Range	Package
MC79M05CDT, CDT-1	−5.0 Volts	0°C to +125°C	DPAK
MC79M05CT			PLASTIC POWER
MC79M12CDT, CDT-1	−12 Volts		DPAK
MC79M12CT			PLASTIC POWER
MC79M15CDT, CDT-1	−15 Volts		DPAK
MC79M15CT			PLASTIC POWER

MC79MXX Series MAXIMUM RATINGS (T_A = +25°C unless otherwise noted.)

Rating	Symbol	Value	Unit
Input Voltage	V_I	-35	Vdc
Power Dissipation Plastic Package T_A = +25°C Derate above T_A = +25°C T_C = +25°C Derate above T_C = +95°C	 P_D $1/R\theta_{JA}$ P_D $1/R\theta_{JC}$	 Internally Limited 14.2 Internally Limited 200	 Watts mW/°C Watts mW/°C
Storage Junction Temperature Range	T_{stg}	-65 to +150	°C
Junction Temperature Range	T_J	0 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Ambient	$R\theta_{JA}$	65	°C/W
Thermal Resistance, Junction to Case	$R\theta_{JC}$	5.0	°C/W

MC79MO5C ELECTRICAL CHARACTERISTICS (V_I = -10 V, I_O = 350 mA, 0°C < T_J < +125°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Output Voltage (T_J = +25°C)	V_O	-4.8	-5.0	-5.2	Vdc
Line Regulation (T_J = +25°C) (Note 1) -7.0 Vdc ≥ V_I ≥ -25 Vdc -8.0 Vdc ≥ V_I ≥ -18 Vdc	Reg_{line}	 — —	 7.0 2.0	 50 30	mV
Load Regulation (T_J = +25°C) (Note 1) 5.0 mA ≤ I_O ≤ 500 mA	Reg_{load}	—	30	100	mV
Output Voltage -7.0 Vdc ≥ V_I ≥ -25 Vdc, 5.0 mA ≤ I_O ≤ 350 mA	V_O	4.75	—	-5.25	Vdc
Input Bias Current (T_J = +25°C)	I_{IB}	—	4.3	8.0	mA
Input Bias Current Change -8.0 Vdc≥ V_I ≥ -25 Vdc, I_O = 350 mA 5.0 mA ≤ I_O ≤ 350 mA, V_I = -10 V	ΔI_{IB}	 — —	 — —	 0.4 0.4	mA
Output Noise Voltage (T_A = +25°C, 10 Hz ≤ f ≤ 100 kHz)	V_n	—	40	—	μV
Ripple Rejection (f = 120 Hz)	RR	54	66	—	dB
Dropout Voltage I_O = 500 mA, T_J = +25°C	V_I-V_O	—	1.1	—	Vdc
Average Temperature Coefficient of Output Voltage I_O = 5.0 mA, 0°C ≤ T_J ≤ +125°C	$\Delta V_O/\Delta T$	—	0.2	—	mV/°C

Note:
1. Load and line regulation are specified at constant junction temperature. Changes in V_O due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

MC79M12C ELECTRICAL CHARACTERISTICS (V_I = −19 V, I_O = 350 mA, 0°C < T_J < +125°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Output Voltage (T_J = +25°C)	V_O	−11.5	−12	−12.5	Vdc
Line Regulation (T_J = +25°C) (Note 1) −14.5 Vdc ≥ V_I ≥ −30 Vdc −15 Vdc ≥ V_I ≥ −25 Vdc	Reg_{line}	 — —	 5.0 3.0	 80 50	mV mV
Load Regulation (T_J = +25°C) (Note 1) 5.0 mA ≤ I_O ≤ 500 mA	Reg_{load}	—	30	240	mV
Output Voltage −14.5 Vdc ≥ V_I ≥ −30 Vdc, 5.0 mA ≤ I_O ≤ 350 mA	V_O	−11.4	—	−12.6	Vdc
Input Bias Current (T_J = +25°C)	I_{IB}	—	4.4	8.0	mA
Input Bias Current Change −14.5 Vdc ≥ V_I ≥ −30 Vdc, I_O = 350 mA 5.0 mA ≤ I_O ≤ 350 mA, V_I = −19 V	ΔI_{IB}	 — —	 — —	 0.4 0.4	mA
Output Noise Voltage (T_A = +25°C, 10Hz ≤ f ≤ 100 kHz)	V_n	—	75	—	μV
Ripple Rejection (f = 120 Hz)	RR	54	60	—	dB
Dropout Voltage I_O = 500 mA, T_J = +25°C	V_I-V_O	—	1.1	—	Vdc
Average Temperature Coefficient of Output Voltage I_O = 5.0 mA, 0°C ≤ T_J ≤ +125°C	$\Delta V_O/\Delta T$	—	−0.8	—	mV/°C

MC79M15C ELECTRICAL CHARACTERISTICS (V_I = −23 V, I_O = 350 mA, 0°C < T_J < +125°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Output Voltage (T_J = +25°C)	V_O	−14.4	−15	−15.6	Vdc
Line Regulation (T_J = +25°) (Note 1) −17.5 Vdc ≥ V_I ≥ −30 Vdc −18 Vdc ≥ V_I ≥ −28 Vdc	Reg_{line}	 — —	 5.0 3.0	 80 50	mV
Load Regulation (T_J = +25°C) (Note 1) 5.0 mA ≤ I_O ≤ 500 mA	Reg_{load}	—	30	240	mV
Output Voltage −17.5 Vdc ≥ V_I ≥ −30 Vdc, 5.0 mA ≤ I_O ≤ 350 mA	V_O	−14.25	—	−15.75	Vdc
Input Bias Current (T_J = +25°C)	I_{IB}	—	4.4	8.0	mA
Input Bias Current Change −17.5 Vdc ≥ V_I ≥ −30 Vdc, I_O = 350 mA 5.0 mA ≤ I_O ≤ 350 mA, V_I = −23 V	ΔI_{IB}	 — —	 — —	 0.4 0.4	mA
Output Noise Voltage (T_A = +25°C, 10 Hz ≤ f ≤ 100 kHz)	V_n	—	90	—	μV
Ripple Rejection (f = 120 Hz)	RR	54	60	—	dB
Dropout Voltage I_O = 500 mA, T_J = +25°C	V_I-V_O	—	1.1	—	Vdc
Average Temperature Coefficient of Output Voltage I_O = 5.0 mA, 0°C ≤ T_J ≤ +125°C	$\Delta V_O/\Delta T$	—	−1.0	—	mV/°C

Note:

1. Load and line regulation are specified at constant junction temperature. Changes in V_O due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

MOTOROLA

MC34060
MC35060

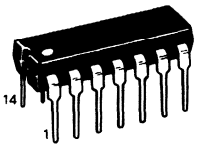
SWITCHMODE PULSE WIDTH MODULATION CONTROL CIRCUITS

The MC35060 and MC34060 are low cost fixed frequency, pulse width modulation control circuits designed primarily for single ended SWITCHMODE power supply control. These devices feature:

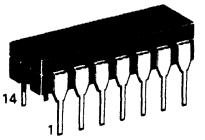
- Complete Pulse Width Modulation Control Circuitry
- On-Chip Oscillator With Master or Slave Operation
- On-Chip Error Amplifiers
- On-Chip 5.0 Volt Reference
- Adjustable Dead Time Control
- Uncommitted Output Transistor for 200 mA Source or Sink

SWITCHMODE PULSE WIDTH MODULATION CONTROL CIRCUITS

SILICON MONOLITHIC INTEGRATED CIRCUITS

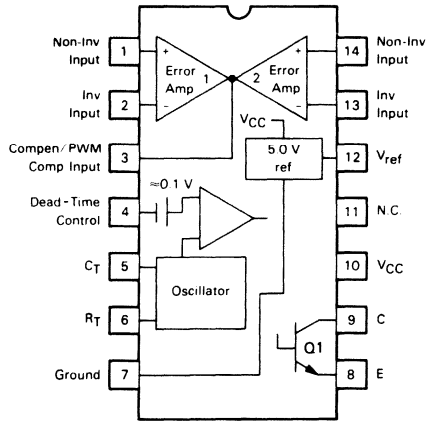


P SUFFIX
PLASTIC PACKAGE
CASE 646-06



L SUFFIX
CERAMIC PACKAGE
CASE 632-08

PIN CONNECTIONS



(Top View)

The MC34060 is specified over the commercial operating range of 0°C to +70°C. The MC35060 is specified over the full military range of -55 to +125°C.

ORDERING INFORMATION

Device	Temperature Range	Package
MC35060L	-55 to +125°C	Ceramic DIP
MC34060P	0 to +70°C	Plastic DIP
MC34060L	0 to +70°C	Ceramic DIP

SWITCHMODE is a trademark of Motorola Inc.

FIGURE 1 — BLOCK DIAGRAM

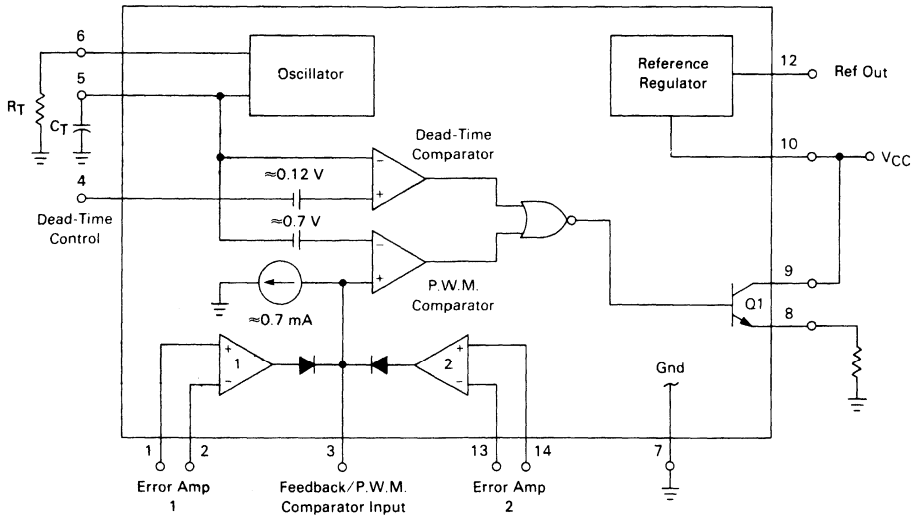
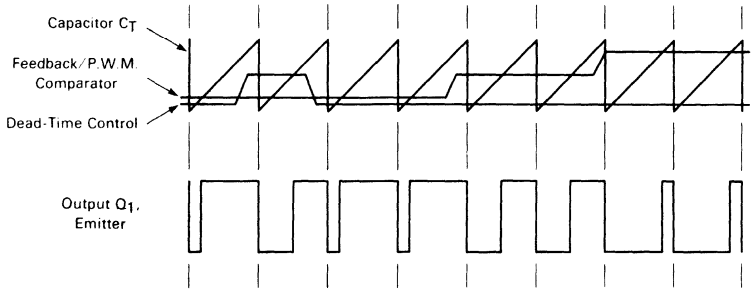


FIGURE 2 — TIMING DIAGRAM



Description

The MC35060/34060 is a fixed-frequency pulse width modulation control circuit, incorporating the primary building blocks required for the control of a switching power supply. (See Figure 1.) An internal-linear sawtooth oscillator is frequency-programmable by two external components, R_T and C_T. The approximate oscillator frequency is determined by:

$$f_{osc} \cong \frac{1.1}{R_T \bullet C_T}$$

For more information refer to Figure 3.

Output pulse width modulation is accomplished by comparison of the positive sawtooth waveform across capacitor C_T to either of two control signals. The output is enabled only during that portion of time when the sawtooth voltage is greater than the control signals. Therefore, an increase in control-signal amplitude causes a corresponding linear decrease of output pulse width. (Refer to the timing diagram shown in Figure 2.)

The control signals are external inputs that can be fed into the dead-time control, the error amplifier inputs, or the feed-back input. The dead-time control comparator has an effective 120 mV input offset which limits the minimum output dead time to approximately the first 4% of the sawtooth-cycle time. This would result in a maximum duty cycle of 96%. Additional dead time may be imposed on the output by setting the dead time-control input to a fixed voltage, ranging between 0 to 3.3 V.

The pulse width modulator comparator provides a means for the error amplifiers to adjust the output pulse width from the maximum percent on-time, established by the dead time control input, down to zero, as the voltage at the feedback pin varies from 0.5 to 3.5 V. Both error amplifiers have a common-mode input range from −0.3 V to (V_{CC} − 2 V), and may be used to sense power supply output voltage and current. The error-amplifier outputs are active high and are ORed together at the non-inverting input of the pulse-width modulator comparator. With this configuration, the amplifier that demands minimum output on time, dominates control of the loop.

The MC35060/34060 has an internal 5.0 V reference capable of sourcing up to 10 mA of load currents for external bias circuits. The reference has an internal accuracy of ±5% with a typical thermal drift of less than 50 mV over an operating temperature range of 0 to +70°C.

MAXIMUM RATINGS (Full operating ambient temperature range applies unless otherwise noted)

Rating	Symbol	MC35060	MC34060	Unit
Power Supply Voltage	V_{CC}	42	42	V
Collector Output Voltage	V_C	42	42	V
Collector Output Current	I_C	250	250	mA
Amplifier Input Voltage	V_{in}	V_{CC} + 0.3	V_{CC} + 0.3	V
Power Dissipation @ $T_A \leq 45°C$	P_D	1000	1000	mW
Operating Junction Temperature Plastic Package Ceramic Package	T_J	 — 150	 125 150	°C
Operating Ambient Temperature Range	T_A	-55 to 125	0 to 70	°C
Storage Temperature Range Plastic Package Ceramic Package	T_{stg}	 — -65 to 150	 -55 to 125 -65 to 150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	L Suffix Ceramic Package	P Suffix Plastic Package	Unit
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	100	80	°C/W
Power Derating Factor	$1/R_{\theta JA}$	10	12.5	mW/°C
Derating Ambient Temperature	T_A	50	45	°C

RECOMMENDED OPERATING CONDITIONS

Condition/Value	Symbol	MC35060/MC34060			Unit
		Min	Typ	Max	
Power Supply Voltage	V_{CC}	7.0	15	40	V
Collector Output Voltage	V_C	—	30	40	V
Collector Output Current	I_C	—	—	200	mA
Amplifier Input Voltage	V_{in}	-0.3	—	V_{CC} - 2	V
Current Into Feedback Terminal	I_{fb}	—	—	0.3	mA
Reference Output Current	I_{ref}	—	—	10	mA
Timing Resistor	R_T	1.8	47	500	kΩ
Timing Capacitor	C_T	0.0047	0.001	10	μF
Oscillator Frequency	f_{osc}	1.0	25	200	kHz

ELECTRICAL CHARACTERISTICS V_{CC} = 15 V, C_T = 0.01 μF, R_T = 12 kΩ unless otherwise noted. For typical values T_A = 25°C, for min/max values T_A is the operating ambient temperature range that applies unless otherwise noted.

Characteristic	Symbol	MC35060			MC34060			Unit
		Min	Typ	Max	Min	Typ	Max	
REFERENCE SECTION								
Reference Voltage (I_O = 1.0 mA)	V_{ref}	4.75	5.0	5.25	4.75	5.0	5.25	V
Input Regulation (V_{CC} = 7.0 V to 40 V)	Reg_{line}	—	2.0	25	—	2.0	25	mV
Output Regulation (I_O = 1.0 mA to 10 mA)	Reg_{load}	—	3.0	15	—	3.0	15	mV
Short-Circuit Output Current (V_{ref} = 0 V)	I_{SC}	15	35	75	15	35	75	mA
OUTPUT SECTION								
Collector Off-State Current (V_{CC} = 40 V, V_{CE} = 40 V)	$I_{C(off)}$	—	2.0	100	—	2.0	100	μA
Emitter Off-State Current (V_{CC} = 40 V, V_C = 40 V, V_E = 0 V)	$I_{E(off)}$	—	—	-150	—	—	-100	μA
Collector-Emitter Saturation Voltage Common-Emitter (V_E = 0 V, I_C = 200 mA)	$V_{sat(C)}$	—	1.1	1.5	—	1.1	1.3	V
Emitter-Follower (V_C = 15 V, I_E = -200 mA)	$V_{sat(E)}$	—	1.5	2.5	—	1.5	2.5	V
Output Voltage Rise Time (T_A = 25°C) Common-Emitter (See Figure 12)	t_r	—	100	200	—	100	200	ns
Emitter-Follower (See Figure 13)		—	100	200	—	100	200	ns
Output Voltage Fall Time (T_A = 25°C) Common-Emitter (See Figure 12)	t_f	—	25	100	—	25	100	ns
Emitter-Follower (See Figure 13)		—	40	100	—	40	100	ns

Characteristic	Symbol	MC35060/MC34060			Unit
		Min	Typ	Max	
ERROR AMPLIFIER SECTIONS					
Input Offset Voltage ($V_{O[Pin\ 3]}$ = 2.5 V)	V_{IO}	—	2.0	10	mV
Input Offset Current ($V_{C[Pin\ 3]}$ = 2.5 V)	I_{IO}	—	5.0	250	nA
Input Bias Current ($V_{O[Pin\ 3]}$ = 2.5 V)	I_{IB}	—	-0.1	-1.0	μA
Input Common-Mode Voltage Range (V_{CC} = 40 V, T_A = 25°C)	V_{ICR}	-0.3 to V_{CC} - 2.0	—	—	V
Open Loop Voltage Gain (ΔV_O = 3.0 V, V_O = 0.5 to 3.5 V, R_L = 2.0 kΩ)	A_{VOL}	70	95	—	dB

ELECTRICAL CHARACTERISTICS V_{CC} = 15 V, C_T = 0.01 μF, R_T = 12 kΩ unless otherwise noted. For typical values T_A = 25°C, for min/max values T_A is the operating ambient temperature range that applies unless otherwise noted.

Characteristic	Symbol	MC35060/MC34060			Unit
		Min.	Typ.	Max.	
ERROR AMPLIFIER SECTIONS (Continued)					
Unity-Gain Crossover Frequency (V_O = 0.5, to 3.5 V, R_L = 2.0 kΩ)	f_c	—	350	—	kHz
Phase Margin at Unity-Gain (V_O = 0.5 to 3.5 V, R_L = 2.0 kΩ)	ϕ_m	—	65	—	deg.
Common-Mode Rejection Ratio (V_{CC} = 40 V)	CMRR	65	90	—	dB
Power Supply Rejection Ratio (ΔV_{CC} = 33 V, V_O = 2.5 V, R_L = 2.0 kΩ)	PSRR	—	100	—	dB
Output Sink Current ($V_{O[Pin\ 3]}$ = 0.7 V)	I_O^-	0.3	0.7	—	mA
Output Source Current ($V_{O[Pin\ 3]}$ = 3.5 V)	I_O^+	-2.0	-4.0	—	mA
PWM COMPARATOR SECTION (Test circuit Figure 11)					
Input Threshold Voltage (Zero Duty Cycle)	V_{TH}	—	3.5	4.5	V
Input Sink Current ($V_{[Pin\ 3]}$ = 0.7 V)	I_I^-	0.3	0.7	—	mA
DEAD-TIME CONTROL SECTION (Test Circuit Figure 11)					
Input Bias Current (Pin 4) (V_{in} = 0 to 5.25 V)	$I_{IB(DT)}$	—	-2.0	-10	μA
Maximum Output Duty Cycle (V_{in} = 0 V, C_T = 0.01 μF, R_T = 12 kΩ) (V_{in} = 0 V, C_T = 0.001 μF, R_T = 47 kΩ)	DC_{max}	 90 —	 96 92	 100 100	%
Input Threshold Voltage (Pin 4) (Zero Duty Cycle) (Maximum Duty Cycle)	V_{TH}	 — 0	 2.8 —	 3.3 —	V
OSCILLATOR SECTION					
Frequency (C_T = 0.001 μF, R_T = 47 kΩ)	f_{osc}	—	25	—	kHz
Standard Deviation of Frequency* (C_T = 0.001 μF, R_T = 47 kΩ)	σf_{osc}	—	3.0	—	%
Frequency Change with Voltage (V_{CC} = 7.0 V to 40 V, T_A = 25°C)	$\Delta f_{osc}(\Delta V)$	—	0.1	—	%
Frequency Change with Temperature (ΔT_A = T_{low} to T_{high}) (C_T = 0.01 μF, R_T = 12 kΩ)	$\Delta f_{osc}(\Delta T)$	 — —	 —	 12	%
TOTAL DEVICE					
Standby Supply Current (Pin 6 at V_{ref}, all other inputs and outputs open) (V_{CC} = 15 V) (V_{CC} = 40 V)	I_{CC}	 — —	 5.5 7.0	 10 15	mA
Average Supply Current ($V_{[Pin\ 4]}$ = 2.0 V, C_T = 0.001, R_T = 47 kΩ). See Figure 11.	I_S	—	7.0	—	mA

*Standard deviation is a measure of the statistical distribution about the mean as derived from the formula, $\sigma = \sqrt{\frac{\sum_{n=1}^{N} (x_n - \bar{x})^2}{N-1}}$

FIGURE 3 — OSCILLATOR FREQUENCY versus TIMING RESISTANCE

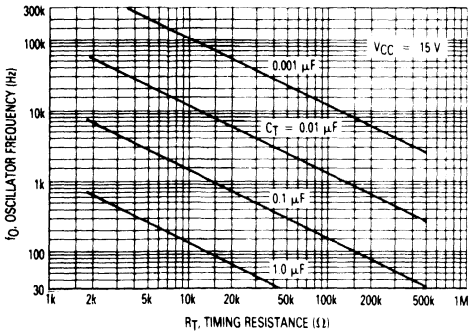


FIGURE 4 — OPEN LOOP VOLTAGE GAIN AND PHASE versus FREQUENCY

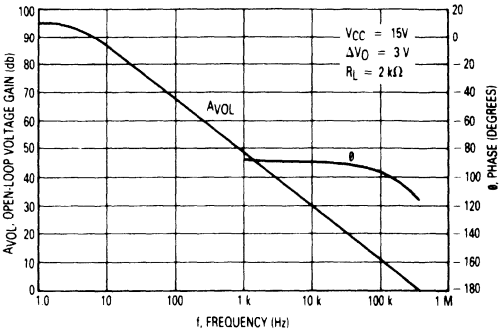


FIGURE 5 — PERCENT DEAD-TIME versus OSCILLATOR FREQUENCY

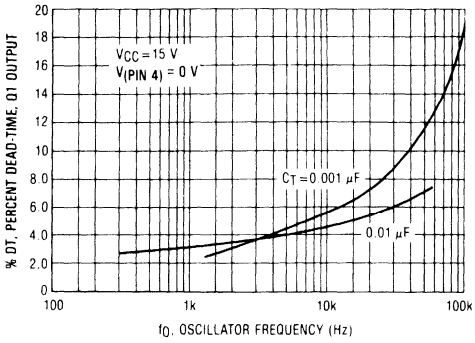


FIGURE 6 — PERCENT DUTY CYCLE versus DEAD-TIME CONTROL VOLTAGE

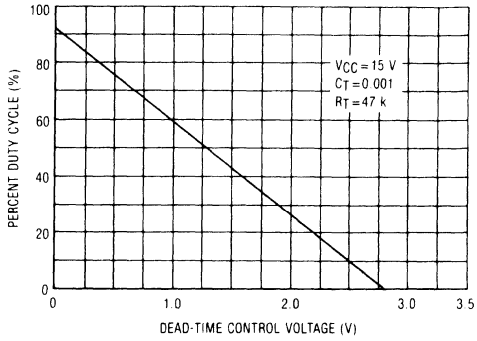


FIGURE 7 — EMITTER FOLLOWER CONFIGURATION OUTPUT-SATURATION VOLTAGE versus EMITTER CURRENT

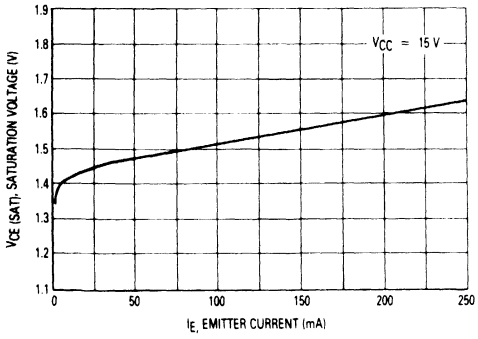


FIGURE 8 — COMMON EMITTER CONFIGURATION OUTPUT-SATURATION VOLTAGE versus COLLECTOR CURRENT

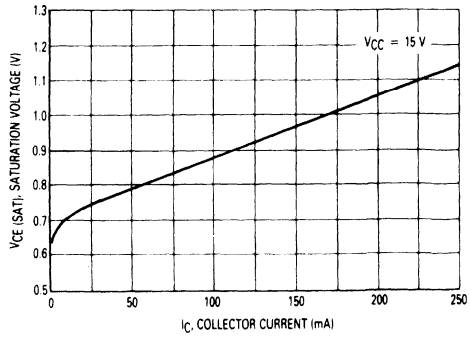


FIGURE 9 — STANDBY-SUPPLY CURRENT versus SUPPLY VOLTAGE

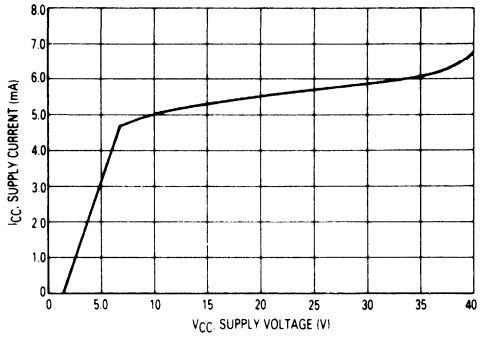


FIGURE 10 — ERROR AMPLIFIER CHARACTERISTICS

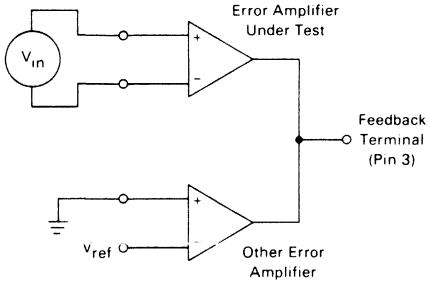


FIGURE 11 — DEAD-TIME AND FEEDBACK CONTROL TEST CIRCUIT

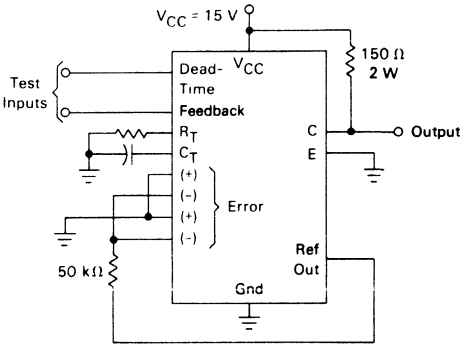


FIGURE 12 — COMMON-EMITTER CONFIGURATION TEST CIRCUIT AND WAVEFORM

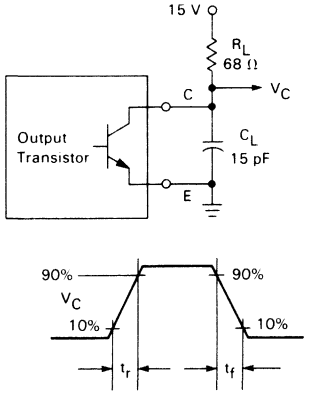


FIGURE 13 — EMITTER-FOLLOWER CONFIGURATION TEST CIRCUIT AND WAVEFORM

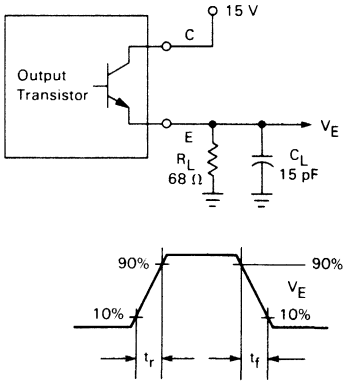
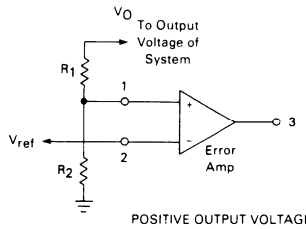
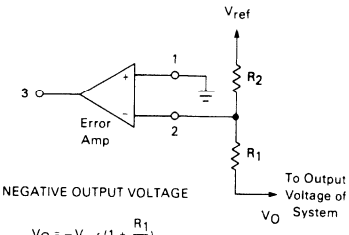


FIGURE 14 — ERROR AMPLIFIER SENSING TECHNIQUES



POSITIVE OUTPUT VOLTAGE

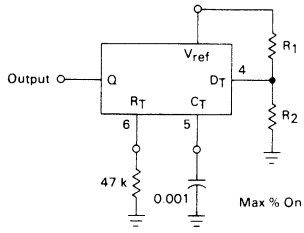
$$V_O = V_{ref}\left(1 + \frac{R_1}{R_2}\right)$$



NEGATIVE OUTPUT VOLTAGE

$$V_O = -V_{ref}\left(1 + \frac{R_1}{R_2}\right)$$

FIGURE 15 — DEAD-TIME CONTROL CIRCUIT



$$\text{Max \% On Time} \approx 92 - \left(\frac{160}{1 + \frac{R1}{R2}}\right)$$

FIGURE 16 — SOFT-START CIRCUIT

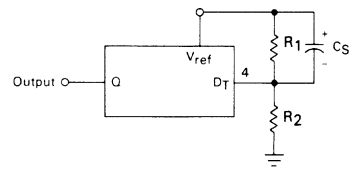


FIGURE 17 — SLAVING TWO OR MORE CONTROL CIRCUITS

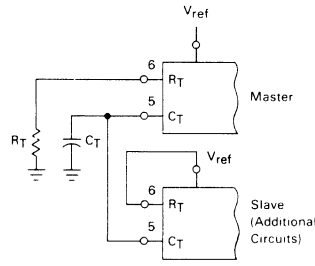
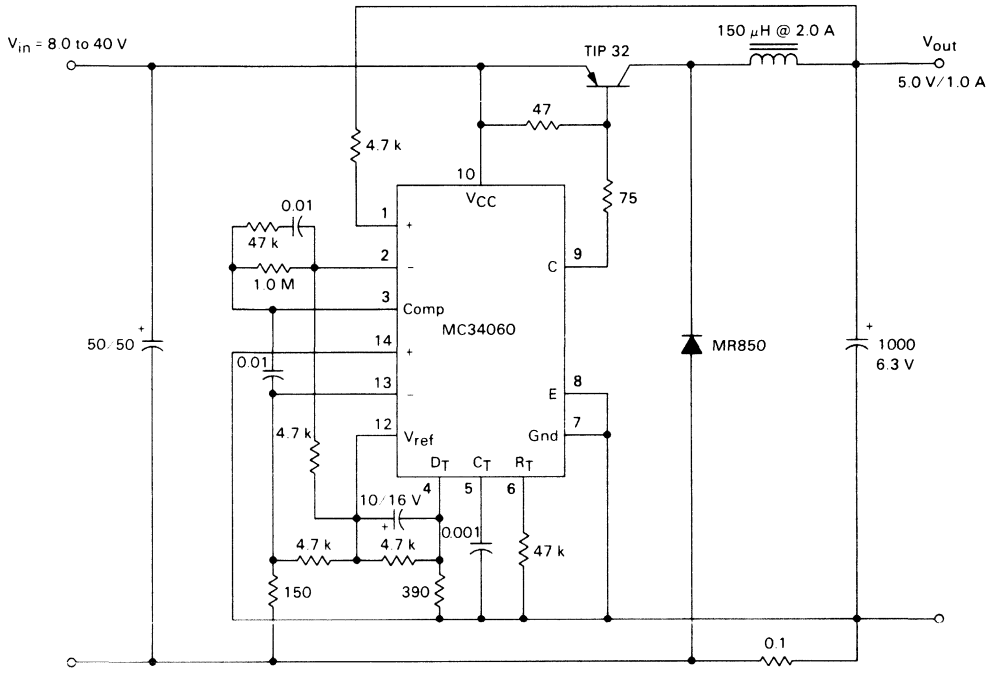
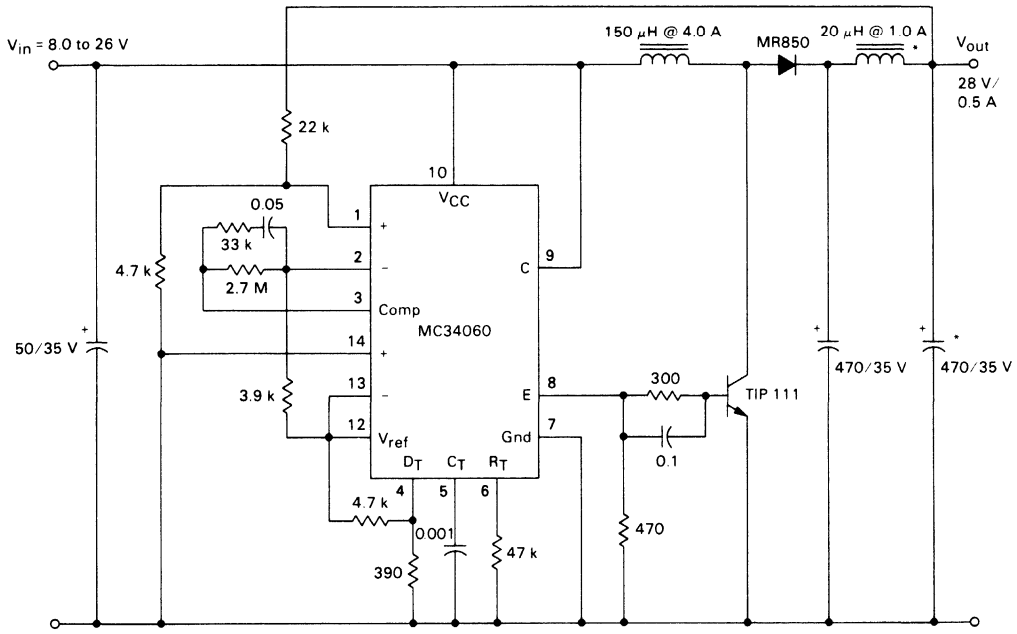


FIGURE 18 — STEP-DOWN CONVERTER WITH SOFT-START AND OUTPUT CURRENT LIMITING



TEST	CONDITIONS	RESULTS
Line Regulation	V_{in} = 8.0 V to 40 V, I_O = 1.0 A	25 mV 0.5%
Load Regulation	V_{in} = 12 V, I_O = 1.0 mA to 1.0 A	3.0 mV 0.06%
Output Ripple	V_{in} = 12 V, I_O = 1.0 A	75 mV p-p P.A.R.D.
Short Circuit Current	V_{in} = 12 V, R_L = 0.1 Ω	1.6 A
Efficiency	V_{in} = 12 V, I_O = 1.0 A	73%

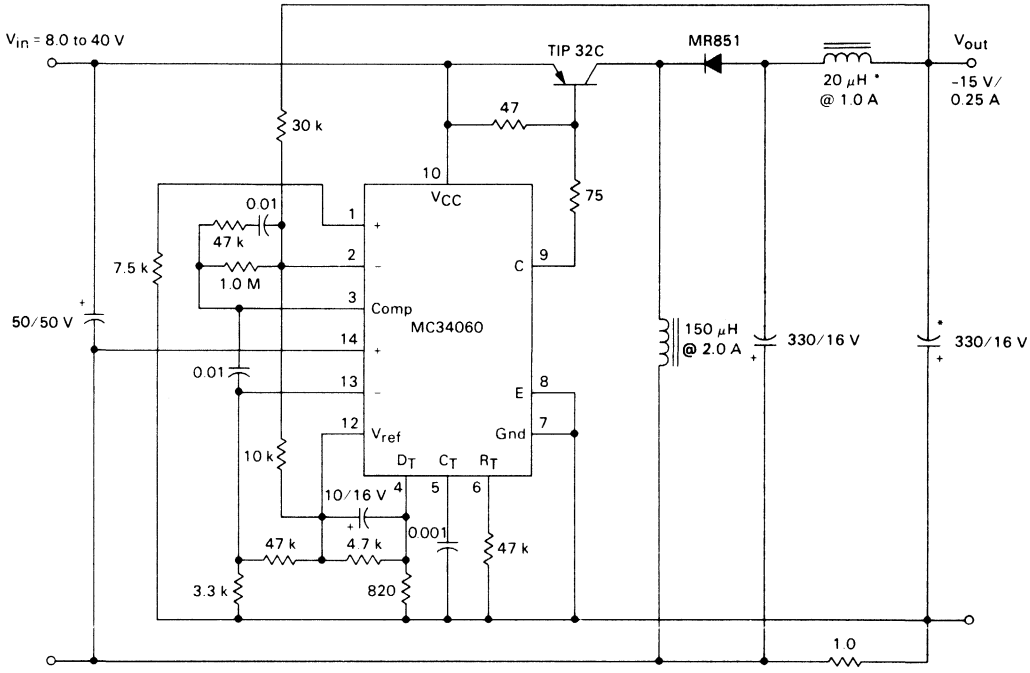
FIGURE 19 — STEP-UP CONVERTER



TEST	CONDITIONS	RESULTS
Line Regulation	V_{in} = 8.0 V to 26 V, I_O = 0.5 A	40 mV 0.14%
Load Regulation	V_{in} = 12 V, I_O = 1.0 mA to 0.5 A	5.0 mV 0.18%
Output Ripple	V_{in} = 12 V, I_O = 0.5 A	24 mV p-p P.A.R.D.
Efficiency	V_{in} = 12 V, I_O = 0.5 A	75%

*Optional circuit to minimize output ripple.

FIGURE 20 — STEP-UP/DOWN VOLTAGE INVERTING CONVERTER WITH SOFT-START AND CURRENT LIMITING



TEST	CONDITIONS	RESULTS
Line Regulation	V_{in} = 8.0 V to 40 V, I_O = 250 mA	52 mV 0.35%
Load Regulation	V_{in} = 12 V, I_O = 1 mA to 250 mA	47 mV 0.32%
Output Ripple	V_{in} = 12 V, I_O = 250 mA	10 mV p.p. P.A.R.D.
Short Circuit Current	V_{in} = 12 V, R_L = 0.1 Ω	330 mA
Efficiency	V_{in} = 12 V, I_O = 250 mA	86%

* Optional circuit to minimize output ripple

MOTOROLA

MC34060A
MC35060A
MC33060A

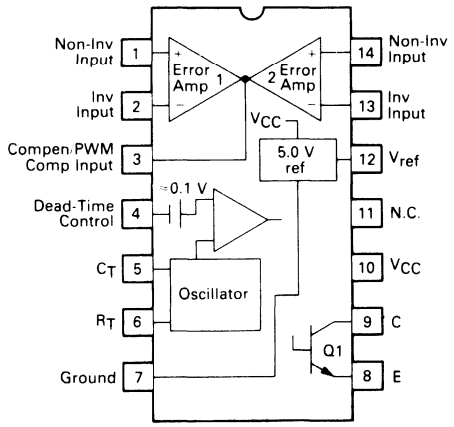
PRECISION SWITCHMODE PULSE WIDTH MODULATION CONTROL CIRCUITS

The MC35060A/MC34060A/MC33060A are low cost fixed frequency, pulse width modulation control circuits designed primarily for single ended SWITCHMODE power supply control. These devices feature:

The MC34060A is specified over the commercial operating range of 0° to +70°C. The MC35060A is specified over the full military range of −55° to +125°C. The MC33060A is specified over the vehicular temperature range of −40° to +85°C.

- Complete Pulse Width Modulation Control Circuitry
- On-Chip Oscillator With Master or Slave Operation
- On-Chip Error Amplifiers
- On-Chip 5.0 Volt Reference, 1.5% Accuracy
- Adjustable Dead Time Control
- Uncommitted Output Transistor Rated to 500 mA Source or Sink
- Undervoltage Lockout
- Available in Surface Mount Package

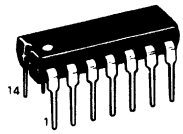
PIN CONNECTIONS



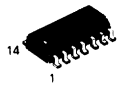
(top view)

PRECISION SWITCHMODE PULSE WIDTH MODULATION CONTROL CIRCUITS

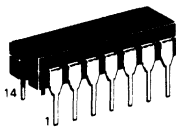
SILICON MONOLITHIC INTEGRATED CIRCUITS



P SUFFIX
PLASTIC PACKAGE
CASE 646-06



D SUFFIX
PLASTIC PACKAGE
CASE 751A-02
SO-14



L SUFFIX
CERAMIC PACKAGE
CASE 632-08

ORDERING INFORMATION

Device	Temperature Range	Package
MC35060AL	−55° to +125°C	Ceramic DIP
MC34060AD	0° to +70°C	SO-14 Plastic DIP
MC34060AP		Plastic DIP
MC33060AD	−40° to +85°C	SO-14 Plastic DIP
MC33060AP		Plastic DIP

FIGURE 1 — BLOCK DIAGRAM

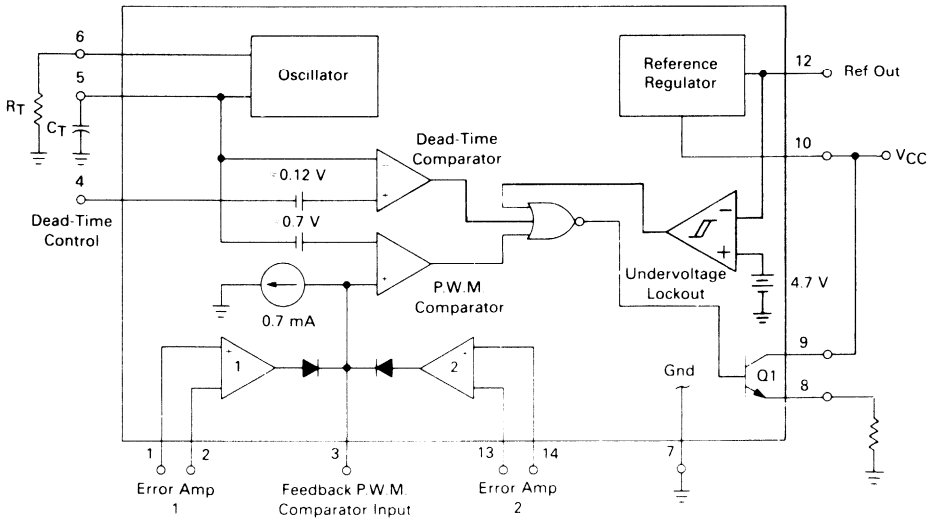
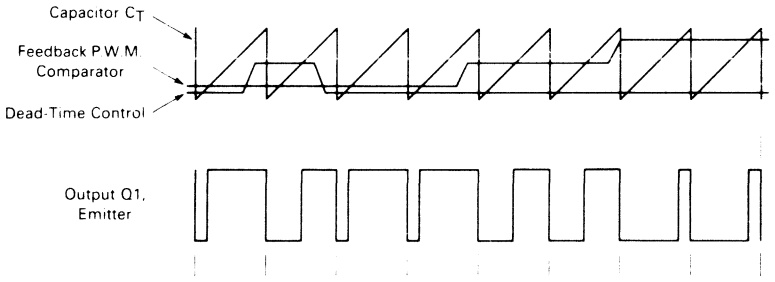


FIGURE 2 — TIMING DIAGRAM



Description

The MC35060A/34060A/33060A is a fixed-frequency pulse width modulation control circuit, incorporating the primary building blocks required for the control of a switching power supply. (See Figure 1.) An internal linear sawtooth oscillator is frequency-programmable by two external components, R_T and C_T. The approximate oscillator frequency is determined by:

$$f_{osc} \cong \frac{1.2}{R_T \bullet C_T}$$

For more information refer to Figure 3.

Output pulse width modulation is accomplished by comparison of the positive sawtooth waveform across capacitor C_T to either of two control signals. The output is enabled only during that portion of time when the sawtooth voltage is greater than the control signals. Therefore, an increase in control-signal amplitude causes a corresponding linear decrease of output pulse width. (Refer to the timing diagram shown in Figure 2.)

The control signals are external inputs that can be fed into the dead-time control, the error amplifier inputs, or the feedback input. The dead-time control comparator has an effective 120 mV input offset which limits the minimum output dead time to approximately the first 4% of the sawtooth-cycle time. This would result in a maximum duty cycle of 96%. Additional dead time may be imposed on the output by setting the dead time-control input to a fixed voltage, ranging between 0 to 3.3 V.

The pulse width modulator comparator provides a means for the error amplifiers to adjust the output pulse width from the maximum percent on-time, established by the dead time control input, down to zero, as the voltage at the feedback pin varies from 0.5 to 3.5 V. Both error amplifiers have a common-mode input range from −0.3 V to (V_{CC} − 2.0 V), and may be used to sense power supply output voltage and current. The error-amplifer outputs are active high and are ORed together at the non-inverting input of the pulse-width modulator comparator. With this configuration, the amplifier that demands minimum output on time, dominates control of the loop.

The MC35060A/34060A/33060A has an internal 5.0 V reference capable of sourcing up to 10 mA of load currents for external bias circuits. The reference has an internal accuracy of ±1.5% with a typical thermal drift of less than 50 mV over an operating temperature range of 0° to +70°C.

MAXIMUM RATINGS (Full operating ambient temperature range applies unless otherwise noted)

Rating	Symbol	MC35060A	MC34060A	MC33060A	Unit
Power Supply Voltage	V_{CC}	42	42	42	V
Collector Output Voltage	V_C	42	42	42	V
Collector Output Current (Note 1)	I_C	500	500	500	mA
Amplifier Input Voltage Range	V_{IR}	−0.3 to +42	−0.3 to +42	−0.3 to +42	V
Power Dissipation @ T_A = 45 C	P_D	1000	1000	1000	mW
Operating Junction Temperature Plastic Package Ceramic Package	T_J	 — 150	 125 —	 125 —	°C
Operating Ambient Temperature Range	T_A	−55 to +125	0 to 70	−40 to +85	°C
Storage Temperature Range Plastic Package Ceramic Package	T_{stg}	 — −65 to +150	 −55 to +125 —	 −55 to +125 —	°C

Note 1: Maximum thermal limits must be observed.

THERMAL CHARACTERISTICS

Characteristic	Symbol	L Suffix Ceramic Package	P Suffix Plastic Package	D Suffix Plastic Package	Unit
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	100	80	120	°C/W
Derating Ambient Temperature	T_A	50	45	45	°C

RECOMMENDED OPERATING CONDITIONS

Condition/Value	Symbol	MC35060A/MC34060A/MC33060A Min	Typ	Max	Unit
Power Supply Voltage	V_{CC}	7.0	15	40	V
Collector Output Voltage	V_C	—	30	40	V
Collector Output Current	I_C	—	—	200	mA
Amplifier Input Voltage	V_{in}	−0.3	—	V_{CC} − 2	V
Current Into Feedback Terminal	I_{fb}	—	—	0.3	mA
Reference Output Current	I_{ref}	—	—	10	mA
Timing Resistor	R_T	1.8	47	500	kΩ
Timing Capacitor	C_T	0.0047	0.001	10	μF
Oscillator Frequency	f_{osc}	1.0	25	200	kHz
PWM Input Voltage (Pins 3 and 4)	—	−0.3	—	5.3	V

ELECTRICAL CHARACTERISTICS (V_{CC} = 15 V, C_T = 0.01 μF, R_T = 12 kΩ unless otherwise noted. For typical values T_A = 25°C, for min/max values T_A is the operating ambient temperature range that applies unless otherwise noted.

Characteristic	Symbol	MC35060A/MC34060A/MC33060A Min	Typ	Max	Unit
REFERENCE SECTION					
Reference Voltage (I_O = 1.0 mA, T_A = 25°C) (I_O = 1.0 mA)	V_{ref}	 4.925 4.9	 5.0 —	 5.075 5.1	V
Line Regulation **(V_{CC} = 7.0 V to 40 V, I_O = 1.0 mA)**	Reg_{line}	—	2.0	25	mV
Load Regulation (I_O = 1.0 mA to 10 mA)	Reg_{load}	—	2.0	15	mV
Short-Circuit Output Current (V_{ref} = 0 V)	I_{SC}	15	35	75	mA
OUTPUT SECTION					
Collector Off-State Current (V_{CC} = 40 V, V_{CE} = 40 V)	$I_{C(off)}$	—	2.0	100	μA
Emitter Off-State Current (V_{CC} = 40 V, V_C = 40 V, V_E 0 V)	$I_{E(off)}$	—	—	100	μA
Collector-Emitter Saturation Voltage (Note 2) Common-Emitter (V_E = 0 V, I_C = 200 mA) Emitter-Follower (V_C = 15 V, I_E 200 mA)	$V_{sat(C)}$ $V_{sat(E)}$	— —	1.1 1.5	1.5 2.5	V
Output Voltage Rise Time (T_A 25 C) Common-Emitter (See Figure 12) Emitter-Follower (See Figure 13)	t_r	 — —	 100 100	 200 200	ns
Output Voltage Fall Time (T_A 25 C) Common-Emitter (See Figure 12) Emitter-Follower (See Figure 13)	t_f	 — —	 40 40	 100 100	ns

Characteristic	Symbol	MC35060A/MC34060A/MC33060A Min	Typ	Max	Unit
ERROR AMPLIFIER SECTIONS					
Input Offset Voltage ($V_{O[Pin\ 3]}$ = 2.5 V)	V_{IO}	—	2.0	10	mV
Input Offset Current ($V_{C[Pin\ 3]}$ = 2.5 V)	I_{IO}	—	5.0	250	nA
Input Bias Current ($V_{O[Pin\ 3]}$ = 2.5 V)	I_{IB}	—	0.1	2.0	μA
Input Common-Mode Voltage Range (V_{CC} = 40 V)	V_{ICR}	0 to V_{CC} 2.0	—	—	V
Inverting Input Voltage Range	$V_{IR(INV)}$	0.3 to V_{CC} 2.0	—	—	V
Open Loop Voltage Gain (ΔV_O = 3.0 V, V_O = 0.5 to 3.5 V, R_L 2.0 kΩ)	A_{VOL}	70	95	—	dB

Note 2: Low duty cycle techniques are used during test to maintain junction temperature as close to ambient temperatures as possible.

ELECTRICAL CHARACTERISTICS (V_{CC} = 15 V, C_T = 0.01 μF, R_T = 12 kΩ unless otherwise noted. For typical values T_A = 25°C, for min/max values T_A is the operating ambient temperature range that applies unless otherwise noted.)

Characteristic	Symbol	MC35060A/MC34060A/MC33060A Min	Typ	Max	Unit
ERROR AMPLIFIER SECTIONS (Continued)					
Unity-Gain Crossover Frequency (V_O = 0.5 to 3.5 V, R_L = 2.0 kΩ)	f_c	—	600	—	kHz
Phase Margin at Unity-Gain (V_O = 0.5 to 3.5 V, R_L = 2.0 kΩ)	ϕ_m	—	65	—	deg.
Common-Mode Rejection Ratio (V_{CC} = 40 V, V_{in} = 0 V to 38 V)	CMRR	65	90	—	dB
Power Supply Rejection Ratio (ΔV_{CC} = 33 V, V_O = 2.5 V, R_L = 2.0 kΩ)	PSRR	—	100	—	dB
Output Sink Current ($V_{O[Pin\ 3]}$ = 0.7 V)	I_O-	0.3	0.7	—	mA
Output Source Current ($V_{O[Pin\ 3]}$ = 3.5 V)	I_O+	−2.0	−4.0	—	mA
PWM COMPARATOR SECTION (Test circuit Figure 11)					
Input Threshold Voltage (Zero Duty Cycle)	V_{TH}	—	3.5	4.5	V
Input Sink Current ($V_{[Pin\ 3]}$ = 0.7 V)	I_I-	0.3	0.7	—	mA
DEAD-TIME CONTROL SECTION (Test Circuit Figure 11)					
Input Bias Current (Pin 4) (V_{in} = 0 to 5.25 V)	$I_{IB(DT)}$	—	−1.0	−10	μA
Maximum Output Duty Cycle	DC_{max}				%
(V_{in} = 0 V, C_T = 0.01 μF, R_T = 12 kΩ)		90	96	100	
(V_{in} = 0 V, C_T = 0.001 μF, R_T = 47 kΩ)		—	92	—	
Input Threshold Voltage (Pin 4)	V_{TH}				V
(Zero Duty Cycle)		—	2.8	3.3	
(Maximum Duty Cycle)		0	—	—	
OSCILLATOR SECTION					
Frequency (C_T = 0.01 μF, R_T = 12 kΩ)	f_{osc}				kHz
T_A = 25°C		9.7	10.5	11.3	
T_A = T_{low} to T_{high}		9.5	—	12.5	
(C_T = 0.001 μF, R_T = 47 kΩ)		—	25	—	
Standard Deviation of Frequency* (C_T = 0.001 μF, R_T = 47 kΩ)	σf_{osc}	—	1.5	—	%
Frequency Change with Voltage (V_{CC} = 7.0 V to 40 V)	$\Delta f_{osc}(\Delta V)$	—	0.5	2.0	%
Frequency Change with Temperature	$\Delta f_{osc}(\Delta T)$				%
(ΔT_A = T_{low} to T_{high})		—	4.0	—	
(C_T = 0.01 μF, R_T = 12 kΩ)		—	—	—	
UNDERVOLTAGE LOCKOUT SECTION					
Turn-On Threshold (V_{CC} increasing, I_{ref} = 1.0 mA)	V_{th}	4.0	4.7	5.5	V
Hysteresis	V_H	50	150	300	mV
TOTAL DEVICE					
Standby Supply Current	I_{CC}				mA
(Pin 6 at V_{ref}, all other inputs and outputs open)					
(V_{CC} = 15 V)		—	5.5	10	
(V_{CC} = 40 V)		—	7.0	15	
Average Supply Current ($V_{[Pin\ 4]}$ = 2.0 V, C_T = 0.001 μF, R_T = 47 kΩ). See Figure 11.	I_S	—	7.0	—	mA

*Standard deviation is a measure of the statistical distribution about the mean as derived from the formula; $\sigma = \sqrt{\frac{\sum_{n=1}^{N} (X_n - x)^2}{N-1}}$

FIGURE 3 — OSCILLATOR FREQUENCY versus TIMING RESISTANCE

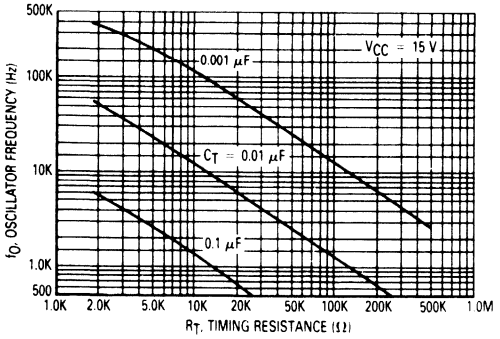


FIGURE 4 — OPEN-LOOP VOLTAGE GAIN AND PHASE versus FREQUENCY

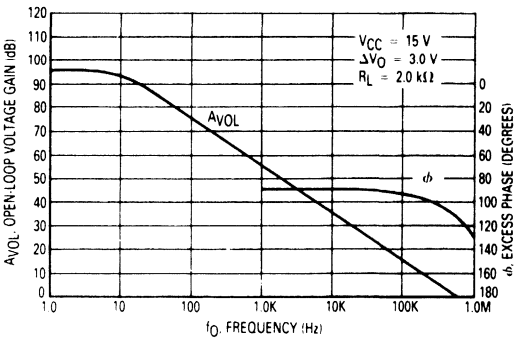


FIGURE 5 — PERCENT DEAD-TIME versus OSCILLATOR FREQUENCY

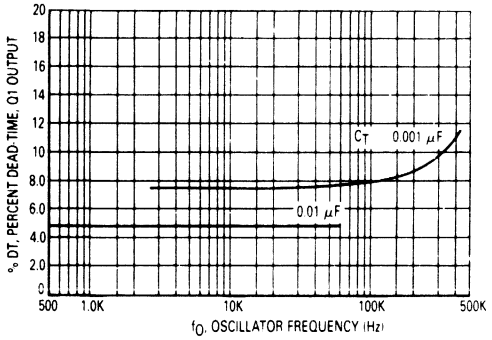


FIGURE 6 — PERCENT DUTY CYCLE versus DEAD-TIME CONTROL VOLTAGE

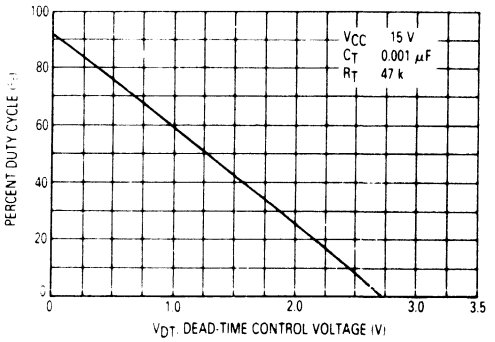


FIGURE 7 — EMITTER FOLLOWER CONFIGURATION OUTPUT SATURATION VOLTAGE versus EMITTER CURRENT

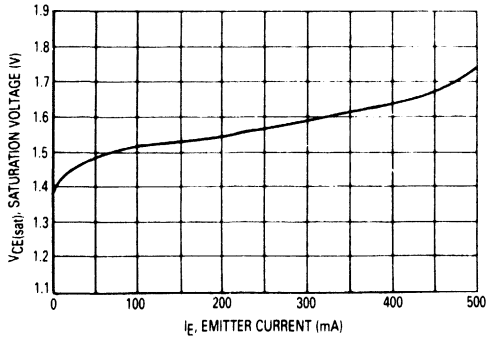


FIGURE 8 — COMMON EMITTER CONFIGURATION OUTPUT SATURATION VOLTAGE versus COLLECTOR CURRENT

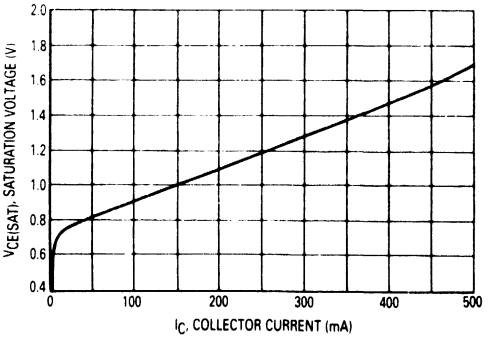


FIGURE 9 — STANDBY SUPPLY CURRENT versus SUPPLY VOLTAGE

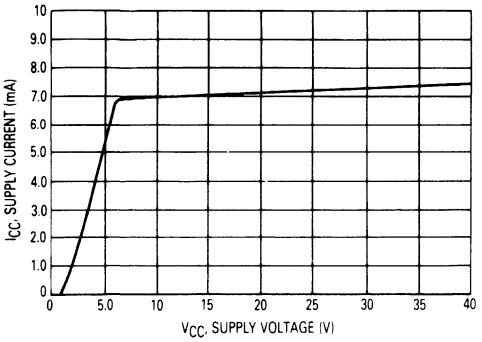


FIGURE 10 — UNDERVOLTAGE LOCKOUT THRESHOLDS versus REFERENCE LOAD CURRENT

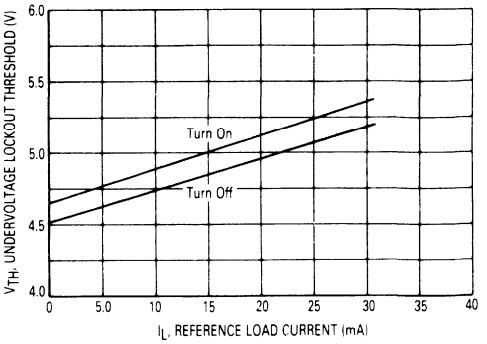


FIGURE 11 — ERROR AMPLIFIER CHARACTERISTICS

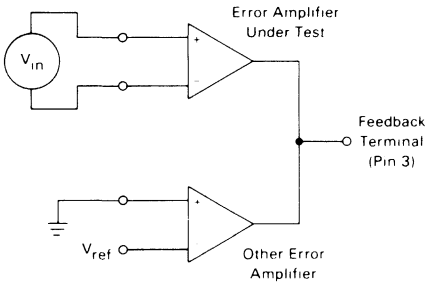


FIGURE 12 — DEAD-TIME AND FEEDBACK CONTROL TEST CIRCUIT

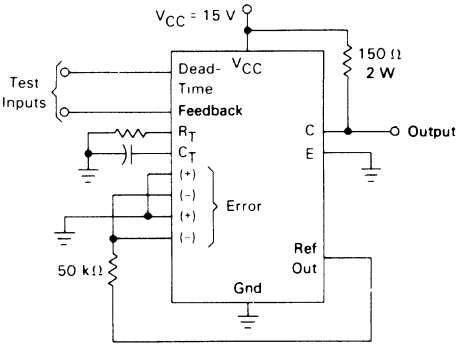


FIGURE 13 — COMMON-EMITTER CONFIGURATION TEST CIRCUIT AND WAVEFORM

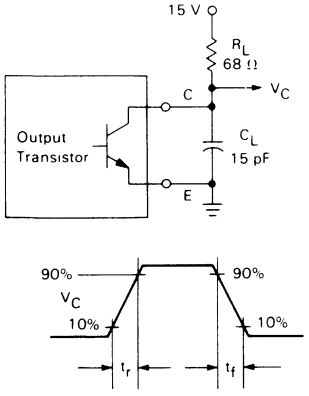


FIGURE 14 — EMITTER-FOLLOWER CONFIGURATION TEST CIRCUIT AND WAVEFORM

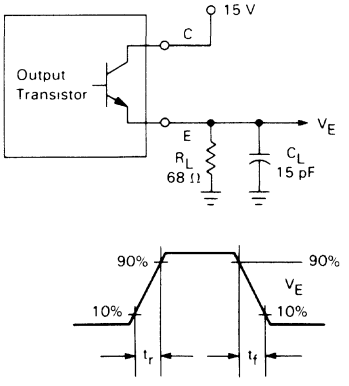
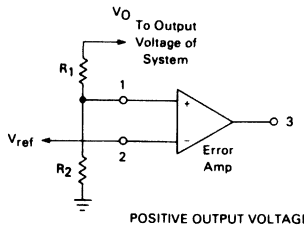
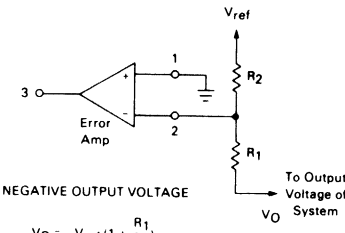


FIGURE 15 — ERROR AMPLIFIER SENSING TECHNIQUES



POSITIVE OUTPUT VOLTAGE

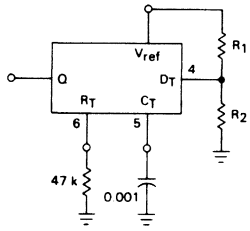
$$V_O = V_{ref}\left(1 + \frac{R_1}{R_2}\right)$$



NEGATIVE OUTPUT VOLTAGE

$$V_O = -V_{ref}\left(1 + \frac{R_1}{R_2}\right)$$

FIGURE 16 — DEAD-TIME CONTROL CIRCUIT



$$\text{Max \% On Time} \approx 92 - \left(\frac{160}{1 + \frac{R1}{R2}}\right)$$

FIGURE 17 — SOFT-START CIRCUIT

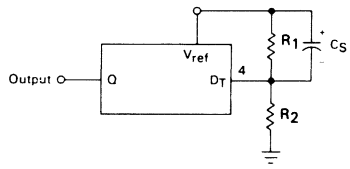


FIGURE 18 — SLAVING TWO OR MORE CONTROL CIRCUITS

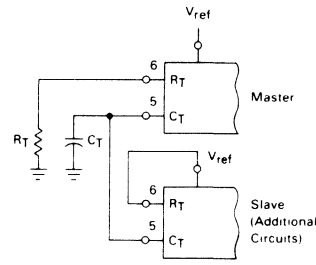
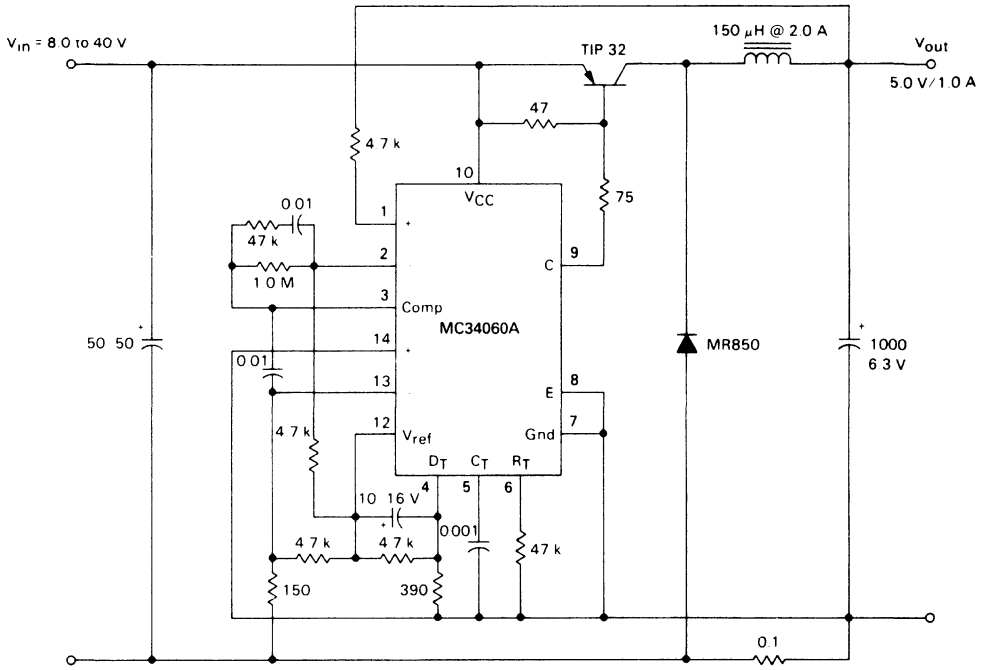
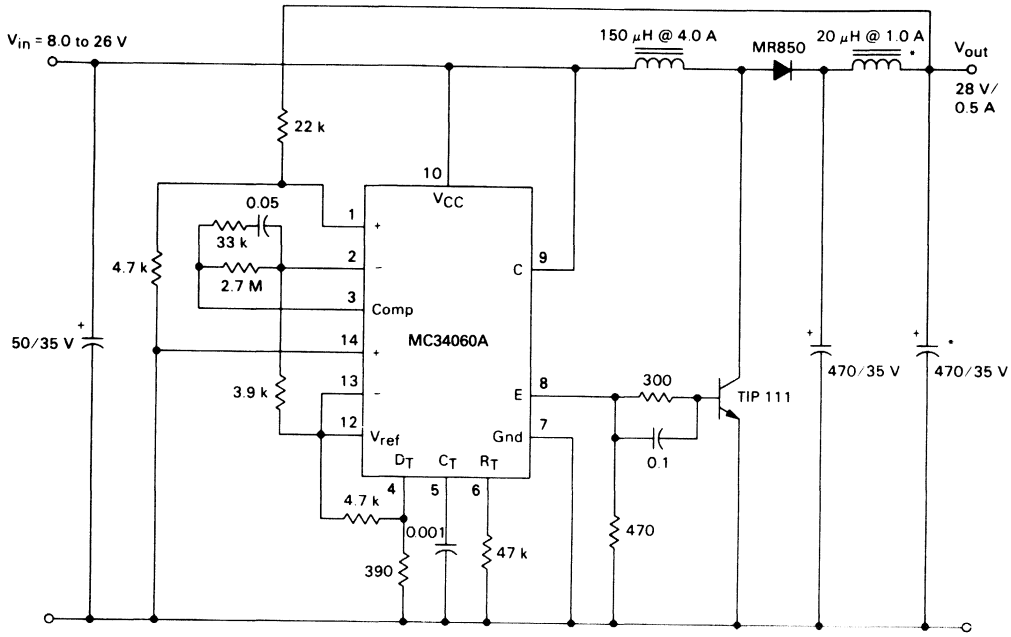


FIGURE 19 — STEP-DOWN CONVERTER WITH SOFT-START AND OUTPUT CURRENT LIMITING



TEST	CONDITIONS	RESULTS
Line Regulation	V_{in} = 8.0 V to 40 V, I_O = 1.0 A	25 mV 0.5%
Load Regulation	V_{in} = 12 V, I_O = 1.0 mA to 1.0 A	3.0 mV 0.06%
Output Ripple	V_{in} = 12 V, I_O = 1.0 A	75 mV p-p P.A.R.D.
Short Circuit Current	V_{in} = 12 V, R_L = 0.1 Ω	1.6 A
Efficiency	V_{in} = 12 V, I_O = 1.0 A	73%

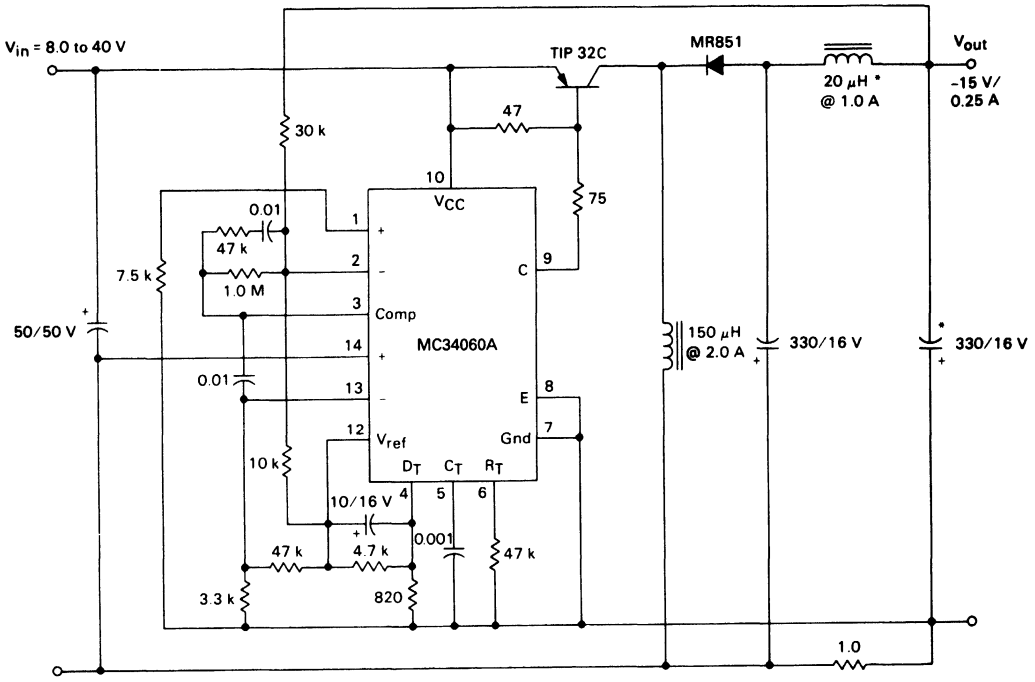
FIGURE 20 — STEP-UP CONVERTER



TEST	CONDITIONS	RESULTS
Line Regulation	V_{in} = 8.0 V to 26 V, I_O = 0.5 A	40 mV 0.14%
Load Regulation	V_{in} = 12 V, I_O = 1.0 mA to 0.5 A	5.0 mV 0.18%
Output Ripple	V_{in} = 12 V, I_O = 0.5 A	24 mV p-p P.A.R.D.
Efficiency	V_{in} = 12 V, I_O = 0.5 A	75%

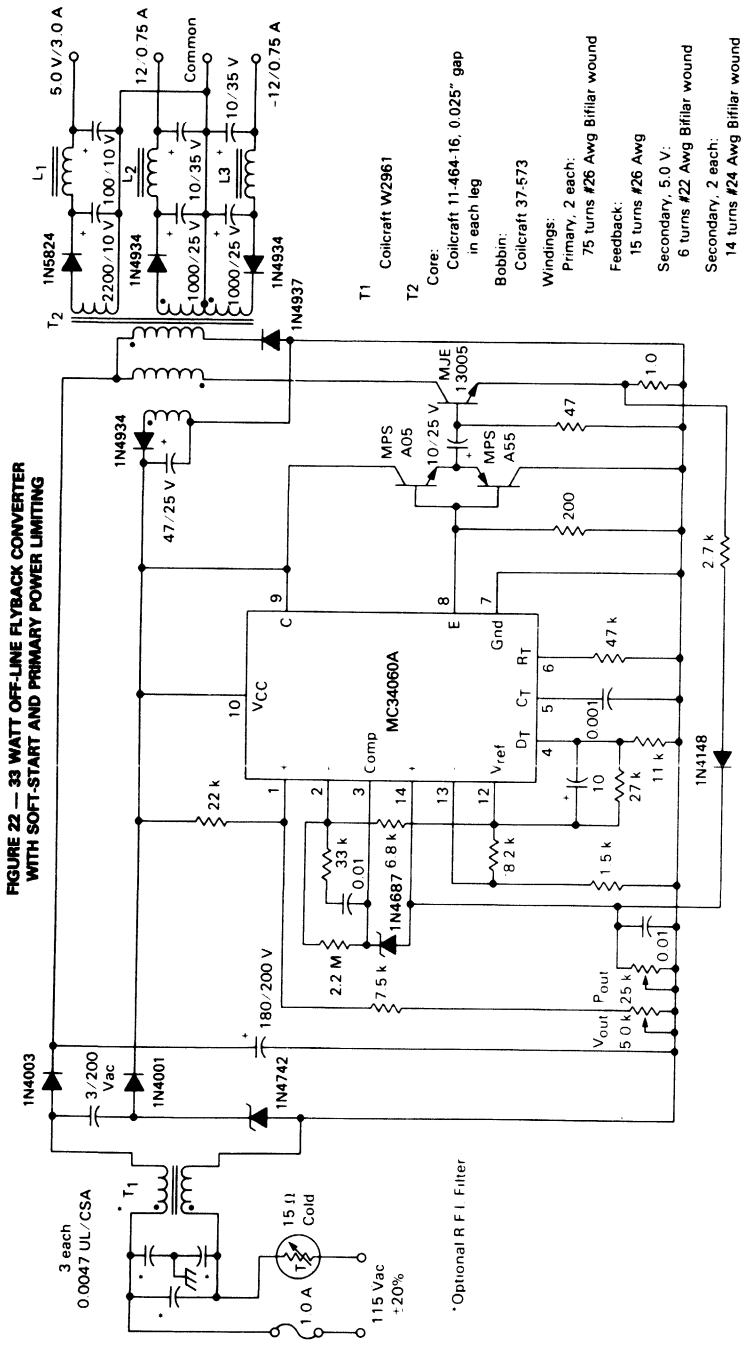
*Optional circuit to minimize output ripple

FIGURE 21 — STEP-UP/DOWN VOLTAGE INVERTING CONVERTER WITH SOFT-START AND CURRENT LIMITING



TEST	CONDITIONS	RESULTS
Line Regulation	V_{in} = 8.0 V to 40 V, I_O = 250 mA	52 mV 0.35%
Load Regulation	V_{in} = 12 V, I_O = 1 mA to 250 mA	47 mV 0.32%
Output Ripple	V_{in} = 12 V, I_O = 250 mA	10 mV p.p. P.A.R.D.
Short Circuit Current	V_{in} = 12 V, R_L = 0.1 Ω	330 mA
Efficiency	V_{in} = 12 V, I_O = 250 mA	86%

*Optional circuit to minimize output ripple.



TEST	CONDITIONS	RESULTS
Line Regulation 5.0 V	V_{in} = 95 to 135 Vac, I_O = 3.0 A	20 mV, 0.40%
Line Regulation +12 V	V_{in} = 95 to 135 Vac, I_O = 0.75 A	52 mV, 0.26%
Load Regulation 5.0 V	V_{in} = 115 Vac, I_O = 1.0 to 4.0 A	476 mV, 9.5%
Load Regulation +12 V	V_{in} = 115 Vac, I_O = ±0.4 to ±0.9 A	300 mV, 2.5%
Output Ripple 5.0 V	V_{in} = 115 Vac, I_O = 3.0 A	45 mV p-p PARD
Output Ripple +12 V	V_{in} = 115 Vac, I_O = 0.75 A	75 mV p-p PARD
Efficiency	V_{in} = 115 Vac, I_O 5.0 V, 3.0 A I_O ±12 = ±0.75 A	74%

FIGURE 22 — 33 WATT OFF-LINE FLYBACK CONVERTER WITH SOFT-START AND PRIMARY POWER LIMITING

MOTOROLA

MC34061

Advance Information

THREE-TERMINAL OVERVOLTAGE "CROWBAR" SENSING CIRCUIT

The MC34061 overvoltage protection (OVP) circuit, in combination with two external programming resistors and a "crowbar" SCR, protects sensitive electronic circuitry from overvoltage damage. It senses an overvoltage condition and quickly "crowbars," or short circuits, the supply. An external capacitor may be used to program a minimum overvoltage duration before tripping, thus providing noise immunity.

This three-terminal circuit provides a cost-effective means of protecting either positive or negative power supplies. The unique design of the MC34061 eliminates trip voltage and temperature drift errors due to SCR gate variations.

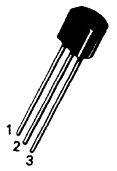
The basic MC34061 device offers a ±2% tolerance on the sense trip voltage. The device is available in a low-cost plastic package and features:

- Unique Three-Terminal Design
- SCR Gate Drive Output of 200 mA
- Sense Voltage of 2.5 V ±2%
- Hysteresis of 250 mV
- Wide Supply Range: 4.0 V ≤ V_{CC} ≤ 41 V

THREE-TERMINAL PROGRAMMABLE OVERVOLTAGE SENSING CIRCUIT

SILICON MONOLITHIC INTEGRATED CIRCUIT

P SUFFIX
PLASTIC PACKAGE
CASE 29-04



Pin 1. V_{CC}
2. Drive Output
3. Sense

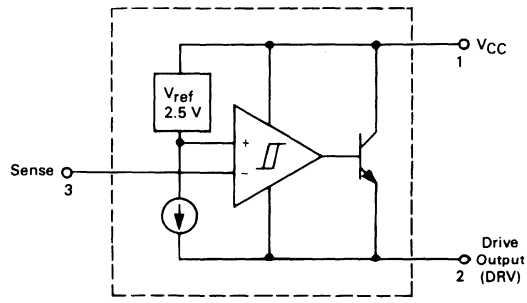
MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Operating Voltage	$V_{CC} - V_{DRV}$	40	Vdc
Sense Voltage	V_{Sense}	40	Vdc
Drive Output Current	I_{DRV}	Internally Limited	mA
Operating Ambient Temperature Range	T_A	0 to +70	°C
Operating Junction Temperature	T_J	150	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C

ORDERING INFORMATION

Device	Temperature Range	Package
MC34061P	0 to +70° C	Plastic TO-92

FUNCTIONAL BLOCK DIAGRAM



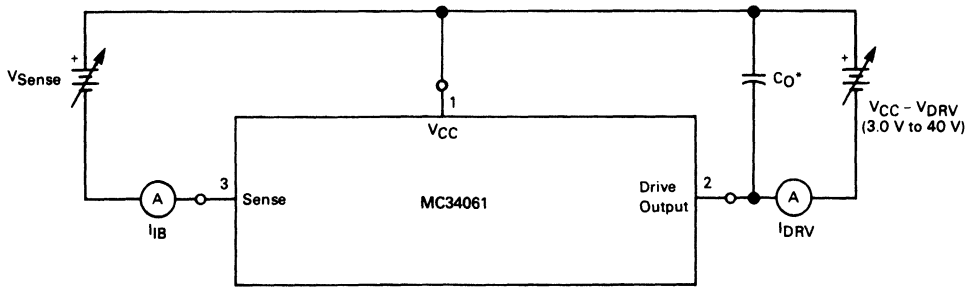
This document contains information on a new product. Specifications and information herein are subject to change without notice.

ELECTRICAL CHARACTERISTICS (V_{CC} – V_{DRV} = 5.0 V; T_A = T_{low} to T_{high} [see Note 1] unless otherwise specified)

Characteristic	Symbol	Min	Typ	Max	Unit
Operating Voltage Range	$V_{CC} - V_{DRV}$	3.0	—	40	Vdc
Sense Trip Voltage T_A = 25°C T_{low} to T_{high} (Note 1)	V_{Sense}	 2.45 2.4	 2.5 2.5	 2.55 2.6	Vdc
Line Regulation, V_{Sense} (3.0 ≤ V_{CC} – V_{DRV} ≤ 40 V) T_A = 25°C T_{low} to T_{high} (Note 1)	Reg_{line}	 — —	 0.001 0.001	 0.01 0.02	%/V
Input Bias Current, Sense Pin At Trip Point (Note 2) After Trip (V_{Sense} = 3.0 V)	I_{IB}	 — —	 0.3 0.9	 2.0 6.0	μA
Hysteresis Voltage, Sense Pin	V_H	—	250	—	mV
Drive Output Current, ON State T_J = 25°C T_{low} to T_{high} (Note 1)	$I_{DRV(on)}$	 130 90	 200 —	 300 350	mA
Drive Output Current, OFF State V_{CC} – V_{DRV} = 5.0 V 3.0 V ≤ V_{CC} – V_{DRV} ≤ 40 V	$I_{DRV(off)}$	 0.2 0.2	 0.6 0.6	 1.0 1.5	mA
Drive Output Current Slew Rate T_A = 25°C	di/dt	—	2.0	—	A/μs
Drive Output V_{CC} Transient Rejection V_{CC} – V_{DRV} = 0 V to 15 V at dV/dt = 200 V/μs; V_{Sense} = 0 V; T_A = 25°C	$\Delta I_{DRV(trans)}$	—	1.0	—	mA (Peak)
Propagation Delay Time (T_A = 25°C) 500 mV Overdrive	t_{PLH}	—	500	—	ns

NOTES:
(1) T_{low} to T_{high} = 0°C to 70°C
(2) This specification is an engineering estimate based on design parameters, and is not tested.

FIGURE 1 — STANDARD TEST CIRCUIT



*A 1.0 μF tantalum or 10 μF electrolytic capacitor may be necessary to compensate for lead inductance when measuring Hysteresis Voltage. When this capacitor is used, it should be placed as close as possible to the device package.

TYPICAL CHARACTERISTICS

FIGURE 2 — DRIVE CURRENT versus SENSE VOLTAGE

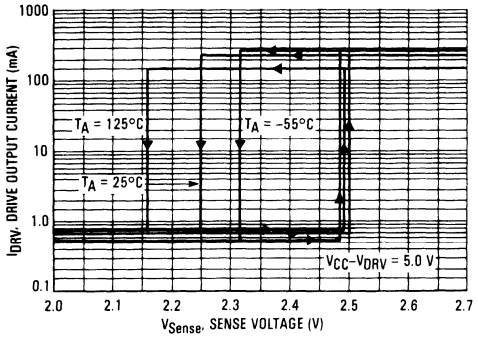


FIGURE 3 — SENSE TRIP VOLTAGE versus TEMPERATURE

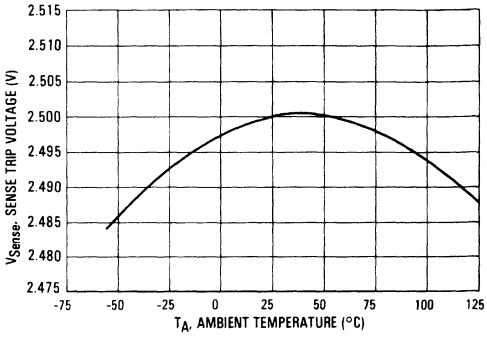


FIGURE 4 — OFF STATE DRIVE CURRENT versus SUPPLY VOLTAGE

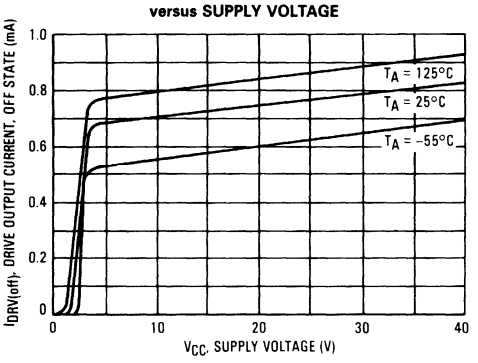


FIGURE 5 — INPUT BIAS CURRENT versus SENSE VOLTAGE

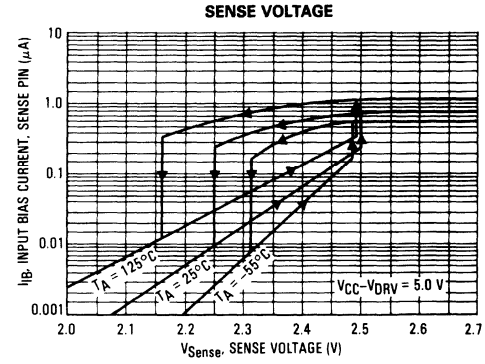


FIGURE 6 — DELAY CAPACITANCE versus DELAY TIME

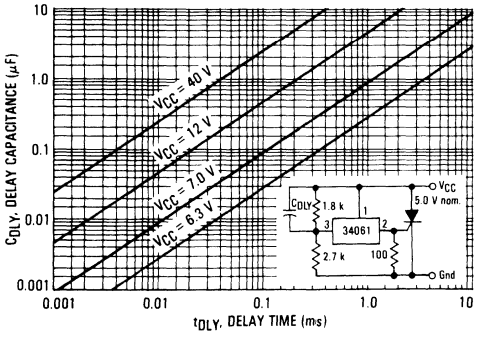
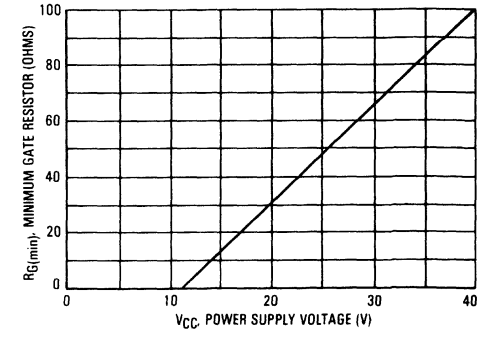
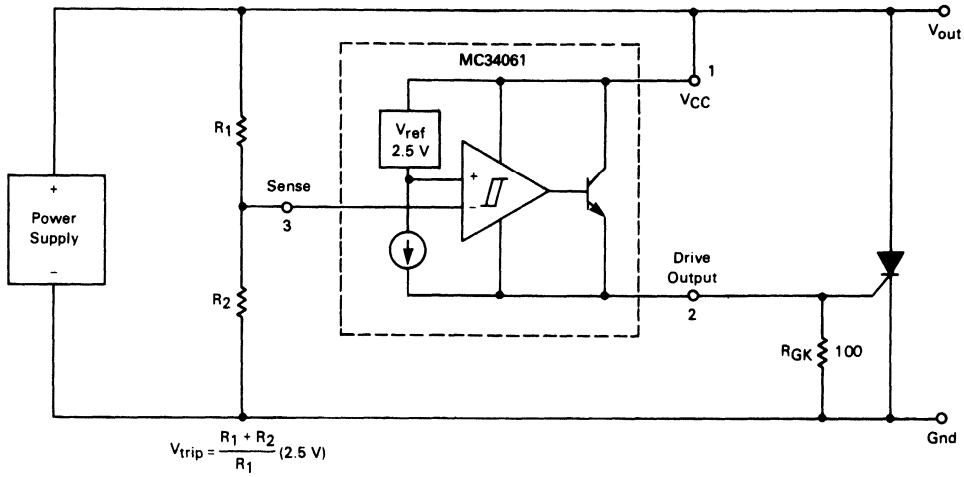


FIGURE 7 — MINIMUM R_G versus SUPPLY VOLTAGE



APPLICATIONS INFORMATION

FIGURE 8 — BLOCK DIAGRAM AND TYPICAL APPLICATION



BASIC CIRCUIT CONFIGURATION

The MC34061, consists of a 2.5 V shunt reference, a comparator with 250 mV hysteresis and a power output transistor. In the typical application of Figure 8, the voltage at the inverting input of the comparator is $\frac{V_{CC}\ R_2}{R_1 + R_2}$, while the voltage at the non-inverting input is $V_{CC} - 2.5$ V. Thus, given (R_1, R_2) voltage divider, the comparator's output state is a function of V_{CC}. The following table applies:

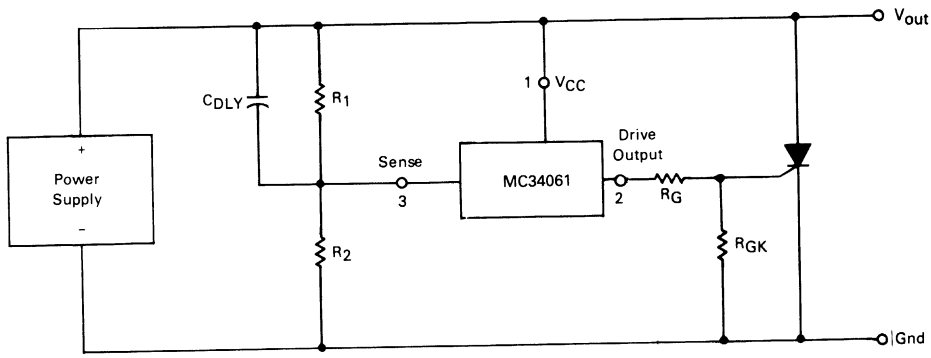
V_{CC}	Drive Output
$< \frac{R_1 + R_2}{R_1}$ (2.5 V)	OFF State
$> \frac{R_1 + R_2}{R_1}$ (2.5 V)	ON State

By making the proper choice of R_1 and R_2, a level detector for any voltage within the device's operating voltage range may be realized. A few precautions are necessary, however.

Note that even in the OFF State, a minimum drive output current, equal to the sum of the reference and comparator supply currents, is available. Therefore, a means of shunting this current away from the driven circuit is necessary. In the example of Figure 8, a 100 Ω resistor (R_{GK}) is used, producing a voltage at the Drive Output of approximately 60 mV in the OFF State.

In the ON State the MC34061 becomes a current source capable of saturating to within 2.0 V of V_{CC}. Therefore, when driving a high impedance load, it may be desirable to clamp the drive output to at least 3.0 V below V_{CC} ($V_{CC} - V_{DRV} \geq 3.0$ V) if it is important that the voltage reference continue to regulate.

FIGURE 9 — OVERVOLTAGE PROTECTION WITH TIME DELAY



PROGRAMMING A MINIMUM OVERVOLTAGE DURATION BEFORE TRIPPING

A time delay may be programmed into the operation of the MC34061 to provide noise immunity. This time delay is implemented by adding a capacitor (C_{DLY}) between the V_{CC} and Sense leads as shown in Figure 9. The time delay obtained by this technique is a function of R_1, R_2 and C_{DLY} as well as the nominal supply voltage, $V_{CC(nom)}$, and the overvoltage supply voltage, V_{CC}. The nominal supply voltage determines the initial charge on C_{DLY}, while the magnitude of the overvoltage condition determines the rate at which C_{DLY} charges to the reference voltage, V_{ref} = 2.5 V. Thus, for a given R_1, R_2 and C_{DLY}, the time delay is reduced as the overvoltage is increased. The expression for the time delay, T_{DLY}, is:

$$t_{DLY} = \frac{R_1 R_2 C_{DLY}}{R_1 + R_2} \ln \left[\frac{V_{CC} - V_{CC(nom)}}{V_{CC} - V_{trip}} \right]$$

where:

$$V_{trip} = \frac{R_1 + R_2}{R_1} (2.5\ V)$$

Figure 6 shows the C_{DLY} values versus delay time (t_{DLY}) for a typical 5.0 V power supply protection circuit. The figure also shows the change in t_{DLY} with variations in the overvoltage supply, V_{CC}. In this example R_1 = 1.8 k, R_2 = 2.7 k, $V_{CC(nom)}$ = 5.0 V, and V_{trip} = 6.25 V.

THE NEED FOR A GATE RESISTOR

For power supplies above 11 V, a gate resistor, R_G, in series with the SCR gate is recommended to limit the power dissipated by the IC to approximately 2.0 W. This resistor will protect the MC34061 in the event of a defective or missing SCR, while allowing the maximum drive output current to the gate of the SCR. Figure 7 shows the minimum recommended gate resistor, $R_{G(min)}$, versus the power supply voltage, V_{CC}. A larger value of R_G may be used if less drive current is needed.

CROWBAR SCR CONSIDERATIONS

Referring to Figure 10, it can be seen that the crowbar SCR, when activated, is subject to a large current surge from the output capacitance, C_{out}. This capacitance consists of the power supply output capacitors, the load's decoupling capacitors, and in the case of Figure 10A, the supply's input filter capacitors. This surge current is illustrated in Figure 11, and can cause SCR failure or degradation by any one of three mechanisms: di/dt, absolute peak surge, or I^2t. The interrelationship of these failure methods and the breadth of the applications make specification of the SCR by the semiconductor manufacturer difficult and expensive. Therefore, the designer must empirically determine the SCR and circuit elements which result in reliable and effective OVP operation. However, an understanding of the factors which influence the SCR's di/dt and surge capabilities simplifies this task.

1. di/dt

As the gate region of the SCR is driven on, its area of conduction takes a finite amount of time to grow, starting as a very small region and gradually spreading. Since the anode current flows through this turned-on gate region, very high current densities can occur in the gate region if high anode currents appear quickly (di/dt). This can result in immediate destruction of the SCR or gradual degradation of its forward blocking voltage capabilities — depending on the severity of the occasion.

The value of di/dt that an SCR can safely handle is influenced by its construction and the characteristics of the gate drive signal. A center-gate-fire SCR has more di/dt capability than a corner-gate-fire type, and heavily overdriving (3 to 5 times I_{GT}) the SCR gate with a fast $<1.0\ \mu s$ rise time signal will maximize its di/dt capability. A typical maximum number in phase control SCRs of less than 50 A(RMS) rating might be 200 $A/\mu s$, assuming a gate current of five times I_{GT} and $< 1.0\ \mu s$ rise time. If having done this, a di/dt problem is seen to still exist, the designer can also decrease the di/dt of the current waveform by adding inductance in series with the SCR, as shown in Figure 12. Of course, this reduces the circuit's ability to rapidly reduce the dc bus voltage and a tradeoff must be made between speedy voltage reduction and di/dt.

FIGURE 10 — TYPICAL CROWBAR CIRCUIT CONFIGURATIONS

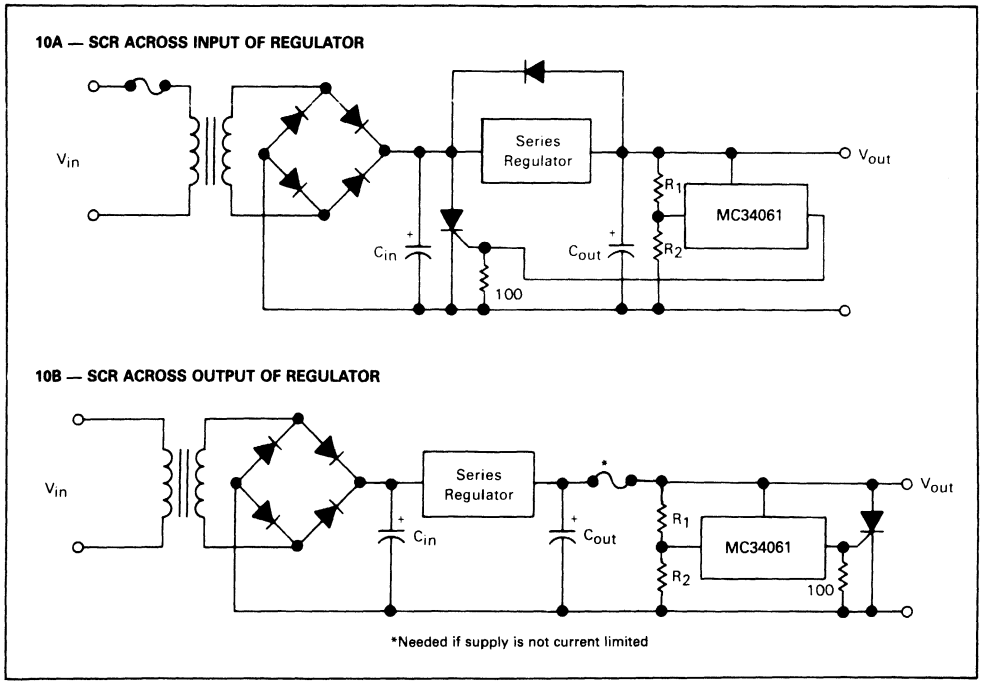
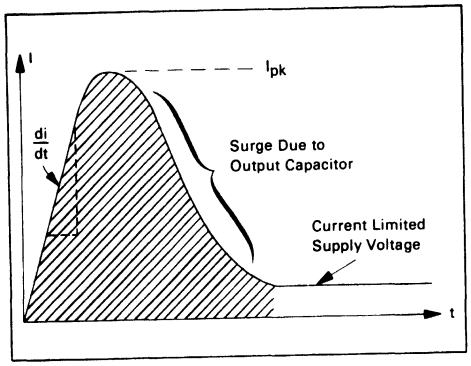


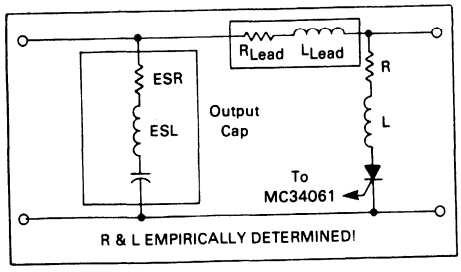
FIGURE 11 — CROWBAR SCR SURGE CURRENT WAVEFORM



2. Surge Current

If the peak current and/or the duration of the surge is excessive, immediate destruction due to device overheating will result. The surge capability of the SCR is directly proportional to its die area. If the surge current cannot be reduced (by adding series resistance — see Figure 12) to a safe level which is consistent with the system's requirements for speedy bus voltage reduction, the designer must use a higher current SCR. This may result in the average current capability of the SCR exceeding the steady state current requirements imposed by the dc power supply.

FIGURE 12 — CIRCUIT ELEMENTS AFFECTING SCR SURGE AND di/dt



A WORD ABOUT FUSING

Before leaving the subject of the crowbar SCR, a few words about fuse protection are in order. Referring back to Figure 10A, it will be seen that a fuse is necessary if the power supply to be protected is not output current limited. This fuse is not meant to prevent SCR failure but rather to prevent a fire!

In order to protect the SCR, the fuse would have to possess an I^2t rating less than that of the SCR and yet have a high enough continuous current rating to survive normal supply output currents. In addition, it must be capable of successfully clearing the high short circuit currents from the supply. Such a fuse as this is quite expensive, and may not even be available.

The usual design compromise then is to use a garden variety fuse (3AG or 3AB style) which cannot be relied on to blow before the thyristor does, and trust that if the SCR does fail, it will fail short circuit. In the majority of the designs, this will be the case, though this is difficult to guarantee. Of course, a sufficiently high surge will cause an open. These comments also apply to the fuse in Figure 10B.

CROWBAR SCR SELECTION GUIDE

As an aid in selecting an SCR for crowbar use, the following selection guide is presented.

DEVICE	I_{RMS}	I_{FSM}	PACKAGE
MCR67 Series	12 A	100 A	Metal Stud
MCR68 Series	12 A	100 A	TO-220 Plastic
2N1842 Series	16 A	125 A	Metal Stud
2N6400 Series	16 A	160 A	TO-220 Plastic
2N6504 Series	25 A	160 A	TO-220 Plastic
2N681 Series	25 A	200 A	Metal Stud
2N2573 Series	25 A	260 A	TO-204AA Metal Can
MCR69 Series	25 A	300 A	TO-220 Plastic
MCR70 Series	35 A	350 A	Metal Stud
MCR71 Series	55 A	550 A	Metal Stud

For a complete and detailed treatment of SCR and fuse selection refer to Motorola Application Note AN-789.

MOTOROLA

MC34063
MC35063
MC33063

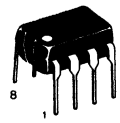
DC-TO-DC CONVERTER CONTROL CIRCUITS

The MC34063 Series is a monolithic control circuit containing the primary functions required for dc-to-dc converters. The device consists of an internal temperature compensated reference, comparator, controlled duty cycle oscillator with an active current limit circuit, driver and high current output switch. This series was specifically designed to be incorporated in Step-Down and Step-Up and Voltage-Inverting applications with a minimum number of external components.

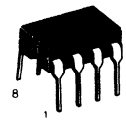
- Operation from 2.5 V to 40 V Input
- Low Standby Current
- Current Limiting
- Output Switch Current of 1.5 A
- Output Voltage Adjustable from 1.25 to 40 V
- Frequency of Operation to 100 kHz

DC-TO-DC CONVERTER CONTROL CIRCUITS

SILICON MONOLITHIC INTEGRATED CIRCUITS

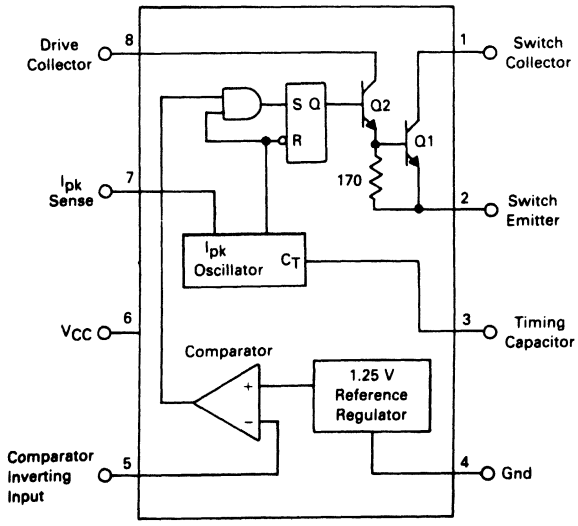


P1 SUFFIX
PLASTIC PACKAGE
CASE 626-05

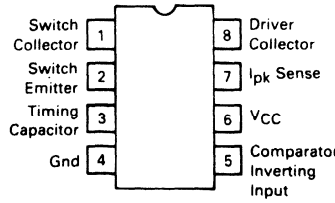


U SUFFIX
CERAMIC PACKAGE
CASE 693-02

FUNCTIONAL BLOCK DIAGRAM



PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

Device	Temperature Range	Package
MC35063U	−55 to +125°C	Ceramic DIP
MC33063U	−40 to +85°C	Ceramic DIP
MC33063P1		Plastic DIP
MC34063U	0 to +70°C	Ceramic DIP
MC34063P1		Plastic DIP

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	40	Vdc
Comparator Input Voltage Range	V_{IR}	−0.3 to +40	Vdc
Switch Collector Voltage	$V_{C(switch)}$	40	Vdc
Switch Emitter Voltage	$V_{E(switch)}$	40	Vdc
Switch Collector to Emitter Voltage	$V_{CE(switch)}$	40	Vdc
Driver Collector Voltage	$V_{C(driver)}$	40	Vdc
Switch Current	I_{SW}	1.5	Amps
Power Dissipation and Thermal Characteristics Ceramic Package T_A = +25°C Derate above T_A = +25°C Plastic Package T_A = +25°C Derate above T_A = +25°C	 P_D $1/\theta JA$ P_D $1/\theta JA$	 1.25 10 1.0 10	 W mW/°C W mW/°C
Operating Junction Temperature Ceramic Package Plastic Package	T_J	 +150 +125	°C
Operating Ambient Temperature Range MC35063 MC33063 MC34063	T_A	 −55 to +125 −40 to +85 0 to +70	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0 V; T_A = T_{low} to T_{high} [Note 1] unless otherwise specified.)

Characteristic	Symbol	Min	Typ	Max	Unit
OSCILLATOR					
Charging Current (5.0 V ≤ V_{CC} ≤ 40 V, T_A = 25°C)	I_{chg}	20	35	50	μA
Discharge current (5.0 V ≤ V_{CC} ≤ 40 V; T_A = 25°C)	I_{dischg}	150	200	250	μA
Voltage Swing (T_A = 25°C)	V_{osc}	—	0.5	—	V_{p-p}
Discharge to Charge Current Ratio ($I_{pk(sense)}$ = V_{CC}, T_A = 25°C)	I_{dischg}/I_{chg}	—	6.0	—	—
Current Limit Sense Voltage I_{chg} = I_{dischg}, T_A = 25°C	$V_{Ipk(sense)}$	250	300	350	mV
OUTPUT SWITCH (Note 2)					
Saturation Voltage, Darlington Connection I_{SW} = 1.0 A; $V_{C(driver)}$ = $V_{C(switch)}$	$V_{CE(sat)}$	—	1.0	1.3	V
Saturation Voltage I_{SW} = 1.0 A; $I_{C(driver)}$ = 50 mA, (Forced B ≈ 20)	$V_{CE(sat)}$	—	0.45	0.7	V
DC Current Gain I_{SW} = 1.0 A; V_{CE} = 5.0 V; T_A = 25°C	h_{FE}	35	120	—	—
Collector Off-State Current (V_{CE} = 40 V; T_A = 25°C)	$I_{C(off)}$	—	10	—	nA
COMPARATOR					
Threshold Voltage	V_{th}	1.18	1.25	1.32	V
Threshold Voltage Line Regulation (3.0 V ≤ V_{CC} ≤ 40 V)	Reg_{line}	—	0.04	0.2	mV/V
Input Bias Current (V_{in} = 0 V)	I_{IB}	—	40	400	nA
TOTAL DEVICE					
Supply Current 5.0 V ≤ V_{CC} ≤ 40 V, C_T = 0.001 μF $I_{pk(sense)}$ = V_{CC}, V pin 5 > V_{th}, Pin 2 = Gnd, Remaining pins open	I_{CC}	—	2.4	3.5	mA

NOTES:

1. T_{low} = −55°C for MC35063, −40°C for MC33063, 0°C for MC34063; T_{high} = +125°C for MC35063, +85°C for MC33063, +70°C for MC34063
2. Output switch tests are performed under pulsed conditions to minimize power dissipation.

FIGURE 1 — OUTPUT SWITCH ON-OFF TIME versus OSCILLATOR TIMING CAPACITOR

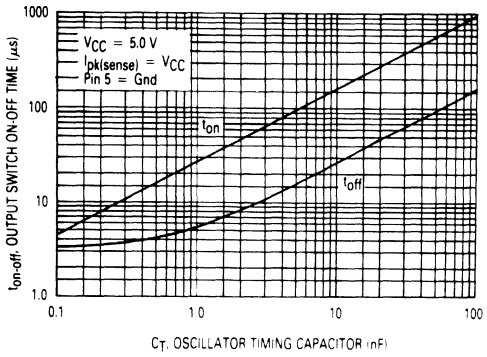


FIGURE 2 — STANDBY SUPPLY CURRENT versus SUPPLY VOLTAGE

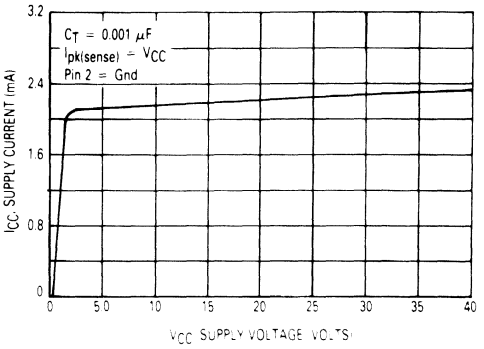


FIGURE 3 — EMITTER-FOLLOWER CONFIGURATION OUTPUT SWITCH SATURATION VOLTAGE versus EMITTER CURRENT

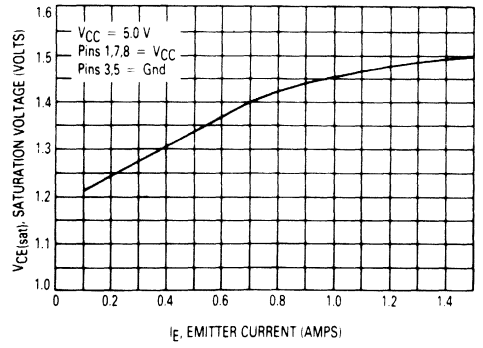


FIGURE 4 — COMMON-EMITTER CONFIGURATION OUTPUT SWITCH SATURATION VOLTAGE versus COLLECTOR CURRENT

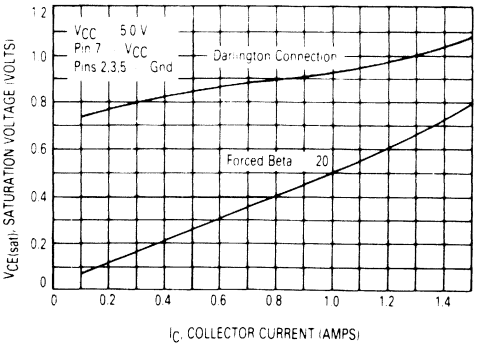
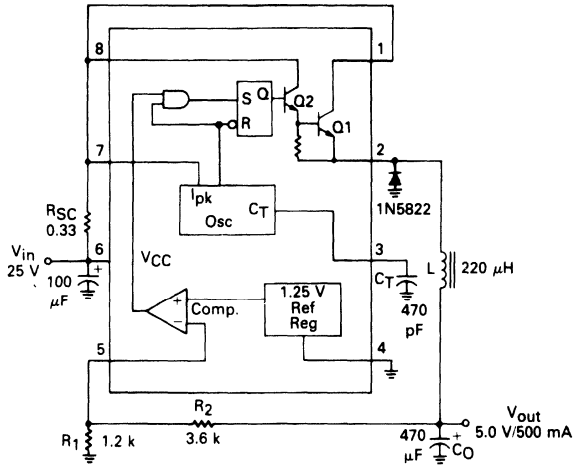


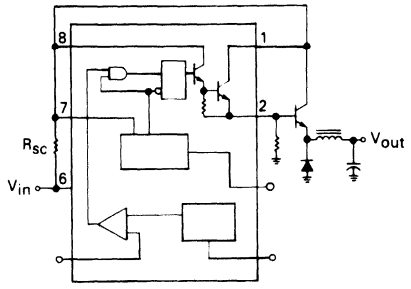
FIGURE 5 — STEP-DOWN CONVERTER



Test	Conditions	Results
Line Regulation	V_{in} = 15 to 25 V, I_O = 500 mA	15 mV
Load Regulation	V_{in} = 25 V, I_O = 50 to 500 mA	5.0 mV
Output Ripple	V_{in} = 25 V, I_O = 500 mA	40 mV_{p-p}
Short Circuit Current	V_{in} = 25 V, R_L = 0.1 Ω	2.3 A
Efficiency	V_{in} = 25 V, I_O = 500 mA	84.7%

FIGURE 6 — EXTERNAL CURRENT BOOST CONNECTIONS FOR I_C PEAK GREATER THAN 1.5 A

6A — EXTERNAL NPN SWITCH



6B — EXTERNAL PNP SATURATED SWITCH

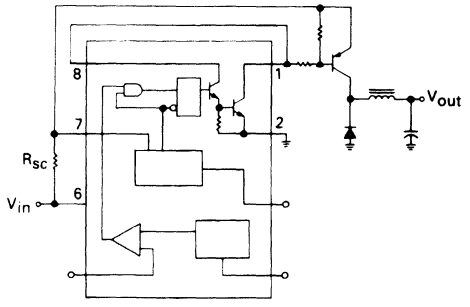
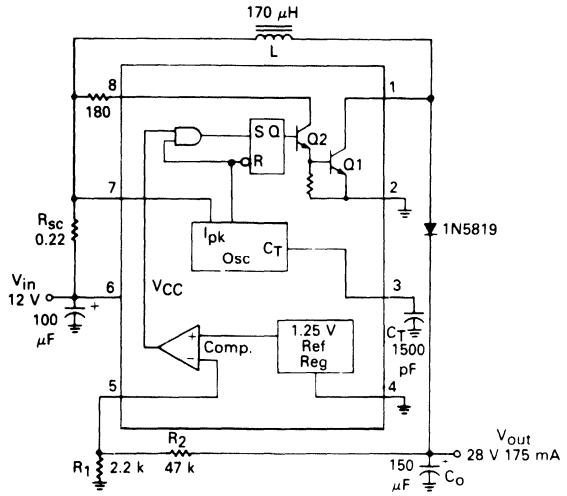


FIGURE 7 — STEP-UP CONVERTER



Test	Conditions	Results
Line Regulation	V_{in} = 8.0 to 16 V, I_O = 175 mA	12 mV
Load Regulation	V_{in} = 12 V, I_O = 75 to 175 mA	45 mV
Output Ripple	V_{in} = 12 V, I_O = 175 mA	150 mV_{p-p}
Short Circuit Current	V_{in} = 12 V, R_L = 0.1 Ω	2.0 A
Efficiency	V_{in} = 12 V, I_O = 175 mA	93%

FIGURE 8 — EXTERNAL CURRENT BOOST CONNECTIONS FOR I_C PEAK GREATER THAN 1.5 A

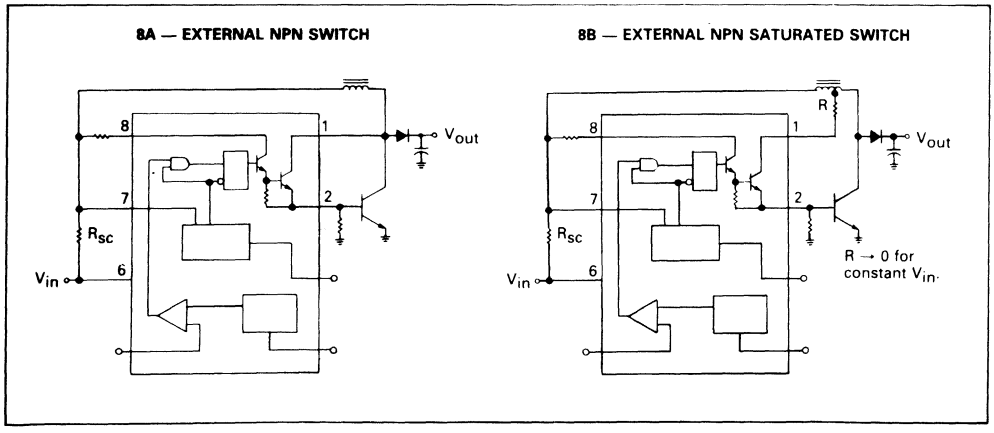


FIGURE 9 — DESIGN FORMULA TABLE

Calculation	Step-Down	Step-Up
$\frac{t_{on}}{t_{off}}$	$\frac{V_{out} + V_F}{V_{in(min)} - V_{sat} - V_{out}}$	$\frac{V_{out} + V_F - V_{in(min)}}{V_{in(min)} - V_{sat}}$
$(t_{on} + t_{off})_{max}$	$\frac{1}{f_{min}}$	$\frac{1}{f_{min}}$
C_T	$4 \times 10^{-5} t_{on}$	$4 \times 10^{-5} t_{on}$
$I_{pk(switch)}$	$2I_{out(max)}$	$2I_{out(max)} \left(\frac{t_{on} + t_{off}}{t_{off}}\right)$
R_{SC}	$0.33/I_{pk(switch)}$	$0.33/I_{pk(switch)}$
$L_{(min)}$	$\left(\frac{V_{in(min)} - V_{sat} - V_{out}}{I_{pk(switch)}}\right) t_{on(max)}$	$\left(\frac{V_{in(min)} - V_{sat}}{I_{pk(switch)}}\right) t_{on(max)}$
C_o	$\frac{I_{pk(switch)} (t_{on} + t_{off})}{8 V_{ripple(p-p)}}$	$\approx \frac{I_{out} t_{on}}{V_{ripple}}$

V_{sat} = Saturation voltage of the output switch.
V_F = Forward voltage drop of the ringback rectifier

The following power supply characteristics must be chosen:

V_{in} — Nominal input voltage. If this voltage is not constant, then use $V_{in(max)}$ for step-down and $V_{in(min)}$ for step-up converter.

V_{out} — Desired output voltage, $V_{out} = 1.25 \left(1 + \frac{R_2}{R_1}\right)$.

I_{out} — Desired output current.

f_{min} — Minimum desired output switching frequency at the selected values for V_{in} and I_o.

$V_{ripple(p-p)}$ — Desired peak-to-peak output ripple voltage. In practice, the calculated value will need to be increased due to the capacitor's equivalent series resistance and board layout. The ripple voltage should be kept to a low value since it will directly effect the line and load regulation.

Note:
For further information refer to application note AN920R2.

MC34063A
MC35063A
MC33063A

Advance Information

DC-TO-DC CONVERTER CONTROL CIRCUITS

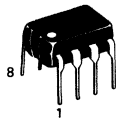
The MC34063A Series is a monolithic control circuit containing the primary functions required for DC-to-DC converters. These devices consist of an internal temperature compensated reference, comparator, controlled duty cycle oscillator with an active current limit circuit, driver and high current output switch. This series was specifically designed to be incorporated in Step-Down and Step-Up and Voltage-Inverting applications with a minimum number of external components. Refer to Application Notes AN920A and AN954 for additional design information.

- Operation from 3.0 V to 40 V Input
- Low Standby Current
- Current Limiting
- Output Switch Current to 1.5 A
- Output Voltage Adjustable
- Frequency Operation to 100 kHz
- Precision 2% Reference

DC-TO-DC CONVERTER CONTROL CIRCUITS

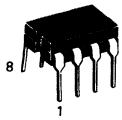
SILICON MONOLITHIC INTEGRATED CIRCUITS

P1 SUFFIX
PLASTIC PACKAGE
CASE 626-05

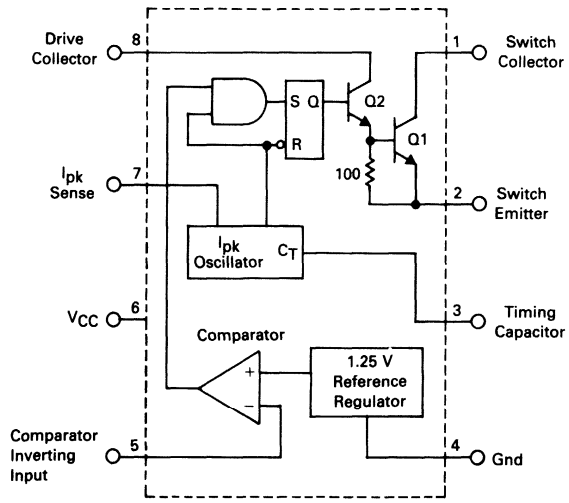


D SUFFIX
PLASTIC PACKAGE
CASE 751-03
SO-8

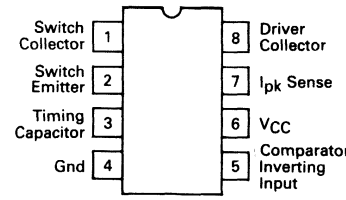
U SUFFIX
CERAMIC PACKAGE
CASE 693-02



FUNCTIONAL BLOCK DIAGRAM



PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

Device	Temperature Range	Package
MC35063AU	−55 to +125°C	Ceramic DIP
MC33063AD	−40 to +85°C	Plastic SOIC
MC33063AP1		Plastic DIP
MC34063AD	0 to +70°C	Plastic SOIC
MC34063AP1		Plastic DIP

This document contains information on a new product. Specifications and information herein are subject to change without notice.

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	40	Vdc
Comparator Input Voltage Range	V_{IR}	−0.3 to +40	Vdc
Switch Collector Voltage	$V_{C(switch)}$	40	Vdc
Switch Emitter Voltage ($V_{Pin\ 1}$ = 40 V)	$V_{E(switch)}$	40	Vdc
Switch Collector to Emitter Voltage	$V_{CE(switch)}$	40	Vdc
Driver Collector Voltage	$V_{C(driver)}$	40	Vdc
Driver Collector Current (Note 1)	$I_{C(driver)}$	100	mA
Switch Current	I_{SW}	1.5	Amps
Power Dissipation and Thermal Characteristics			
Ceramic Package, U Suffix			
T_A = +25°C	P_D	1.25	W
Thermal Resistance	$R_{\theta JA}$	100	°C/W
Plastic Package, P Suffix			
T_A = +25°C	P_D	1.25	W
Thermal Resistance	$R_{\theta JA}$	100	°C/W
SOIC Package, D Suffix			
T_A = +25°C	P_D	625	mW
Thermal Resistance	$R_{\theta JA}$	160	°C/W
Operating Junction Temperature	T_J	+150	°C
Operating Ambient Temperature Range	T_A		°C
MC35063A		−55 to +125	
MC33063A		−40 to +85	
MC34063A		0 to +70	
Storage Temperature Range	T_{stg}	−65 to +150	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0 V; T_A = T_{low} to T_{high} [Note 2] unless otherwise specified)

Characteristic	Symbol	Min	Typ	Max	Units
OSCILLATOR					
Frequency ($V_{Pin\ 5}$ = 0 V, C_T = 1.0 nF, T_A = 25°C)	f_{OSC}	24	33	42	kHz
Charge Current (V_{CC} = 5.0 V to 40 V, T_A = 25°C)	I_{chg}	24	33	42	μA
Discharge Current (V_{CC} = 5.0 V to 40 V, T_A = 25°C)	I_{dischg}	140	200	260	μA
Discharge to Charge Current Ratio (Pin 7 = V_{CC}, T_A = 25°C)	I_{dischg}/I_{chg}	5.2	6.2	7.5	—
Current Limit Sense Voltage (I_{chg} = I_{dischg}, T_A = 25°C)	$V_{ipk(sense)}$	250	300	350	mV

NOTES:
1. Maximum package power dissipation limits must be observed.
2. T_{low} = −55°C for MC35063A, −40°C for MC33063A, 0°C for MC34063A; T_{high} = +125°C for MC35063A, +85°C for MC33063A, +70°C for MC34063A

ELECTRICAL CHARACTERISTICS — continued (V_{CC} = 5.0 V; T_A = T_{low} to T_{high} unless otherwise specified)

Characteristic	Symbol	Min	Typ	Max	Units
OUTPUT SWITCH (Note 3)					
Saturation Voltage, Darlington Connection (I_{SW} = 1.0 A, Pins 1, 8 connected)	$V_{CE(sat)}$	—	1.0	1.3	V
Saturation Voltage (I_{SW} = 1.0 A, $R_{Pin\ 8}$ = 82 Ω to V_{CC}, Forced $\beta \approx 20$)	$V_{CE(sat)}$	—	0.45	0.7	V
DC Current Gain (I_{SW} = 1.0 A, V_{CE} = 5.0 V, T_A = 25°C)	h_{FE}	50	120	—	—
Collector Off-State Current (V_{CE} = 40 V)	$I_{C(off)}$	—	0.01	100	μA
COMPARATOR					
Threshold Voltage (T_A = 25°C) (T_A = T_{low} to T_{high})	V_{th}	 1.225 1.21	1.25 —	 1.275 1.29	V
Threshold Voltage Line Regulation (V_{CC} = 3.0 V to 40 V)	Reg_{line}	—	1.4	5.0	mV
Input Bias Current (V_{in} = 0 V)	I_{IB}	—	−40	−400	nA
TOTAL DEVICE					
Supply Current (V_{CC} = 5.0 V to 40 V, C_T = 1.0 nF, Pin 7 = V_{CC}, $V_{Pin\ 5}$ > V_{th}, Pin 2 = Gnd, Remaining pins open)	I_{CC}	—	2.5	4.0	mA
TOTAL DEVICE					
Supply Current (V_{CC} = 5.0 V to 40 V, C_T = 1.0 nF, Pin 7 = V_{CC}, $V_{Pin\ 5}$ > V_{th}, Pin 2 = Gnd, Remaining pins open)	I_{CC}	—	2.5	4.0	mA

NOTES:

3. Low duty cycle pulse techniques are used during test to maintain junction temperature as close to ambient temperature as possible.
4. If the output switch is driven into hard saturation (non-Darlington configuration) at low switch currents (≤300 mA) and high driver currents (≥30 mA), it may take up to (2.0 μs) to come out of saturation. This condition will shorten the "off" time at frequencies ≥ 30 kHz, and is magnified at high temperatures. This condition does not occur with a Darlington configuration, since the output switch cannot saturate. If a non-Darlington configuration is used, the following output drive condition is recommended:

Forced β of output switch = I_C, output/(I_C, driver − 7.0 mA*) ≥ 10

*The 100 Ω resistor in the emitter of the driver device requires about 7.0 mA before the output switch conducts.

FIGURE 1 — OUTPUT SWITCH ON-OFF TIME versus OSCILLATOR TIMING CAPACITOR

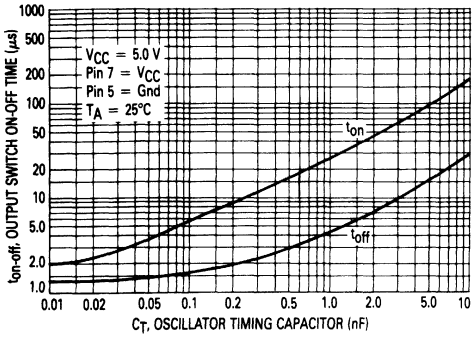


FIGURE 2 — TIMING CAPACITOR WAVEFORM

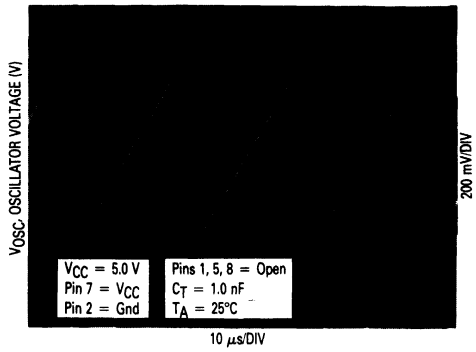


FIGURE 3 — EMITTER FOLLOWER CONFIGURATION OUTPUT SATURATION VOLTAGE versus EMITTER CURRENT

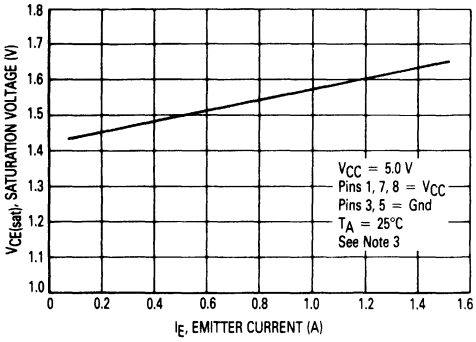


FIGURE 4 — COMMON EMITTER CONFIGURATION OUTPUT SWITCH SATURATION VOLTAGE versus COLLECTOR CURRENT

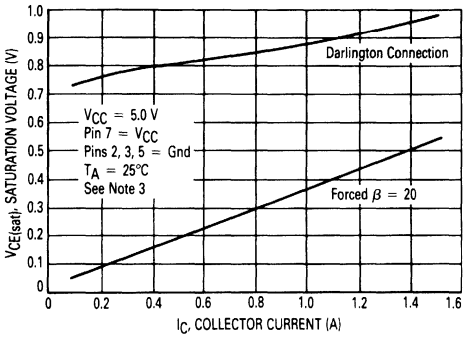


FIGURE 5 — CURRENT LIMIT SENSE VOLTAGE versus TEMPERATURE

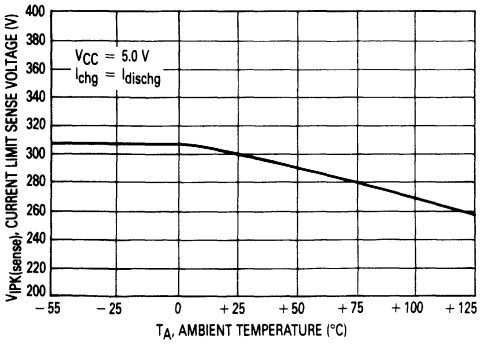


FIGURE 6 — STANDBY SUPPLY CURRENT versus SUPPLY VOLTAGE

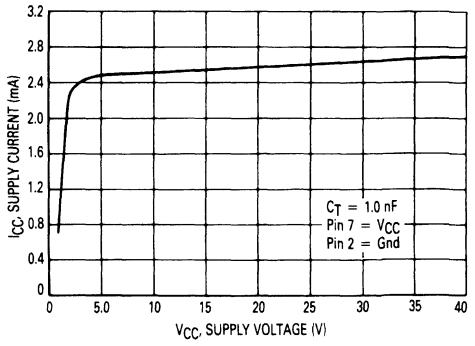
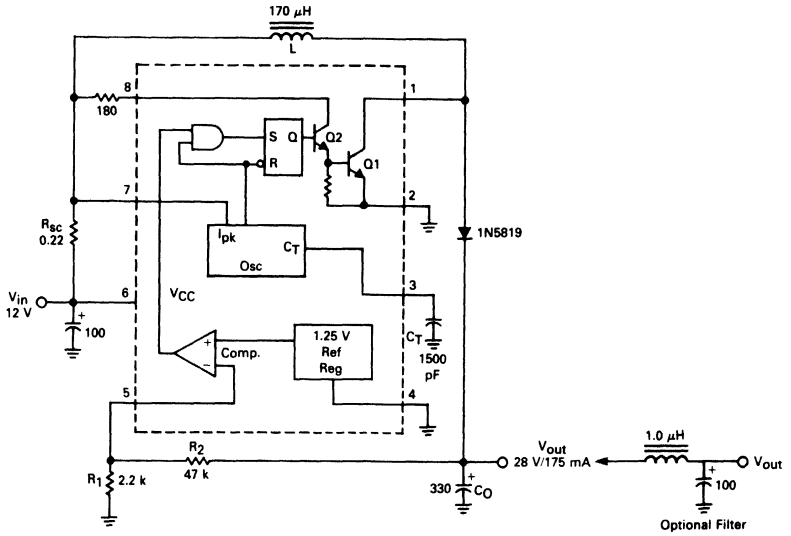


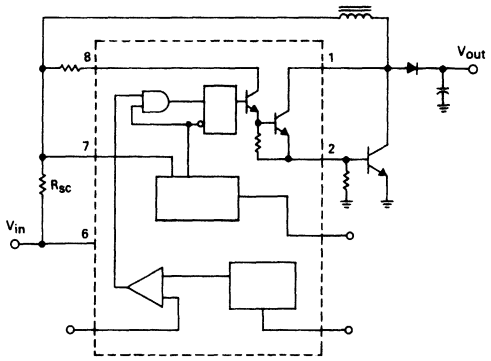
FIGURE 7 — STEP-UP CONVERTER



Test	Conditions	Results
Line Regulation	V_{in} = 8.0 V to 16 V, I_O = 175 mA	30 mV = ±0.05%
Load Regulation	V_{in} = 12 V, I_O = 75 to 175 mA	10 mV = ±0.017%
Output Ripple	V_{in} = 12 V, I_O = 175 mA	400 mVp-p
Efficiency	V_{in} = 12 V, I_O = 175 mA	89.2%
Output Ripple With Optional Filter	V_{in} = 12 V, I_O = 175 mA	40 mVp-p

FIGURE 8 — EXTERNAL CURRENT BOOST CONNECTIONS FOR I_C PEAK GREATER THAN 1.5 A

8A — EXTERNAL NPN SWITCH



8B — EXTERNAL NPN SATURATED SWITCH (REFER TO NOTE 4)

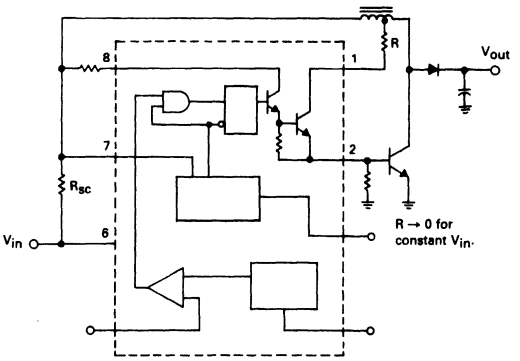
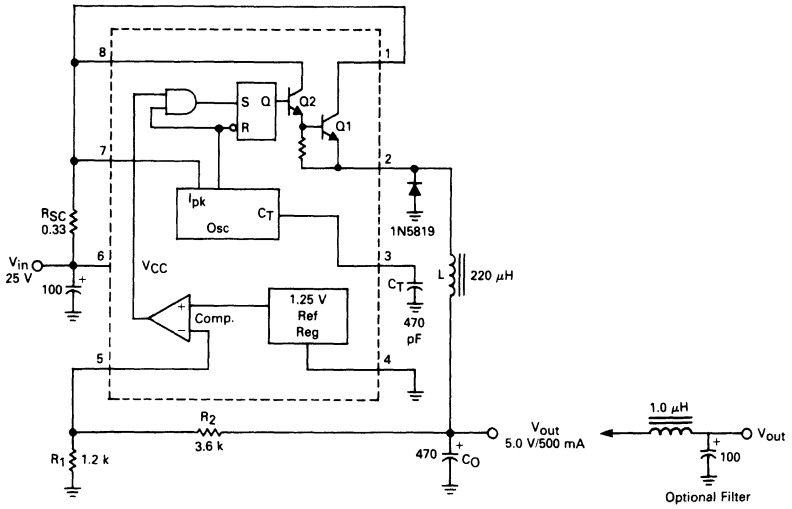


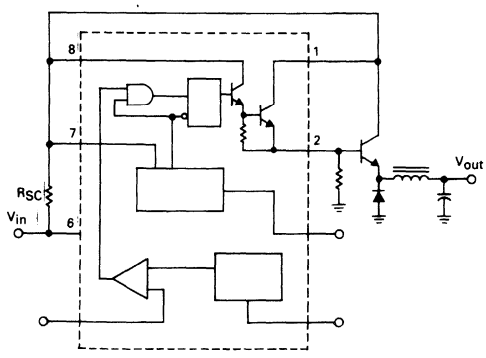
FIGURE 9 — STEP-DOWN CONVERTER



Test	Conditions	Results
Line Regulation	V_{in} = 15 V to 25 V, I_O = 500 mA	12 mV = ±0.12%
Load Regulation	V_{in} = 25 V, I_O = 50 to 500 mA	3.0 mV = ±0.03%
Output Ripple	V_{in} = 25 V, I_O = 500 mA	120 mVp-p
Short Circuit Current	V_{in} = 25 V, R_L = 0.1 Ω	1.1 A
Efficiency	V_{in} = 25 V, I_O = 500 mA	82.5%
Output Ripple With Optional Filter	V_{in} = 25 V, I_O = 500 mA	40 mVp-p

FIGURE 10 — EXTERNAL CURRENT BOOST CONNECTIONS FOR I_C PEAK GREATER THAN 1.5 A

10A — EXTERNAL NPN SWITCH



10B — EXTERNAL PNP SATURATED SWITCH

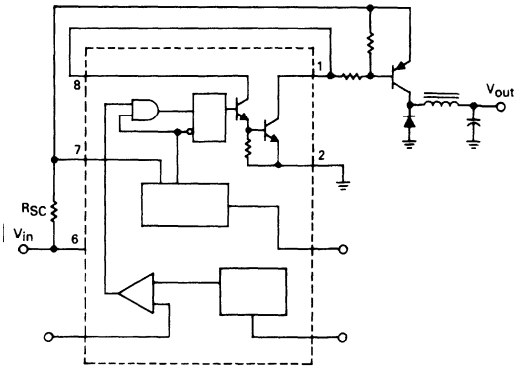
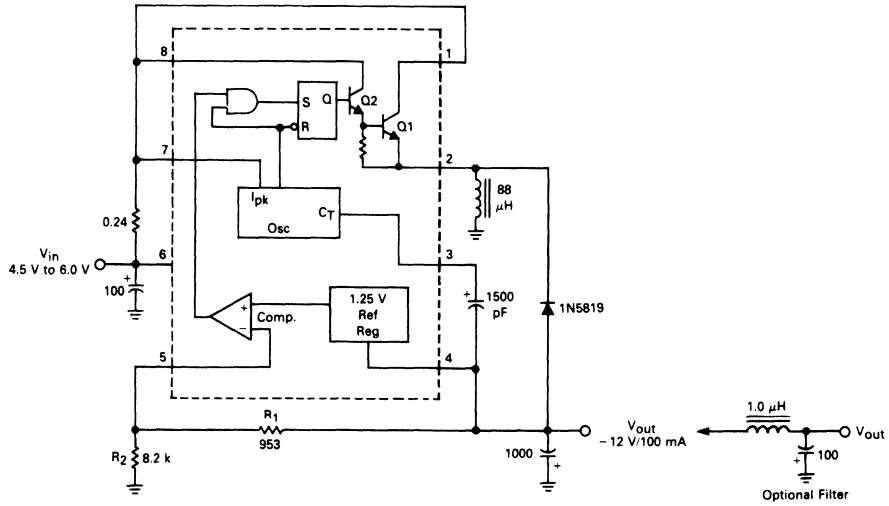


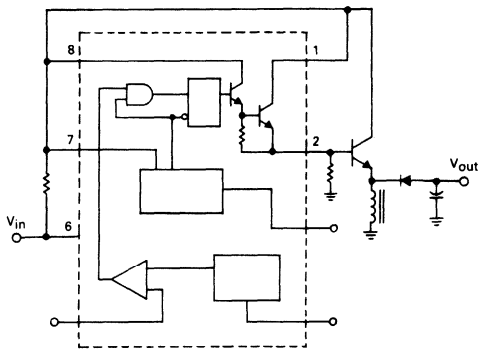
FIGURE 11 — VOLTAGE INVERTING CONVERTER



Test	Conditions	Results
Line Regulation	V_{in} = 4.5 V to 6.0 V, I_O = 100 mA	3.0 mV = ±0.012%
Load Regulation	V_{in} = 5.0 V, I_O = 10 to 100 mA	0.022 V = ±0.09%
Output Ripple	V_{in} = 5.0 V, I_O = 100 mA	500 mVp-p
Short Circuit Current	V_{in} = 5.0 V, R_L = 0.1 Ω	910 mA
Efficiency	V_{in} = 5.0 V, I_O = 100 mA	64.5%
Output Ripple With Optional Filter	V_{in} = 5.0 V, I_O = 100 mA	70 mVp-p

FIGURE 12 — EXTERNAL CURRENT BOOST CONNECTIONS FOR I_C PEAK GREATER THAN 1.5 A

12A — EXTERNAL NPN SWITCH



12B — EXTERNAL PNP SATURATED SWITCH

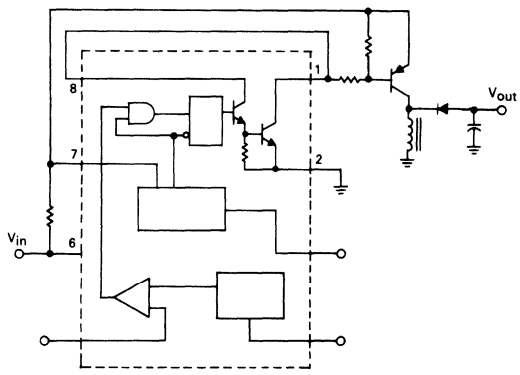
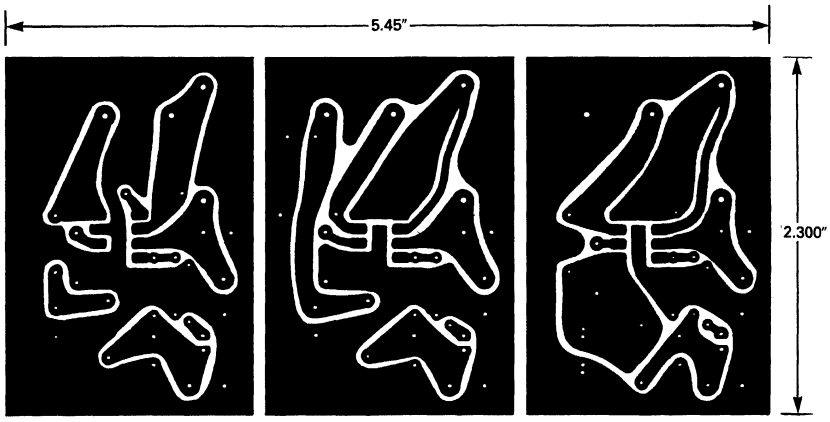
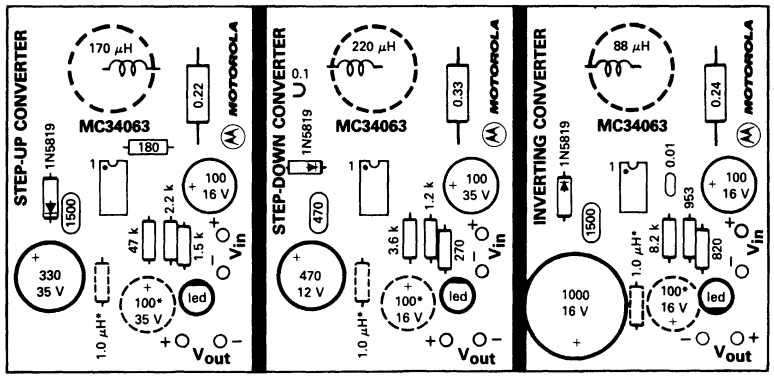


FIGURE 13 — PRINTED CIRCUIT BOARD AND COMPONENT LAYOUT
(CIRCUITS OF FIGURES 7, 9, 11)



(Top view, copper foil as seen through the board from the component side)



*Optional Filter.

Top View, Component Side

INDUCTOR DATA

Converter	Inductance (µH)	Turns/Wire
Step-Up	170	38 Turns of #22 AWG
Step-Down	220	48 Turns of #22 AWG
Voltage-Inverting	88	28 Turns of #22 AWG

All inductors are wound on Magnetics 55117 toroidal core.

FIGURE 14 — DESIGN FORMULA TABLE

Calculation	Step-Up	Step-Down	Voltage-Inverting
t_{on}/t_{off}	$\frac{V_{out}+V_F-V_{in(min)}}{V_{in(min)}-V_{sat}}$	$\frac{V_{out}+V_F}{V_{in(min)}-V_{sat}-V_{out}}$	$\frac{\lvert V_{out}\rvert+V_F}{V_{in}-V_{sat}}$
$(t_{on}+t_{off})$ max	$1/f_{min}$	$1/f_{min}$	$1/f_{min}$
C_T	$4 \times 10^{-5}\, t_{on}$	$4 \times 10^{-5}\, t_{on}$	$4 \times 10^{-5}\, t_{on}$
$I_{pk(switch)}$	$2I_{out(max)}(t_{on}/t_{off}+1)$	$2I_{out(max)}$	$2I_{out(max)}(t_{on}/t_{off}+1)$
R_{SC}	$0.3/I_{pk(switch)}$	$0.3/I_{pk(switch)}$	$0.3/I_{pk(switch)}$
$L_{(min)}$	$\frac{(V_{in(min)}-V_{sat})t_{on(max)}}{I_{pk(switch)}}$	$\frac{(V_{in(min)}-V_{sat}-V_{out})t_{on(max)}}{I_{pk(switch)}}$	$\frac{(V_{in(min)}-V_{sat})t_{on(max)}}{I_{pk(switch)}}$
C_O	$\simeq I_{out}t_{on}/V_{ripple(p-p)}$	$\frac{I_{pk(switch)}(t_{on}+t_{off})}{8\,V_{ripple(p-p)}}$	$\simeq I_{out}t_{on}/V_{ripple(p-p)}$

V_{sat} = Saturation voltage of the output switch.
V_F = Forward voltage drop of the output rectifier.

The following power supply characteristics must be chosen:

V_{in} — Nominal input voltage.

V_{out} — Desired output voltage, $|V_{out}| = 1.25\ (1 + R2/R1)$

I_{out} — Desired output current.

f_{min} — Minimum desired output switching frequency at the selected values of V_{in} and I_O.

$V_{ripple(p-p)}$ — Desired peak-to-peak output ripple voltage. In practice, the calculated capacitor value will need to be increased due to its equivalent series resistance and board layout. The ripple voltage should be kept to a low value since it will directly affect the line and load regulation.

MOTOROLA

MC34064
MC33064

Advance Information

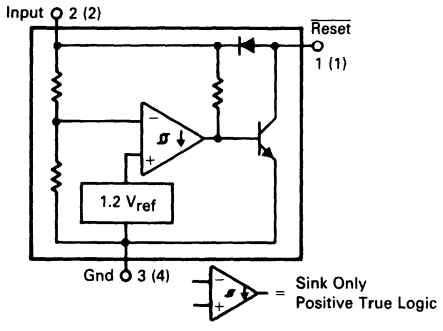
UNDERVOLTAGE SENSING CIRCUIT

The MC34064 is an undervoltage sensing circuit specifically designed for use as a reset controller in microprocessor-based systems. It offers the designer an economical solution for low voltage detection with a single external resistor. The MC34064 features a trimmed-in-package bandgap reference, and a comparator with precise thresholds and built-in hysteresis to prevent erratic reset operation. The open collector reset output is capable of sinking in excess of 10 mA, and operation is guaranteed down to 1.0 volt input with low standby current. These devices are packaged in 3-pin TO-226AA and 8-pin surface mount packages.

Applications include direct monitoring of the 5.0 volt MPU/logic power supply used in appliance, automotive, consumer and industrial equipment.

- Trimmed-In-Package Temperature Compensated Reference
- Comparator Threshold of 4.6 V at 25°C
- Precise Comparator Thresholds Guaranteed Over Temperature
- Comparator Hysteresis Prevents Erratic Reset
- Reset Output Capable of Sinking in Excess of 10 mA
- Internal Clamp Diode for Discharging Delay Capacitor
- Guaranteed Reset Operation with 1.0 Volt Input
- Low Standby Current
- Economical TO-226AA and SO-8 Surface Mount Packages

REPRESENTATIVE BLOCK DIAGRAM



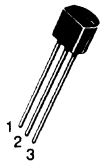
Pin numbers adjacent to terminals are for the 3-pin TO-226AA package.
Pin numbers in parenthesis are for the D suffix SO-8 package.

This document contains information on a new product. Specifications and information herein are subject to change without notice.

UNDERVOLTAGE SENSING CIRCUIT

SILICON MONOLITHIC INTEGRATED CIRCUIT

P SUFFIX
PLASTIC PACKAGE
CASE 29-04
TO-226AA



PIN 1. $\overline{\text{RESET}}$
2. INPUT
3. GROUND

D SUFFIX
PLASTIC PACKAGE
CASE 751-03
SO-8

PIN 1. $\overline{\text{RESET}}$
2. INPUT
3. N.C.
4. GROUND
5. N.C.
6. N.C.
7. N.C.
8. N.C.

ORDERING INFORMATION		
Device	**Temperature Range**	**Package**
MC34064D-5	0°C to +70°C	Plastic SO-8
MC34064P-5		Plastic TO-226AA
MC33064D-5	−40°C to +85°C	Plastic SO-8
MC33064P-5		Plastic TO-226AA

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Input Supply Voltage	V_{in}	−1.0 to 10	V
$\overline{\text{Reset}}$ Output Voltage	V_O	10	V
$\overline{\text{Reset}}$ Output Sink Current (Note 1)	I_{Sink}	Internally Limited	mA
Clamp Diode Forward Current, Pin 1 to 2 (Note 1)	I_F	100	mA
Power Dissipation and Thermal Characteristics			
P Suffix, Plastic Package			
Maximum Power Dissipation @ T_A = 25°C	P_D	625	mW
Thermal Resistance, Junction to Air	$R_{\theta JA}$	200	°C/W
D Suffix, Plastic Package			
Maximum Power Dissipation @ T_A = 25°C	P_D	625	mW
Thermal Resistance Junction to Air	$R_{\theta JA}$	200	°C/W
Operating Junction Temperature	T_J	+150	°C
Operating Ambient Temperature	T_A		°C
MC34064		0 to +70	
MC33064		−40 to +85	
Storage Temperature Range	T_{stg}	−65 to +150	°C

ELECTRICAL CHARACTERISTICS For typical values T_A = 25°C, for min/max values T_A is the operating ambient temperature range that applies [Notes 2 and 3].

Characteristic	Symbol	Min	Typ	Max	Unit
COMPARATOR					
Threshold Voltage					V
High State Output (V_{in} Increasing)	V_{IH}	4.5	4.61	4.7	
Low State Output (V_{in} Decreasing)	V_{IL}	4.5	4.59	4.7	
Hysteresis	V_H	0.01	0.02	0.05	
$\overline{\text{RESET}}$ OUTPUT					
Output Sink Saturation	V_{OL}				V
(V_{in} = 4.0 V, I_{Sink} = 8.0 mA)		—	0.46	1.0	
(V_{in} = 4.0 V, I_{Sink} = 2.0 mA)		—	0.15	0.4	
(V_{in} = 1.0 V, I_{Sink} = 0.1 mA)		—	—	0.1	
Output Sink Current (V_{in}, $\overline{\text{Reset}}$ = 4.0 V)	I_{Sink}	10	27	60	mA
Output Off-State Leakage (V_{in}, $\overline{\text{Reset}}$ = 5.0 V)	I_{OH}	—	0.02	0.5	μA
Clamp Diode Forward Voltage, Pin 1 to 2 (I_F = 10 mA)	V_F	0.6	0.9	1.2	V
TOTAL DEVICE					
Operating Input Voltage Range	V_{in}	1.0 to 6.5	—	—	V
Quiescent Input Current (V_{in} = 5.0 V)	I_{in}	—	390	500	μA

NOTES:
1. Maximum package power dissipation limits must be observed.
2. Low duty cycle pulse techniques are used during test to maintain junction temperature as close to ambient as possible.
3. T_{low} = 0°C for MC34064 = −40°C for MC33064; T_{high} = +70°C for MC34064 = +85°C for MC33064

FIGURE 1 — $\overline{\text{RESET}}$ OUTPUT VOLTAGE versus INPUT VOLTAGE

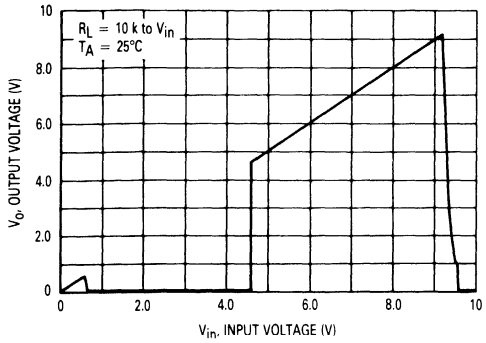


FIGURE 2 — $\overline{\text{RESET}}$ OUTPUT VOLTAGE versus INPUT VOLTAGE

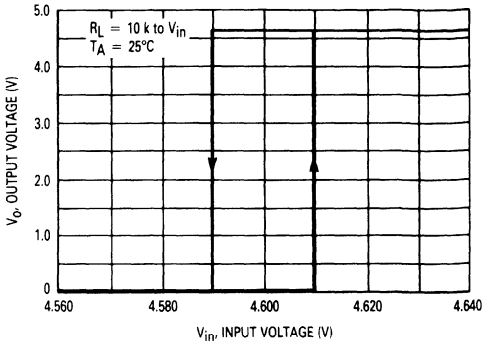


FIGURE 3 — COMPARATOR THRESHOLD VOLTAGE versus TEMPERATURE

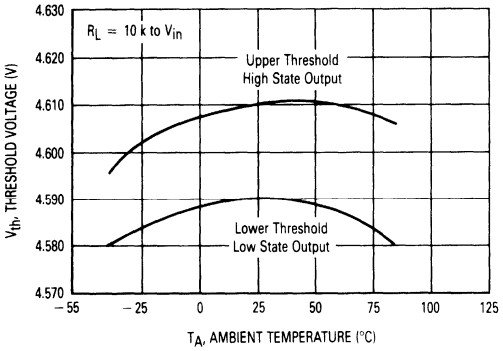


FIGURE 4 — INPUT CURRENT versus INPUT VOLTAGE

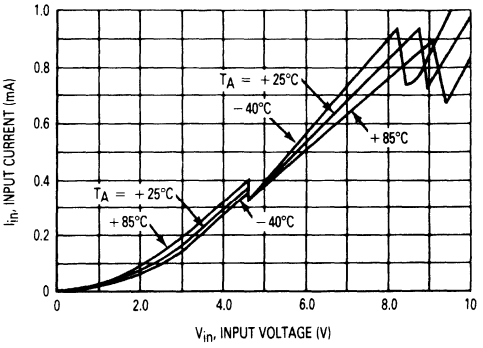


FIGURE 5 — $\overline{\text{RESET}}$ OUTPUT SATURATION versus SINK CURRENT

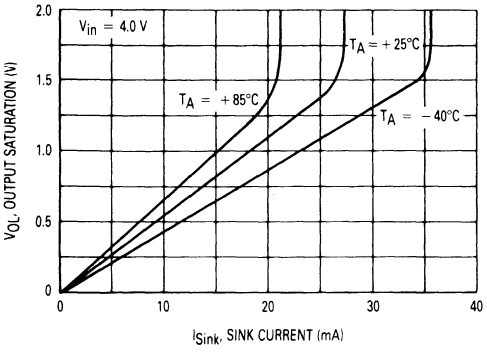


FIGURE 6 — $\overline{\text{RESET}}$ DELAY TIME

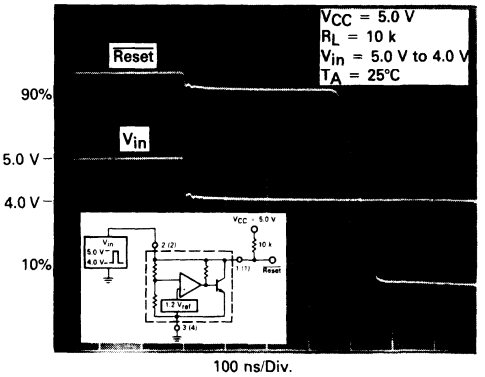


FIGURE 7 — CLAMP DIODE FORWARD CURRENT versus VOLTAGE

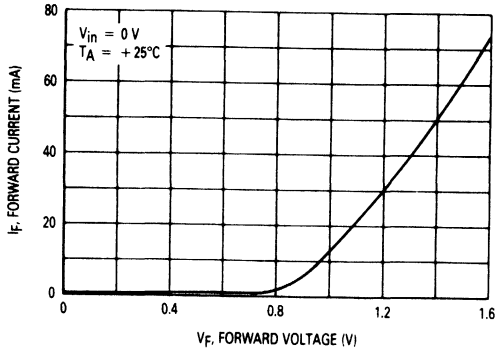
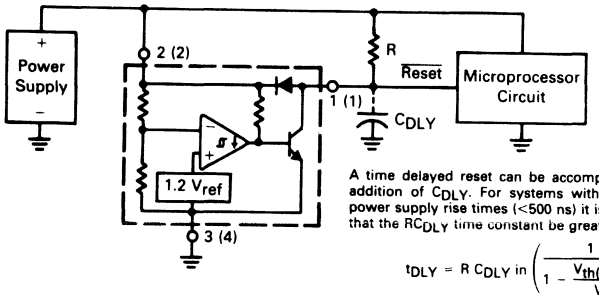


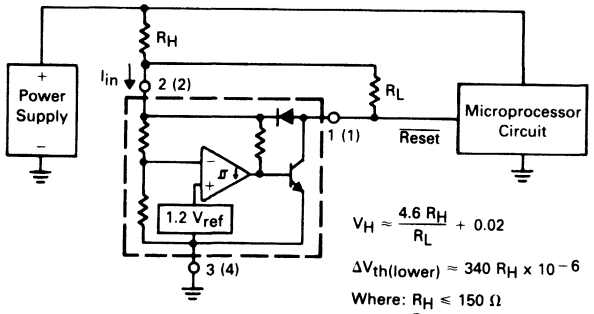
FIGURE 8 — LOW VOLTAGE MICROPROCESSOR RESET



A time delayed reset can be accomplished with the addition of C_{DLY}. For systems with extremely fast power supply rise times (<500 ns) it is recommended that the RC_{DLY} time constant be greater than 5.0 μs.

$$t_{DLY} = R\,C_{DLY} \ln\left(\frac{1}{1 - \frac{V_{th(MPU)}}{V_{in}}}\right)$$

FIGURE 9 — LOW VOLTAGE MICROPROCESSOR RESET WITH ADDITIONAL HYSTERESIS



$$V_H \approx \frac{4.6\,R_H}{R_L} + 0.02$$

$$\Delta V_{th(lower)} \approx 340\,R_H \times 10^{-6}$$

Where: $R_H \leq 150\ \Omega$

$R_L \geq 1.5\ k\Omega, \leq 10\ k\Omega$

Comparator hysteresis can be increased with the addition of resistor R_H. The hysteresis equation has been simplified and does not account for the change of input current I_{in} as V_{CC} crosses the comparator threshold (Figure 4). An increase of the lower threshold $\Delta V_{th(lower)}$ will be observed due to I_{in} which is typically 340 μA at 4.59 V. The equations are accurate to ±10% with R_H less than 150 Ω and R_L between 1.5 kΩ and 10 kΩ.

TEST DATA			
V_H (mV)	ΔV_{th} (mV)	R_H (Ω)	R_L (kΩ)
20	0	0	0
51	3.4	10	1.5
40	6.8	20	4.7
81	6.8	20	1.5
71	10	30	2.7
112	10	30	1.5
100	16	47	2.7
164	16	47	1.5
190	34	100	2.7
327	34	100	1.5
276	51	150	2.7
480	51	150	1.5

FIGURE 10 — VOLTAGE MONITOR

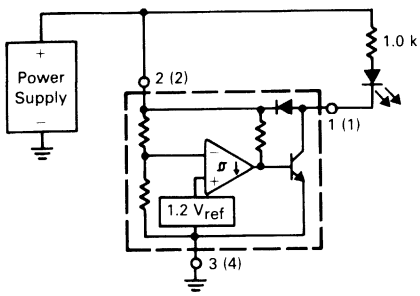


FIGURE 11 — SOLAR POWERED BATTERY CHARGER

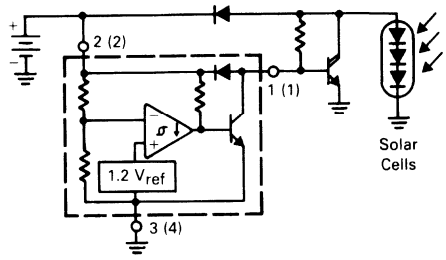
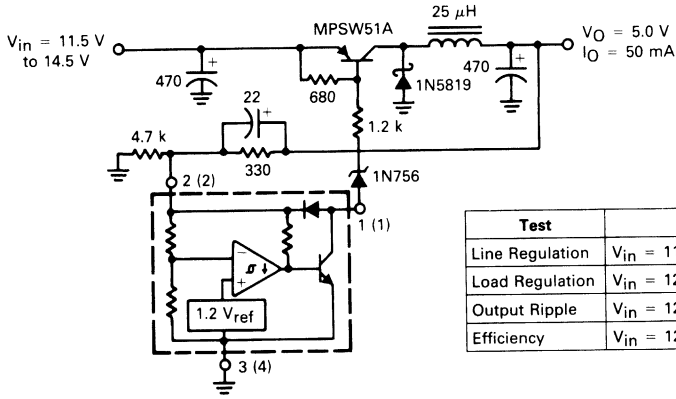
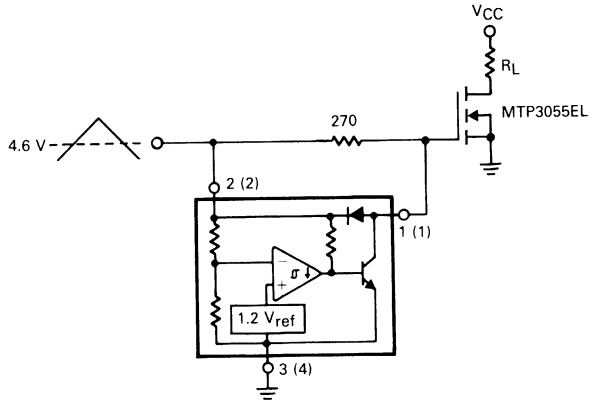


FIGURE 12 — LOW POWER SWITCHING REGULATOR



Test	Conditions	Results
Line Regulation	V_{in} = 11.5 V to 14.5 V, I_O = 50 mA	35 mV
Load Regulation	V_{in} = 12.6 V, I_O = 0 mA to 50 mA	12 mV
Output Ripple	V_{in} = 12.6 V, I_O = 50 mA	60 mV_{p-p}
Efficiency	V_{in} = 12.6 V, I_O = 50 mA	77%

FIGURE 13 — MOSFET LOW-VOLTAGE GATE DRIVE PROTECTION



Overheating of the logic level power MOSFET due to insufficient gate voltage can be prevented with the above circuit. When the input signal is below the 4.6 volt threshold of the MC34064, it's output grounds the gate of the L^2 MOSFET.

MOTOROLA

MC34065
MC33065

Advance Information

HIGH PERFORMANCE DUAL CHANNEL CURRENT MODE CONTROLLER

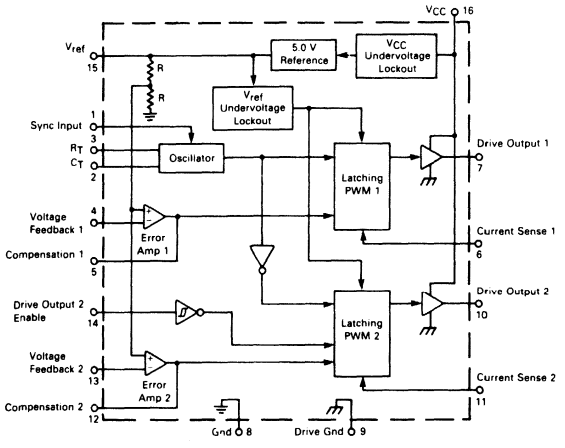
The MC34065 series are high performance, fixed frequency, dual current mode controllers. They are specifically designed for Off-Line and DC to DC converter applications offering the designer a cost effective solution with minimal external components. These integrated circuits feature a unique oscillator for precise duty cycle limit and frequency control, a temperature compensated reference, two high gain error amplifiers, two current sensing comparators, drive output 2 enable pin, and two high current totem pole outputs ideally suited for driving power MOSFETs.

Also included are protective features consisting of input and reference undervoltage lockouts each with hysteresis, cycle-by-cycle current limiting, and a latch for single pulse metering of each output.

These devices are available in dual-in-line and surface mount packages.

- Unique Oscillator for Precise Duty Cycle Limit and Frequency Control
- Current Mode Operation to 500 kHz
- Automatic Feed Forward Compensation
- Separate Latching PWMs for Cycle-By-Cycle Current Limiting
- Internally Trimmed Reference with Undervoltage Lockout
- Drive Output 2 Enable Pin
- Two High Current Totem Pole Outputs
- Input Undervoltage Lockout with Hysteresis
- Low Start-Up and Operating Current
- Direct Interface with Motorola SENSEFET Products

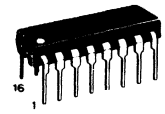
SIMPLIFIED BLOCK DIAGRAM



This document contains information on a new product. Specifications and information herein are subject to change without notice.

HIGH PERFORMANCE DUAL CHANNEL CURRENT MODE CONTROLLER

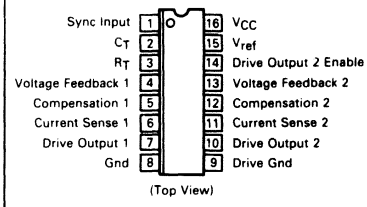
SILICON MONOLITHIC INTEGRATED CIRCUIT



P SUFFIX
PLASTIC PACKAGE
CASE 648-08

DW SUFFIX
PLASTIC PACKAGE
CASE 751G-01
SO-16

PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

Device	Temperature Range	Package
MC34065DW	0 to +70°C	SO-16
MC34065P		Plastic DIP
MC33065DW	−40 to +85°C	SO-16
MC33065P		Plastic DIP

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Total Power Supply and Zener Current	$(I_{CC}+I_Z)$	50	mA
Output Current, Source or Sink (Note 1)	I_O	1.0	A
Output Energy (Capacitive Load per Cycle)	W	5.0	μJ
Current Sense, Enable, and Voltage Feedback Inputs	V_{in}	−0.3 to +5.5	V
Sync Input −High State (Voltage) −Low State (Reverse Current)	V_{IH} I_{IL}	5.5 −5.0	V mA
Error Amp Output Sink Current	I_O	10	mA
Power Dissipation and Thermal Characteristics DW Suffix Package SO-16 Case 751G-01 Maximum Power Dissipation @ T_A = 25°C Thermal Resistance Junction to Air P Suffix Package Case 648-06 Maximum Power Dissipation @ T_A = 25°C Thermal Resistance Junction to Air	 P_D $R_{\theta JA}$ P_D $R_{\theta JA}$	 862 145 1.25 100	 mW °C/W W °C/W
Operating Junction Temperature	T_J	+150	°C
Operating Ambient Temperature MC34065 MC33065	T_A	0 to +70 −40 to +85	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = 15 V [Note 2], R_T = 8.2 kΩ, C_T = 3.3 nF, for typical values T_A = 25°C, for min/max values T_A is the operating ambient temperature range that applies [Note 3].)

Characteristic		Symbol	Min	Typ	Max	Unit
REFERENCE SECTION						
Reference Output Voltage (I_O = 1.0 mA, T_J = 25°C)		V_{ref}	4.9	5.0	5.1	V
Line Regulation (V_{CC} = 11 V to 15 V)		Reg_{line}	—	2.0	20	mV
Load Regulation (I_O = 1.0 mA to 10 mA)		Reg_{load}	—	3.0	25	mV
Total Output Variation over Line, Load, and Temperature		V_{ref}	4.85	—	5.15	V
Output Short Circuit Current		I_{SC}	30	100	—	mA
OSCILLATOR and PWM SECTIONS						
Total Frequency Variation over Line and Temperature (V_{CC} = 11 V to 15 V, T_A = T_{low} to T_{high})	MC34065 MC33065	f_{OSC}	46.5 45	49 49	51.5 53	kHz
Frequency Change with Voltage (V_{CC} = 11 V to 15 V)		$\Delta f_{OSC}/\Delta V$	—	0.2	1.0	%
Duty Cycle at each Output −Maximum −Minimum		DC_{max} DC_{min}	46 —	49.5 —	52 0	%
Sync Input Current −High State (V_{in} = 2.4 V) −Low State (V_{in} = 0.8 V)		I_{IH} I_{IL}	— —	170 80	250 160	μA
ERROR AMPLIFIERS						
Voltage Feedback Input (V_O = 2.5 V)		V_{FB}	2.42	2.5	2.58	V
Input Bias Current (V_{FB} = 5.0 V)		I_{IB}	—	−0.1	−1.0	μA
Open-Loop Voltage Gain (V_O = 2.0 to 4.0 V)		A_{VOL}	65	100	—	dB
Unity Gain Bandwidth (T_J = 25°C)		BW	0.7	1.0	—	MHz
Power Supply Rejection Ratio (V_{CC} = 11 V to 15 V)		PSRR	60	90	—	dB
Output Current −Source (V_O = 3.0 V, V_{FB} = 2.3 V) −Sink (V_O = 1.2 V, V_{FB} = 2.7 V)		I_{Source} I_{Sink}	−0.45 2.0	−1.0 12	— —	mA
Output Voltage Swing −High State (R_L = 15 k to ground, V_{FB} = 2.3 V) −Low State (R_L = 15 k to V_{ref}, V_{FB} = 2.7 V)		V_{OH} V_{OL}	5.0 —	6.2 0.8	— 1.1	V

Notes: 1. Maximum package power dissipation limits must be observed.
2. Adjust V_{CC} above the Start-Up threshold before setting to 15 V.
3. Low duty cycle pulse techniques are used during test to maintain junction temperature as close to ambient as possible.
T_{low} = 0°C for the MC34065 = −40°C for MC33065
T_{high} = +70°C for MC34065 = +85°C for MC33065

ELECTRICAL CHARACTERISTICS (V_{CC} = 15 V [Note 2], R_T = 8.2 kΩ, C_T = 3.3 nF, for typical values T_A = 25°C, for min/max values T_A is the operating ambient temperature range that applies [Note 3].)

Characteristic	Symbol	Min	Typ	Max	Unit
CURRENT SENSE SECTION					
Current Sense Input Voltage Gain (Notes 4 and 5)	A_V	2.75	3.0	3.25	V/V
Maximum Current Sense Input Threshold (Note 4)	V_{th}	430	480	530	mV
Input Bias Current	I_{IB}	—	−2.0	−10	μA
Propagation Delay (Current Sense Input to Output)	$t_{PLN(IN/OUT)}$	—	150	300	ns
DRIVE OUTPUT 2 ENABLE PIN					
Enable Pin Voltage High State (Output 2 Enabled) Low State (Output 2 Disabled)	 V_{IH} V_{IL}	 3.5 0	 — —	 V_{ref} 1.5	V
Low State Input Current (V_{IL} = 0 V)	I_{IB}	100	250	400	μA
DRIVE OUTPUTS					
Output Voltage Low State (I_{Sink} = 20 mA) (I_{Sink} = 200 mA) High State (I_{Source} = 20 mA) (I_{Source} = 200 mA)	 V_{OL} V_{OH} 	 — — 13 12	 0.1 1.6 13.5 13.4	 0.4 2.5 — —	V
Output Voltage with UVLO Activated (V_{CC} = 6.0 V, I_{Sink} = 1.0 mA)	$V_{OL(UVLO)}$	—	0.1	1.1	V
Output Voltage Rise Time (C_L = 1.0 nF)	t_r	—	28	150	ns
Output Voltage Fall Time (C_L = 1.0 nF)	t_f	—	25	150	ns
UNDERVOLTAGE LOCKOUT SECTION					
Start-Up Threshold	V_{th}	13	14	15	V
Minimum Operating Voltage After Turn-On	$V_{CC(min)}$	9.0	10	11	V
TOTAL DEVICE					
Power Supply Current Start-Up (V_{CC} = 12 V) Operating (Note 2)	I_{CC}	 — —	 0.6 20	 1.0 25	mA
Power Supply Zener Voltage (I_{CC} = 30 mA)	V_Z	15.5	17	19	V

Notes: 1. Maximum package power dissipation limits must be observed.
2. Adjust V_{CC} above the Start-Up threshold before setting to 15 V.
3. Low duty cycle pulse techniques are used during test to maintain junction temperature as close to ambient as possible.
T_{low} = 0°C for the MC34065 = −40°C for MC33065 T_{high} = +70°C for MC34065 = +85°C for MC33065
4. This parameter is measured at the latch trip point with V_{fb} = 0 V.
5. Comparator gain is defined as $A_V = \frac{\Delta V \text{ Compensation}}{\Delta V \text{ Current Sense}}$

FIGURE 1 — TIMING RESISTOR versus OSCILLATOR FREQUENCY

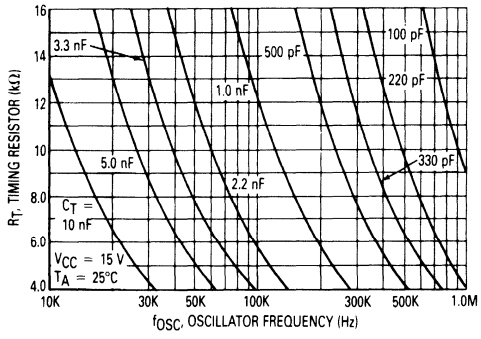


FIGURE 2 — MAXIMUM OUTPUT DUTY CYCLE versus OSCILLATOR FREQUENCY

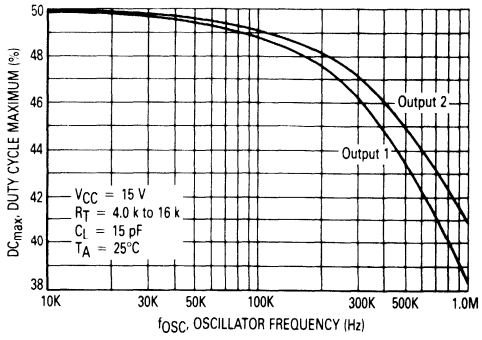


FIGURE 3 — ERROR AMP SMALL-SIGNAL TRANSIENT RESPONSE

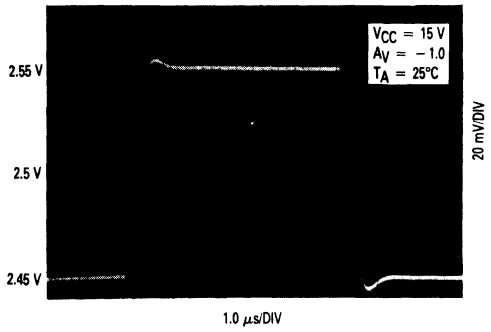


FIGURE 4 — ERROR AMP LARGE-SIGNAL TRANSIENT RESPONSE

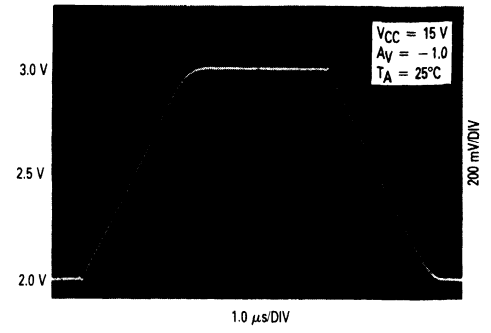


FIGURE 5 — ERROR AMP OPEN-LOOP GAIN AND PHASE versus FREQUENCY

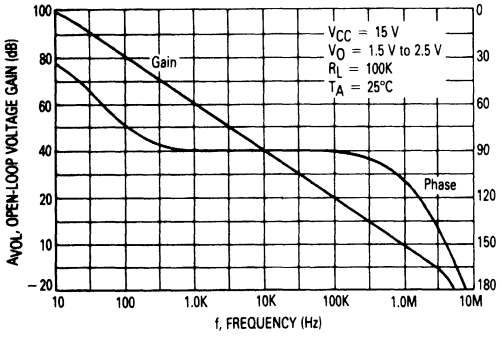


FIGURE 6 — CURRENT SENSE INPUT THRESHOLD versus ERROR AMP OUTPUT VOLTAGE

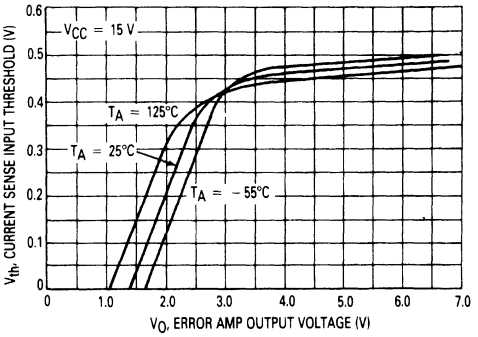


FIGURE 7 — REFERENCE VOLTAGE CHANGE versus SOURCE CURRENT

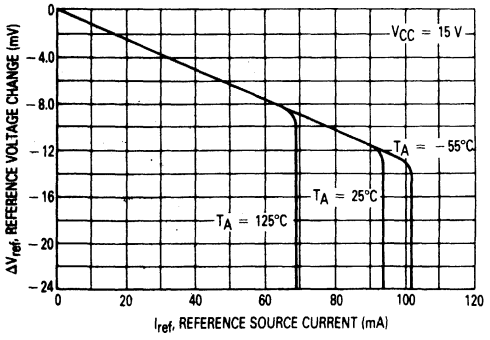


FIGURE 8 — REFERENCE SHORT CIRCUIT CURRENT versus TEMPERATURE

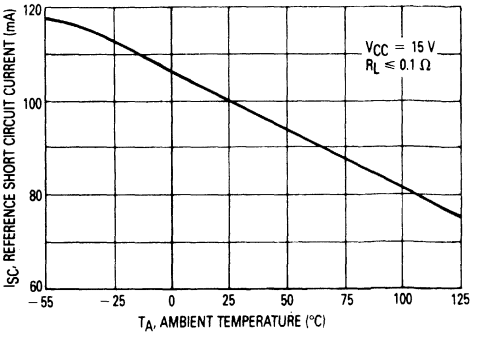


FIGURE 9 — REFERENCE LOAD REGULATION

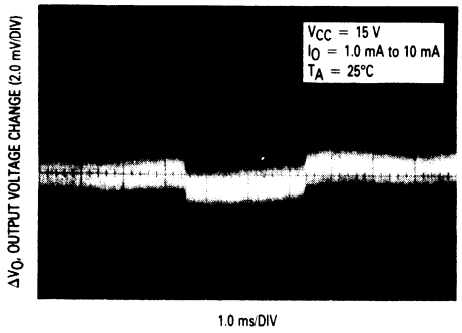


FIGURE 10 — REFERENCE LINE REGULATION

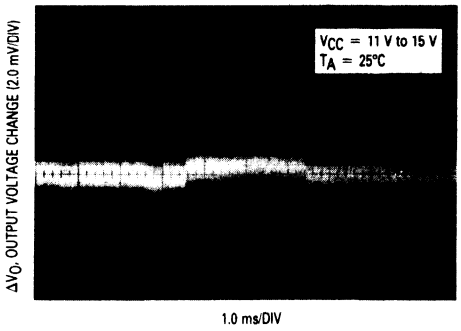


FIGURE 11 — OUTPUT SATURATION VOLTAGE versus LOAD CURRENT

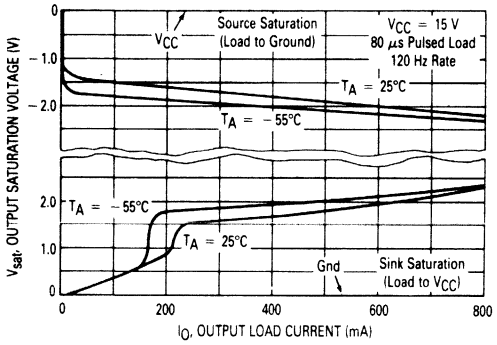


FIGURE 12 — OUTPUT WAVEFORM

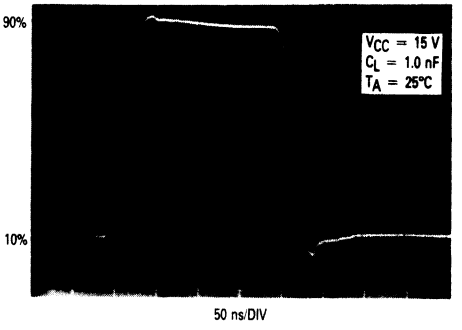


FIGURE 13 — OUTPUT CROSS-CONDUCTION

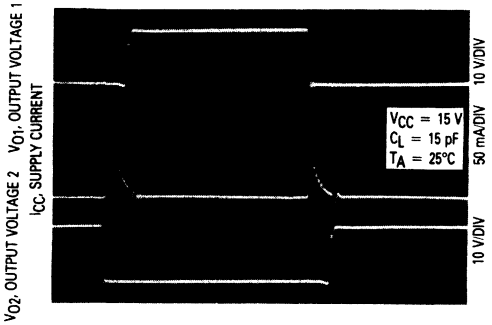
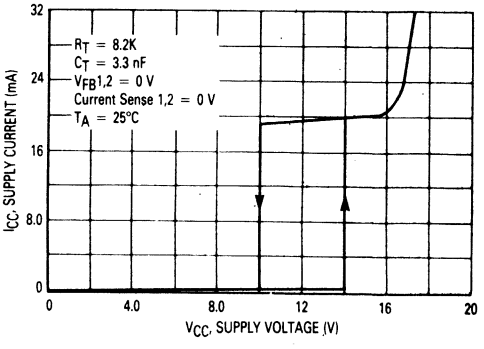


FIGURE 14 — SUPPLY CURRENT versus SUPPLY VOLTAGE



OPERATING DESCRIPTION

The MC34065 series are high performance, fixed frequency, dual channel current mode controllers specifically designed for Off-Line and DC to DC converter applications. These devices offer the designer a cost effective solution with minimal external components where independent regulation of two power converters is required. The Representative Block Diagram is shown in Figure 15. Each channel contains a high gain error amplifier, current sensing comparator, pulse width modulator latch, and totem pole output driver. The oscillator, reference regulator, and undervoltage lockout circuits are common to both channels.

Oscillator

The unique oscillator configuration employed features precise frequency and duty cycle control. The frequency is programmed by the values selected for the timing components R_T and C_T. Capacitor C_T is charged and discharged by an equal magnitude internal current source and sink, generating a symmetrical 50 percent duty cycle waveform at Pin 2. The oscillator peak and valley thresholds are 3.5 V and 1.6 V respectively. The source/sink current magnitude is controlled by resistor R_T. For proper operation over temperature it must be in the range of 4.0 kΩ to 16 kΩ as shown in Figure 1.

As C_T charges and discharges, an internal blanking pulse is generated that alternately drives the center inputs of the upper and lower NOR gates high. This, in conjunction with a precise amount of delay time introduced into each channel, produces well defined non-overlapping output duty cycles. Output 2 is enabled while C_T is charging, and Output 1 is enabled during the discharge. Figure 2 shows the Maximum Output Duty Cycle versus Oscillator Frequency. Note that even at 500 kHz, each output is capable of approximately 44% on-time, making this controller suitable for high frequency power conversion applications.

In many noise sensitive applications it may be desirable to frequency-lock the converter to an external system clock. This can be accomplished by applying a clock signal as shown in Figure 17. For reliable locking, the free-running oscillator frequency should be set about 10% less than the clock frequency. Referring to the timing diagram shown in Figure 16, the rising edge of the clock signal applied to the Sync input, terminates charging of C_T and Drive Output 2 conduction. By tailoring the clock waveform symmetry, accurate duty cycle clamping of either output can be achieved. A circuit method for this, and multi unit synchronization, is shown in Figure 18.

Error Amplifier

Each channel contains a fully-compensated Error Amplifier with access to the inverting input and output. The amplifier features a typical dc voltage gain of 100 dB, and a unity gain bandwidth of 1.0 MHz with 71 degrees of phase margin (Figure 5). The non-inverting input is internally biased at 2.5 V and is not pinned out. The converter output voltage is typically divided down and monitored by the inverting input through a resistor divider. The maximum input bias current is −1.0 μA which will cause an output voltage error that is equal to the product of the input bias current and the equivalent input divider source resistance.

The Error Amp output (Pin 5, 12) is provided for external loop compensation. The output voltage is offset by two diode drops (≈1.4 V) and divided by three before it connects to the inverting input of the Current Sense Comparator. This guarantees that no pulses appear at the Drive Output (Pin 7, 10) when the error amplifier output is at its lowest state (V_{OL}). This occurs when the power supply is operating and the load is removed, or at the beginning of a soft-start interval (Figures 20, 21).

The minimum allowable Error Amp feedback resistance is limited by the amplifier's source current (0.5 mA) and the output voltage (V_{OH}) required to reach the comparator's 0.5 V clamp level with the inverting input at ground. This condition happens during initial system startup or when the sensed output is shorted:

$$R_{f(MIN)} \approx \frac{3.0\ (0.5\ V) + 1.4\ V}{0.5\ mA} = 5800\ \Omega$$

Current Sense Comparator and PWM Latch

The MC34065 operates as a current mode controller, whereby output switch conduction is initiated by the oscillator and terminated when the peak inductor current reaches the threshold level established by the Error Amplifier output. Thus the error signal controls the peak inductor current on a cycle-by-cycle basis. The Current Sense Comparator-PWM Latch configuration used ensures that only a single pulse appears at the Drive Output during any given oscillator cycle. The inductor current is converted to a voltage by inserting a ground-referenced sense resistor R_S in series with the source of output switch Q1. This voltage is monitored by the Current Sense Input (Pin 6, 11) and compared to a level derived from the Error Amp output. The peak inductor current under normal operating conditions is controlled by the voltage at Pin 5, 12 where:

$$I_{pk} = \frac{V_{(Pin\ 5,\ 12)} - 1.4\ V}{3\ R_S}$$

Abnormal operating conditions occur when the power supply output is overloaded or if output voltage sensing is lost. Under these conditions, the Current Sense Comparator threshold will be internally clamped to 0.5 V. Therefore the maximum peak switch current is:

$$I_{pk(max)} = \frac{0.5\ V}{R_S}$$

When designing a high power switching regulator it may be desirable to reduce the internal clamp voltage in order to keep the power dissipation of R_S to a reasonable level. A simple method to adjust this voltage is shown in Figure 19. The two external diodes are used to compensate the internal diodes, yielding a constant clamp voltage over temperature. Erratic operation due to noise pickup can result if there is an excessive reduction of the $I_{pk(max)}$ clamp voltage.

A narrow spike on the leading edge of the current waveform can usually be observed and may cause the power supply to exhibit an instability when the output is lightly loaded. This spike is due to the power transformer interwinding capacitance and output rectifier recovery time. The addition of an RC filter on the Current Sense input with a time constant that approximates the spike duration will usually eliminate the instability; refer to Figure 24.

FIGURE 15 — REPRESENTATIVE BLOCK DIAGRAM

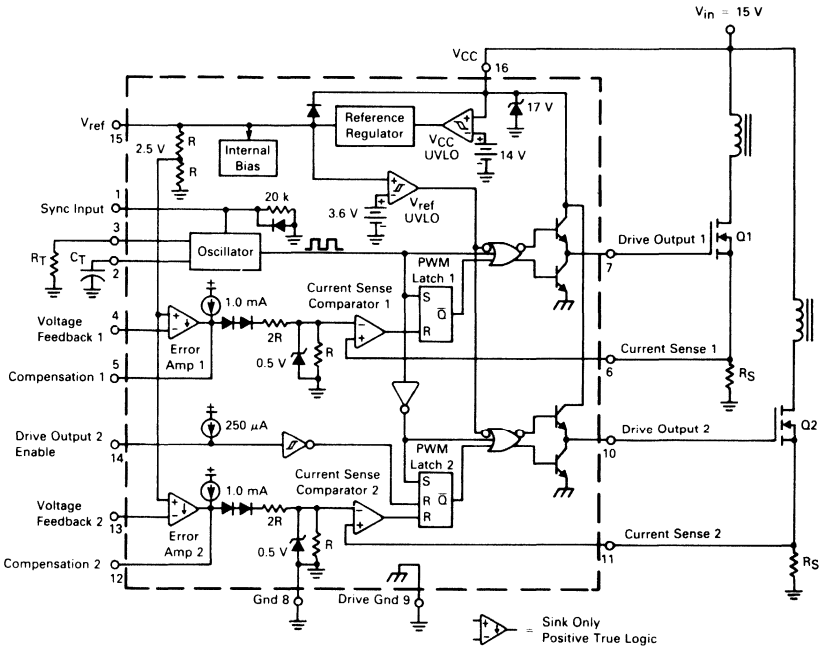
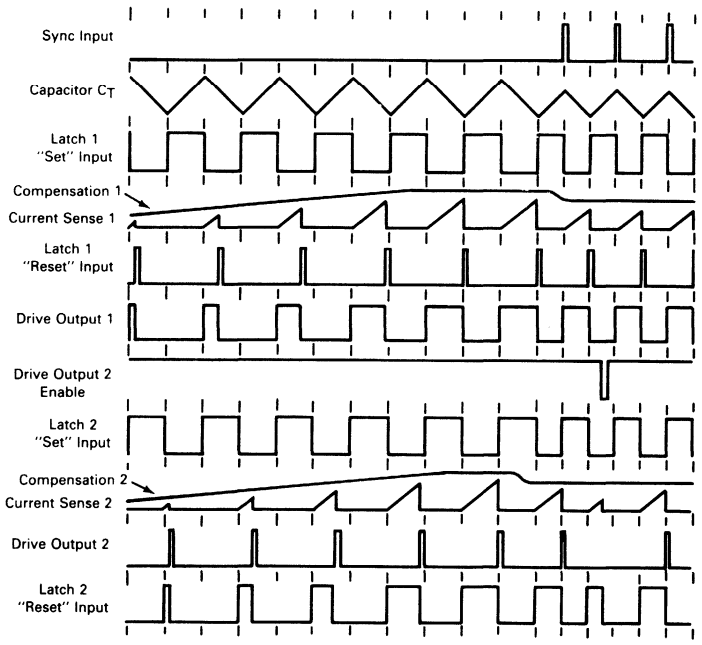


FIGURE 16 — TIMING DIAGRAM



Undervoltage Lockout

Two Undervoltage Lockout comparators have been incorporated to guarantee that the IC is fully functional before the output stages are enabled. The positive power supply terminal (V_{CC}) and the reference output (V_{ref}) are each monitored by separate comparators. Each has built-in hysteresis to prevent erratic output behavior as their respective thresholds are crossed. The V_{CC} comparator upper and lower thresholds are 14 V and 10 V respectively. The hysteresis and low start-up current makes these devices ideally suited to off-line converter applications where efficient bootstrap start-up techniques are required (Figure 28). The V_{ref} comparator disables the Drive Outputs until the internal circuitry is functional. This comparator has upper and lower thresholds of 3.6 V and 3.4 V. A 17 V zener is connected as a shunt regulator from V_{CC} to ground. Its purpose is to protect the IC and power MOSFET gate from excessive voltage that can occur during system start-up. The guaranteed minimum operating voltage after turn-on is 11 V.

Drive Outputs and Drive Ground

Each channel contains a single totem-pole output stage that is specifically designed for direct drive of power MOSFET's. The Drive Outputs are capable of up to ±10 A peak current and have a typical rise and fall times of 28 ns with a 1.0 nF load. Internal circuitry has been added to keep the outputs in a sinking mode whenever an Undervoltage Lockout is active. This characteristic eliminates the need for an external pull-down resistor. Cross-conduction current in the totem-pole output stage has been minimized for high speed operation, as shown in Figure 13. The average added power due to cross-conduction with V_{CC} = 15 V is only 60 mW at 500 kHz.

Although the Drive Outputs were optimized for MOSFETs, they can easily supply the negative base current required by bipolar NPN transistors for enhanced turn-off (Figure 25). The outputs do not contain internal current limiting, therefore an external series resistor may be required to prevent the peak output current from exceeding the ±1.0 A maximum rating. The sink saturation (V_{OL}) is less than 0.4 V at 100 mA.

A separate Drive Ground pin is provided and, with proper implementation, will significantly reduce the level of switching transient noise imposed on the control circuitry. This becomes particularly useful when reducing the $I_{pk(max)}$ clamp level. Figure 23 shows the proper ground connections required for current sensing power MOSFET applications.

Drive Output 2 Enable Pin

This input is used to enable Drive Output 2. Drive Output 1 can be used to control circuitry that must run continuously such as volatile memory and the system clock, or a remote controlled receiver, while Drive Output 2 controls the high power circuitry that is occasionally turned off.

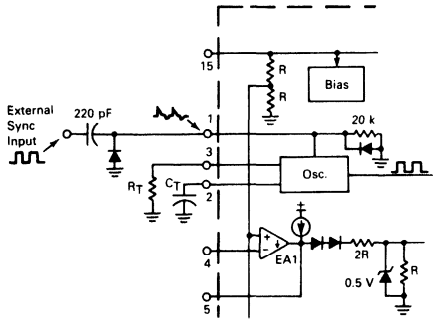
Reference

The 5.0 V bandgap reference is trimmed to ±2.0% tolerance at T_J = 25°C. The reference has short circuit protection and is capable of providing in excess of 30 mA for powering any additional control system circuitry.

Design Considerations

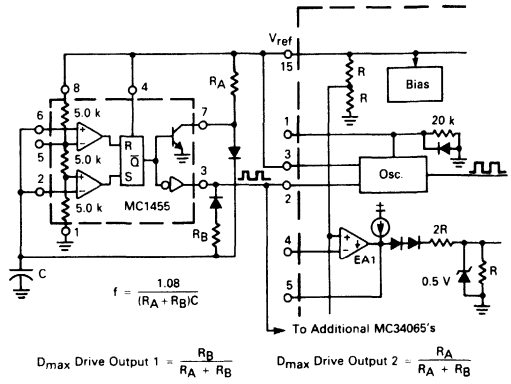
Do not attempt to construct the converter on wire-wrap or plug-in prototype boards. High frequency circuit layout techniques are imperative to prevent pulse-width jitter. This is usually caused by excessive noise pick-up imposed on the Current Sense or Voltage Feedback inputs. Noise immunity can be improved by lowering circuit impedances at these points. The printed circuit layout should contain a ground plane with low current signal and high current switch and output grounds returning on separate paths back to the input filter capacitor. Ceramic bypass capacitors (0.1 μF) connected directly to V_{CC} and V_{ref} may be required depending upon circuit layout. This provides a low impedance path for filtering the high frequency noise. All high current loops should be kept as short as possible using heavy copper runs to minimize radiated EMI. The Error Amp compensation circuitry and the converter output voltage divider should be located close to the IC and as far as possible from the power switch and other noise generating components.

FIGURE 17 — EXTERNAL CLOCK SYNCHRONIZATION



The external diode clamp is required if the negative Sync current is greater than −5.0 mA.

FIGURE 18 — EXTERNAL DUTY CYCLE CLAMP AND MULTI UNIT SYNCHRONIZATION



D_{max} Drive Output 1 = $\frac{R_B}{R_A + R_B}$ D_{max} Drive Output 2 = $\frac{R_A}{R_A + R_B}$

FIGURE 19 — ADJUSTABLE REDUCTION OF CLAMP LEVEL

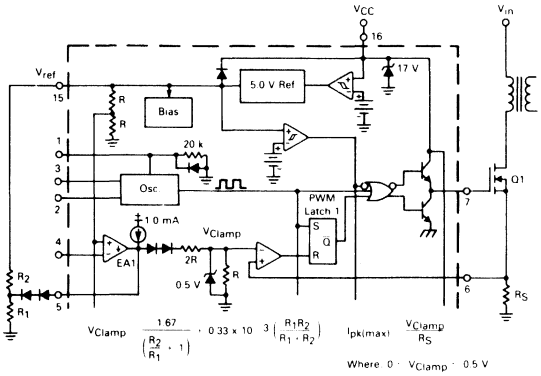


FIGURE 20 — SOFT-START CIRCUIT

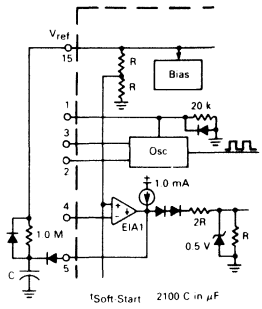


FIGURE 21 — ADJUSTABLE REDUCTION OF CLAMP LEVEL WITH SOFT-START

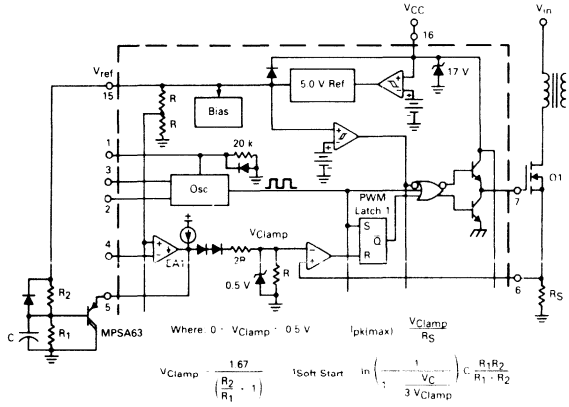
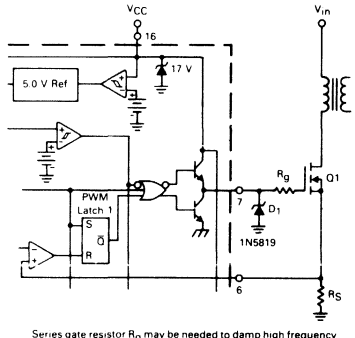
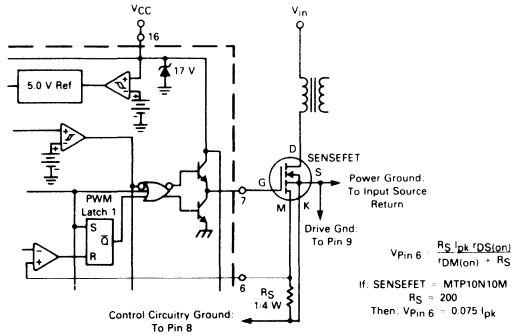


FIGURE 22 — MOSFET PARASITIC OSCILLATIONS



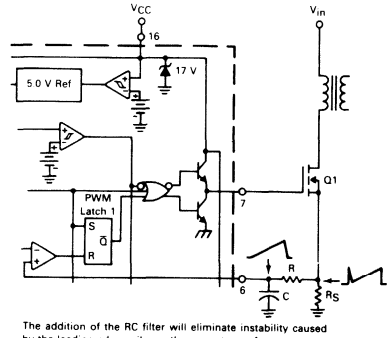
Series gate resistor R_g may be needed to damp high frequency parasitic oscillations caused by the MOSFET input capacitance and any series wiring inductance in the gate-source circuit. R_g will decrease the MOSFET switching speed. Schottky diode D_1 is required if circuit ringing drives the output pin below ground.

FIGURE 23 — CURRENT SENSING POWER MOSFET



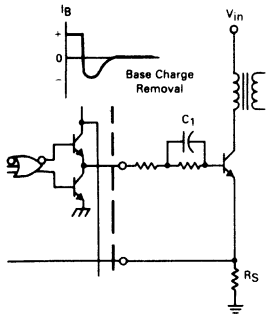
Virtually lossless current sensing can be achieved with the implementation of a SENSEFET power switch. For proper operation during over current conditions, a reduction of the $I_{pk(max)}$ clamp level must be implemented. Refer to Figures 19 and 21.

FIGURE 24 — CURRENT WAVEFORM SPIKE SUPPRESSION



The addition of the RC filter will eliminate instability caused by the leading edge spike on the current waveform.

FIGURE 25 — BIPOLAR TRANSISTOR DRIVE



The totem-pole outputs can furnish negative base current for enhanced transistor turn-off, with the addition of capacitor C_1.

FIGURE 26 — ISOLATED MOSFET DRIVE

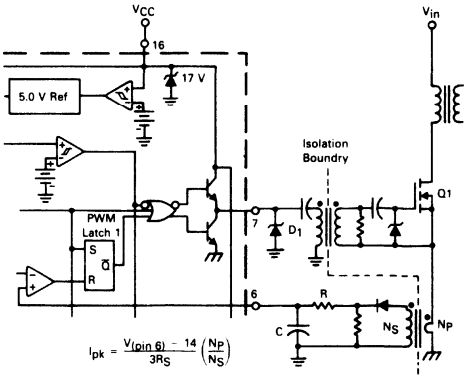
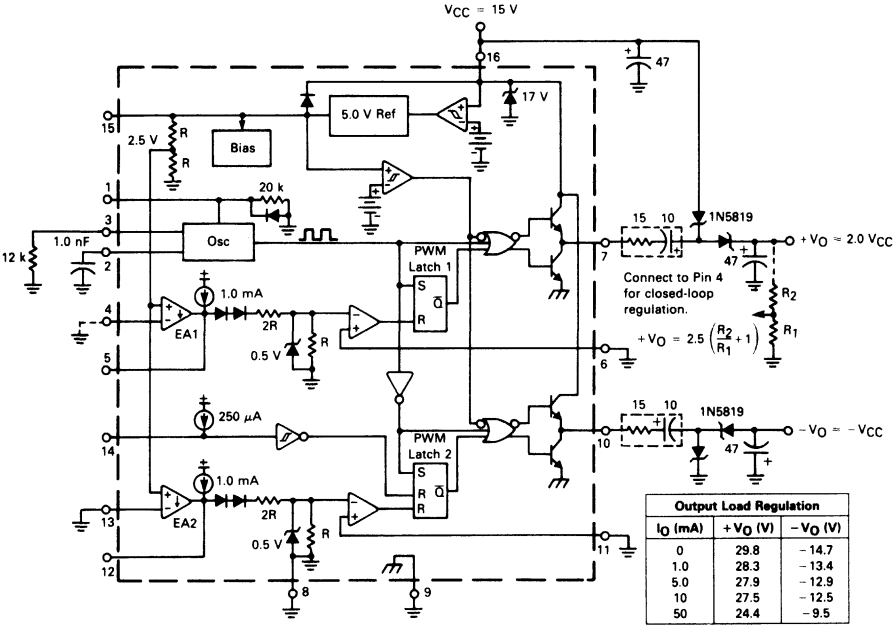
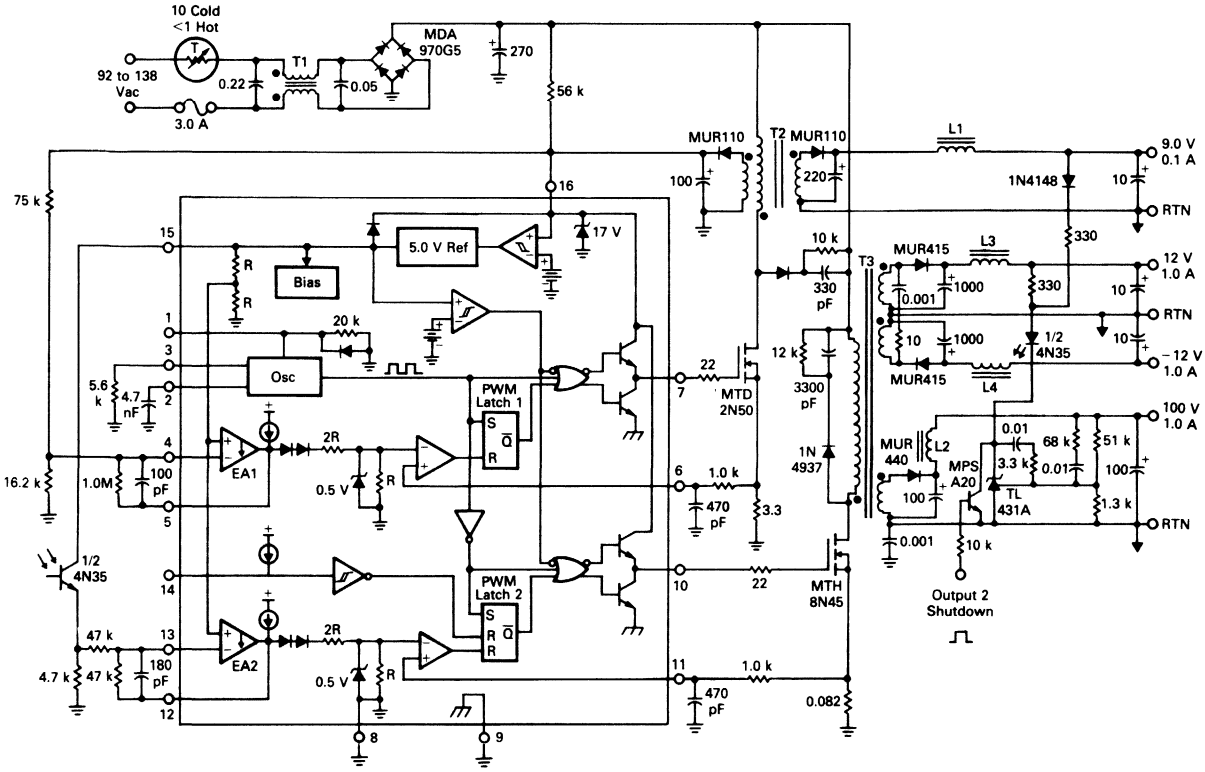


FIGURE 27 — DUAL CHARGE PUMP CONVERTER

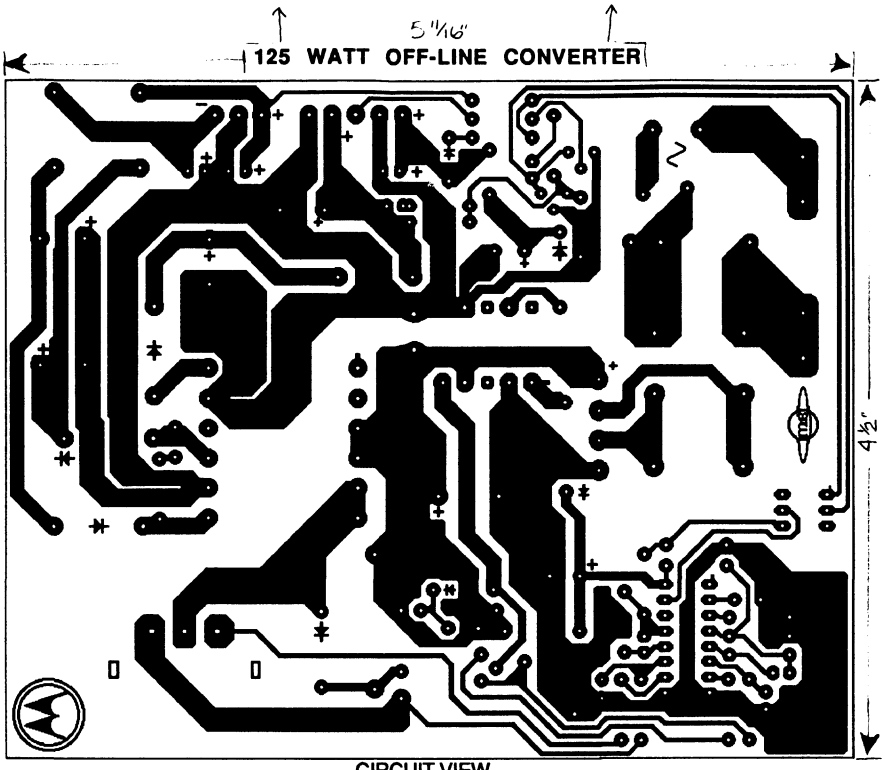


Output Load Regulation		
I_O (mA)	+V_O (V)	−V_O (V)
0	29.8	−14.7
1.0	28.3	−13.4
5.0	27.9	−12.9
10	27.5	−12.5
50	24.4	−9.5

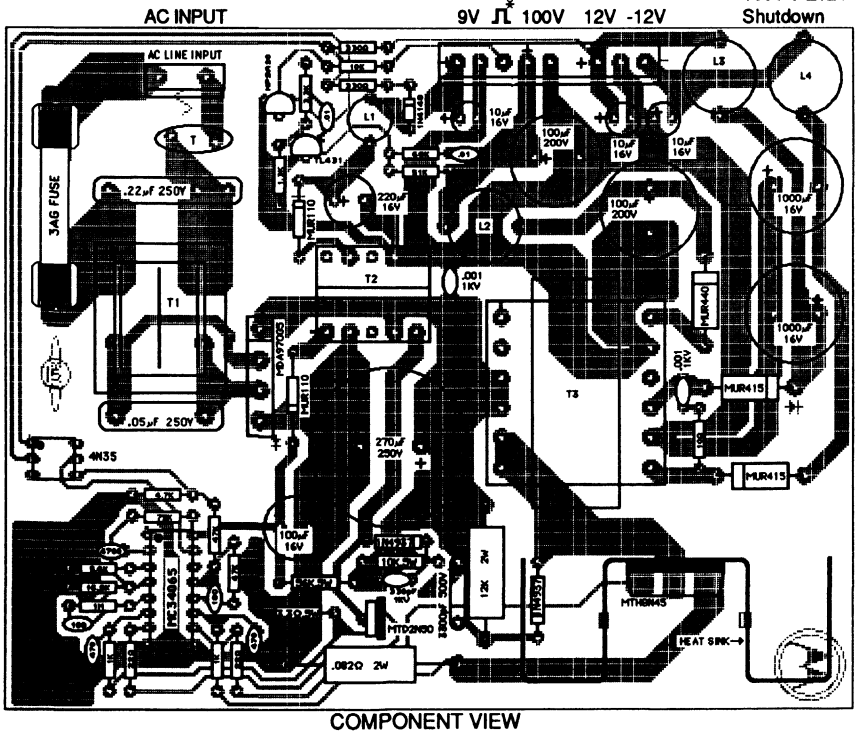
The capacitor is equivalent series resistance must limit the Drive Output current to 1.0 A. An additional series resistor may be required when using tantalum or other low ESR capacitors. The positive output can provide excellent line and load regulation by connecting the R2/R1 resistor divider as shown.



Test	Conditions	Results
Line Regulation	V_{in} = 92 to 138 Vac	
100 V Output	I_O = 1.0 A	Δ = 40 mV or ±0.02%
±12 V Outputs	I_O = ±1.0 A	Δ = 32 mV or ±0.13%
9.0 V Output	I_O = 0.1 A	Δ = 55 mV or ±0.31%
Load Regulation	V_{in} = 115 Vac	
100 V Output	I_O = 0.25 A to 1.0 A	Δ = 50 mV or ±0.025%
±12 V Outputs	I_O = ±0.25 A to ±1.0 A	Δ = 320 mV or ±1.2%
9.0 V Output	I_O = 0.08 A to 0.1 A	Δ = 234 mV or ±1.3%
Output Ripple	V_{in} = 115 Vac	
100 V Output	I_O = 1.0 A	40 mVp-p
±12 V Outputs	I_O = ±1.0 A	100 mVp-p
9.0 V Output	I_O = 0.1 A	60 mVp-p
Short Circuit Current	V_{in} = 115 Vac, R_L = 0.1 Ω	
100 V Output		4.3 A
±12 V Outputs		17 A
9.0 V Output		Output Hiccups
Efficiency	V_{in} = 115 Vac, P_O = 125 W	86%



CIRCUIT VIEW



COMPONENT VIEW

PIN FUNCTION DESCRIPTION

Pin #	Function	Description
1	Sync Input	A narrow rectangular waveform applied to this input will synchronize the Oscillator. A dc voltage within the range of 2.4 V to 5.5 V will inhibit the Oscillator.
2	C_T	Timing capacitor C_T connects from this pin to ground setting the free-running Oscillator frequency range.
3	R_T	Resistor R_T connects from this pin to ground precisely setting the charge current for C_T. R_T must be between 4.0 k and 16 k.
4	Voltage Feedback 1	This pin is the inverting input of Error Amplifier 1. It is normally connected to the switching power supply output through a resistor divider.
5	Compensation 1	This pin is the output of Error Amplifier 1 and is made available for loop compensation.
6	Current Sense 1	A voltage proportional to the inductor current is connected to this input. PWM 1 uses this information to terminate conduction of output switch Q1.
7	Drive Output 1	This pin directly drives the gate of a power MOSFET Q1. Peak currents up to 1.0 A are sourced and sinked by this pin.
8	Gnd	This pin is the control circuitry ground return and is connected back to the source ground.
9	Drive Gnd	This pin is a separate power ground return that is connected back to the power source. It is used to reduce the effects of switching transient noise on the control circuitry.
10	Drive Output 2	This pin directly drives the gate of a power MOSFET Q2. Peak currents up to 1.0 A are sourced and sinked by this pin.
11	Current Sense 2	A voltage proportional to inductor current is connected to this input. PWM 2 uses this information to terminate conduction of output switch Q2.
12	Compensation 2	This pin is the output of Error Amplifier 2 and is made available for loop compensation.
13	Voltage Feedback 2	This pin in the inverting input of Error Amplifier 2. It is normally connected to the switching power supply output through a resistor divider.
14	Drive Output 2 Enable	A logic low at this input disables Drive Output 2.
15	V_{ref}	This is the 5.0 V reference output. It can provide bias for any additional system circuitry.
16	V_{CC}	This pin is the positive supply of the control IC. The minimum operating voltage range after start-up is 11 V to 15.5 V.

MOTOROLA

MC34066
MC33066

Product Preview

HIGH PERFORMANCE RESONANT MODE CONTROLLER

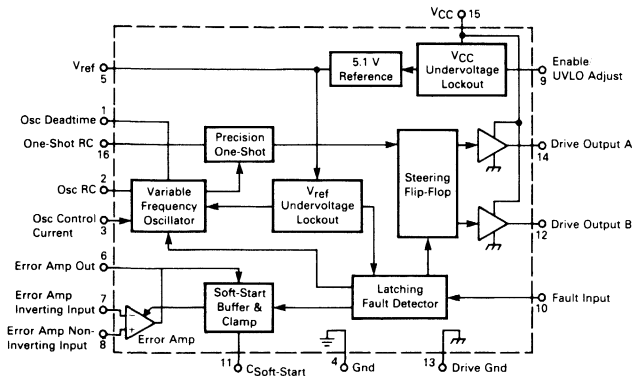
The MC34066 series are high performance resonant mode controllers designed for Off-Line and DC-to-DC converter applications that utilize frequency modulated constant on-time or constant off-time control. These integrated circuits feature a variable frequency oscillator with programmable deadtime, precision retriggerable one-shot timer, temperature compensated reference, high gain wide-bandwidth error amplifier with a precision output clamp, steering flip-flop, and dual high current totem pole outputs ideally suited for driving power MOSFETs.

Also included are protective features consisting of a high speed fault comparator and latch, programmable soft-start circuitry, input undervoltage lockout with selectable thresholds, and reference undervoltage lockout.

These devices are available in dual-in-line and surface mount packages.

- Variable Frequency Oscillator with a Control Range Exceeding 1000:1
- Programmable Oscillator Deadtime Allows Constant Off Time Operation
- Precision Retriggerable One-Shot Timer
- Internally Trimmed Bandgap Reference
- 5.0 MHz Error Amplifier with Precision Output Clamp
- Dual High Current Totem Pole Outputs
- Selectable Undervoltage Lockout Thresholds with Hysteresis
- Enable Input
- Programmable Soft-Start Circuitry
- Low Start-Up Current for Off-Line Operation

SIMPLIFIED BLOCK DIAGRAM



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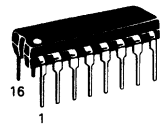
HIGH PERFORMANCE RESONANT MODE CONTROLLER

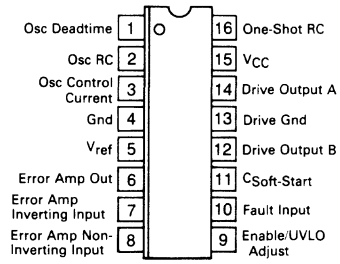
SILICON MONOLITHIC INTEGRATED CIRCUIT

P SUFFIX
PLASTIC PACKAGE
CASE 648-08



DW SUFFIX
PLASTIC PACKAGE
CASE 751G-01
SO-16

PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

Device	Temperature Range	Package
MC34066DW	0 to +70°C	SO-16 Plastic DIP
MC34066P		Plastic DIP
MC33066DW	−40 to +85°C	SO-16 Plastic DIP
MC33066P		Plastic DIP

MOTOROLA

MC34129
MC33129

Advance Information

HIGH PERFORMANCE CURRENT MODE CONTROLLER

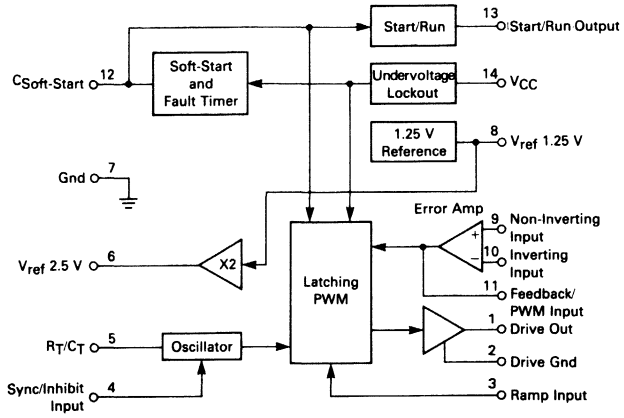
The MC34129 series are high performance current mode switching regulators specifically designed for use in low power digital telephone applications. These integrated circuits feature a unique internal fault timer that provides automatic restart for overload recovery. For enhanced system efficiency, a start/run comparator is included to implement bootstrapped operation of V_{CC}. Other functions contained are a temperature compensated reference, reference amplifier, fully accessible error amplifier, sawtooth oscillator with sync input, pulse width modulator comparator, and a high current totem pole driver ideally suited for driving a power MOSFET.

Also included are protective features consisting of soft-start, undervoltage lockout, cycle-by-cycle current limiting, adjustable dead time, and a latch for single pulse metering.

Although these devices are primarily intended for use in digital telephone systems, they can be used cost effectively in many other applications.

- Current Mode Operation to 300 kHz
- Automatic Feed Forward Compensation
- Latching PWM for Cycle-By-Cycle Current Limiting
- Continuous Retry after Fault Timeout
- Soft-Start with Maximum Peak Switch Current Clamp
- Internally Trimmed 2% Bandgap Reference
- High Current Totem Pole Driver
- Input Undervoltage Lockout
- Low Start-Up and Operating Current
- Direct Interface with Motorola SENSEFET Products

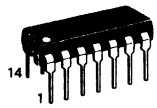
SIMPLIFIED BLOCK DIAGRAM



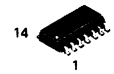
This document contains information on a new product. Specifications and information herein are subject to change without notice.

HIGH PERFORMANCE CURRENT MODE CONTROLLER

SILICON MONOLITHIC INTEGRATED CIRCUIT

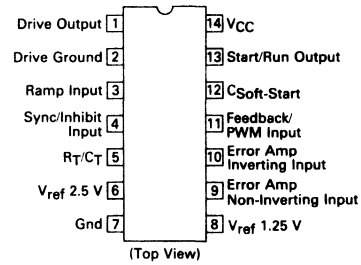


P SUFFIX
PLASTIC PACKAGE
CASE 646-06



D SUFFIX
PLASTIC PACKAGE
CASE 751A-02
SO-14

PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

Device	Temperature Range	Package
MC34129D	0 to +70°C	SO-14 Plastic DIP
MC34129P	0 to +70°C	Plastic DIP
MC33129D	−40 to +85°C	SO-14 Plastic DIP
MC33129P	−40 to +85°C	Plastic DIP

MAXIMUM RATING

Rating	Symbol	Value	Unit
V_{CC} Zener Current	$I_{Z(V_{CC})}$	50	mA
Start/Run Output Zener Current	$I_{Z(Start/Run)}$	50	mA
Analog Inputs (Pins 3, 5, 9, 10, 11, 12)	—	−0.3 to 5.5	V
Sync Input Voltage	V_{sync}	−0.3 to V_{CC}	V
Drive Output Current, Source or Sink	I_{DRV}	1.0	A
Current, Reference Outputs (Pins 6, 8)	I_{ref}	20	mA
Power Dissipation and Thermal Characteristics D Suffix Package SO-14 Case 751A-02 Maximum Power Dissipation @ T_A = 70°C Thermal Resistance Junction to Air P Suffix Package Case 646-06 Maximum Power Dissipation @ T_A = 70°C Thermal Resistance Junction to Air	 P_D $R_{\theta JA}$ P_D $R_{\theta JA}$	 552 145 800 100	 mW °C/W mW °C/W
Operating Junction Temperature	T_J	+150	°C
Operating Ambient Temperature MC34129 MC33129	T_A	 0 to +70 −40 to +85	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = 10 V, T_A = 25°C [Note 1] unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
REFERENCE SECTIONS					
Reference Output Voltage, T_A = 25°C 1.25 V Ref., I_L = 0 mA 2.50 V Ref., I_L = 1.0 mA	V_{ref}	 1.225 2.375	 1.250 2.500	 1.275 2.625	V
Reference Output Voltage, T_A = T_{low} to T_{high} 1.25 V Ref., I_L = 0 mA 2.50 V Ref., I_L = 1.0 mA	V_{ref}	 1.200 2.250	 — —	 1.300 2.750	V
Line Regulation (V_{CC} = 4.0 V to 12 V) 1.25 V Ref., I_L = 0 mA 2.50 V Ref., I_L = 1.0 mA	Reg_{line}	 — —	 2.0 10	 12 50	mV
Load Regulation 1.25 V Ref., I_L = −10 to +500 μA 2.50 V Ref., I_L = −0.1 to +1.0 mA	Reg_{load}	 — —	 1.0 3.0	 12 25	mV
ERROR AMPLIFIER					
Input Offset Voltage (V_{in} = 1.25 V) T_A = 25°C T_A = T_{low} to T_{high}	V_{IO}	 — —	 1.5 —	 — 10	mV
Input Offset Current (V_{in} = 1.25 V)	I_{IO}	—	10	—	nA
Input Bias Current (V_{in} = 1.25 V) T_A = 25°C T_A = T_{low} to T_{high}	I_{IB}	 — —	 25 —	 — 200	nA
Input Common-Mode Voltage Range	V_{ICR}	—	0.5 to 5.5	—	V
Open-Loop Voltage Gain (V_O = 1.25 V)	A_{VOL}	65	87	—	dB
Gain Bandwidth Product (V_O = 1.25 V, f = 100 kHz)	GBW	500	750	—	kHz
Power Supply Rejection Ratio (V_{CC} = 5.0 to 10 V)	PSRR	65	85	—	dB
Output Source Current (V_O = 1.5 V)	I_{Source}	40	80	—	μA
Output Voltage Swing High State (I_{Source} = 0 μA) Low State (I_{Sink} = 500 μA)	 V_{OH} V_{OL}	 1.75 —	 1.96 0.1	 2.25 0.15	V

Note 1. T_{low} = 0°C for MC34129 = −40°C for MC33129 T_{high} = +70°C for MC34129 = +85°C for MC33129

ELECTRICAL CHARACTERISTICS (V_{CC} = 10 V, T_A = 25°C [Note 1] unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
PWM COMPARATOR					
Input Offset Voltage (V_{in} = 1.25 V)	V_{IO}	150	275	400	mV
Input Bias Current	I_{IB}	—	−120	−250	μA
Propagation Delay, Ramp Input to Drive Output	$t_{PLH(IN/DRV)}$	—	250	—	ns
SOFT-START					
Capacitor Charge Current (Pin 12 = 0 V)	I_{chg}	0.75	1.2	1.50	μA
Buffer Input Offset Voltage (V_{in} = 1.25 V)	V_{IO}	—	15	40	mV
Buffer Output Voltage (I_{Sink} = 100 μA)	V_{OL}	—	0.15	0.225	V
FAULT TIMER					
Restart Delay Time	t_{DLY}	200	400	600	μs
START/RUN COMPARATOR					
Threshold Voltage (Pin 12)	V_{th}	—	2.0	—	V
Threshold Hysteresis Voltage (Pin 12)	V_H	—	350	—	mV
Output Voltage (I_{Sink} = 500 μA)	V_{OL}	9.0	10	10.3	V
Output Off-State Leakage Current (V_{OH} = 15 V)	$I_{S/R(leak)}$	—	0.4	2.0	μA
Output Zener Voltage (I_Z = 10 mA)	V_Z	—	(V_{CC} + 7.6)	—	V
OSCILLATOR					
Frequency (R_T = 25.5 kΩ, C_T = 390 pF)	f_{OSC}	80	100	120	kHz
Capacitor C_T Discharge Current (Pin 5 = 1.2 V)	I_{dischg}	240	350	460	μA
Sync Input Current High State (V_{in} = 2.0 V) Low State (V_{in} = 0.8 V)	 I_{IH} I_{IL}	 — —	 40 15	 125 35	μA
Sync Input Resistance	R_{in}	12.5	32	50	kΩ
DRIVE OUTPUT					
Output Voltage High State (I_{Source} = 200 mA) Low State (I_{Sink} = 200 mA)	 V_{OH} V_{OL}	 8.3 —	 8.9 1.4	 — 1.8	V
Low State Holding Current	I_H	—	225	—	μA
Output Voltage Rise Time (C_L = 500 pF)	t_r	—	100	—	ns
Output Voltage Fall Time (C_L = 500 pF)	t_f	—	30	—	ns
Output Pull-Down Resistance	R_{PD}	100	225	350	kΩ
UNDERVOLTAGE LOCKOUT					
Start-Up Threshold	V_{th}	3.0	3.6	4.2	V
Hysteresis	V_H	5.0	10	15	%
TOTAL DEVICE					
Power Supply Current R_T = 25.5 kΩ, C_T = 390 pF, C_L = 500 pF	I_{CC}	1.0	2.5	4.0	mA
Power Supply Zener Voltage (I_Z = 10 mA)	V_Z	12	14.3	—	V

Note 1. T_{low} = 0°C for MC34129 = −40°C for MC33129 T_{high} = +70°C for MC34129 = +85°C for MC33129

FIGURE 1 — TIMING RESISTOR versus OSCILLATOR FREQUENCY

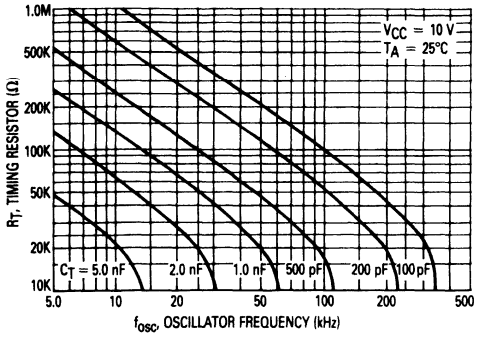


FIGURE 2 — OUTPUT DEAD-TIME versus OSCILLATOR FREQUENCY

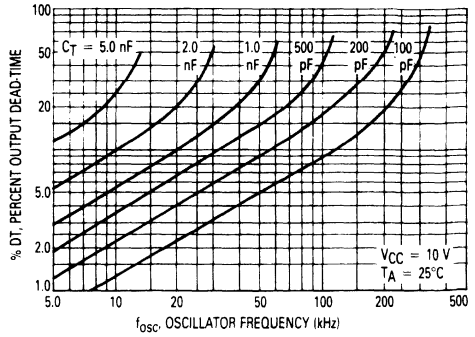


FIGURE 3 — OSCILLATOR FREQUENCY CHANGE versus TEMPERATURE

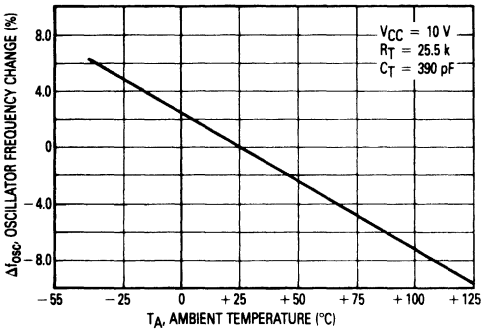


FIGURE 4 — ERROR AMP OPEN-LOOP GAIN AND PHASE versus FREQUENCY

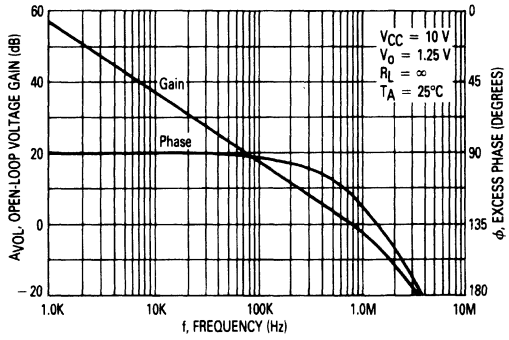


FIGURE 5 — ERROR AMP SMALL-SIGNAL TRANSIENT RESPONSE

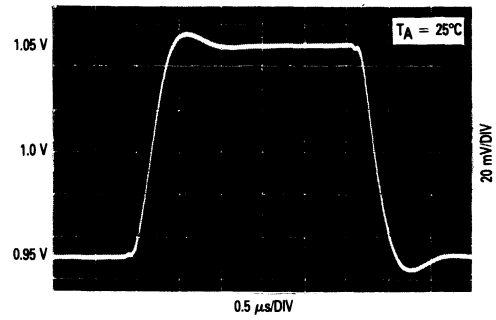


FIGURE 6 — ERROR AMP LARGE-SIGNAL TRANSIENT RESPONSE

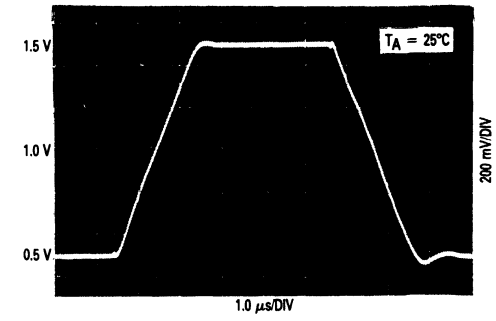


FIGURE 7 — ERROR AMP OPEN-LOOP DC GAIN versus LOAD RESISTANCE

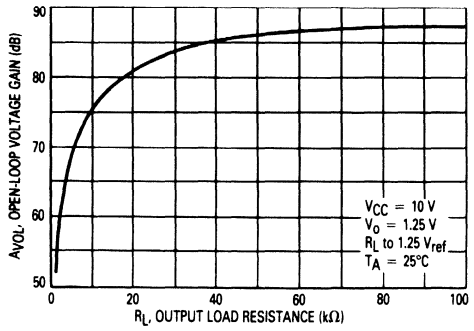


FIGURE 8 — ERROR AMP OUTPUT SATURATION versus SINK CURRENT

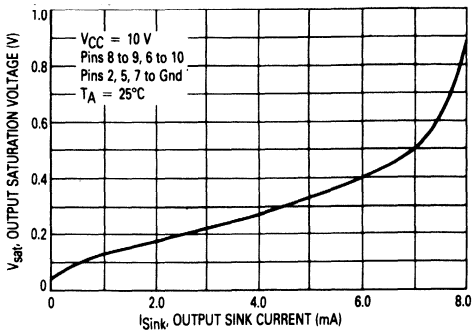


FIGURE 9 — SOFT-START BUFFER OUTPUT SATURATION versus SINK CURRENT

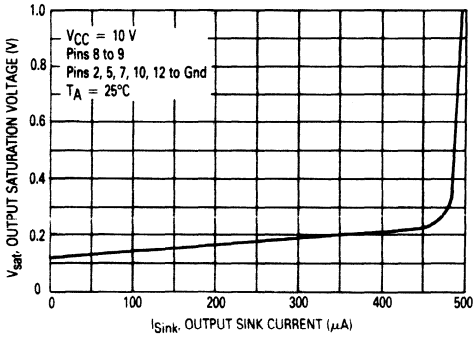


FIGURE 10 — REFERENCE OUTPUT VOLTAGE versus SUPPLY VOLTAGE

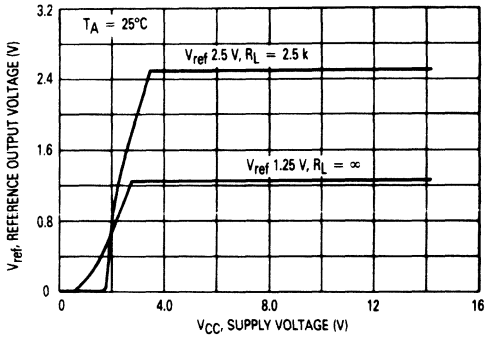


FIGURE 11 — 1.25 V REFERENCE OUTPUT VOLTAGE CHANGE versus SOURCE CURRENT

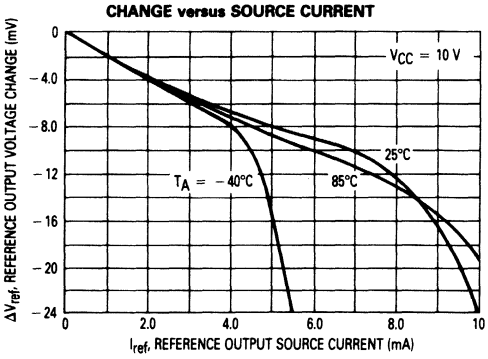


FIGURE 12 — 2.5 V REFERENCE OUTPUT VOLTAGE CHANGE versus SOURCE CURRENT

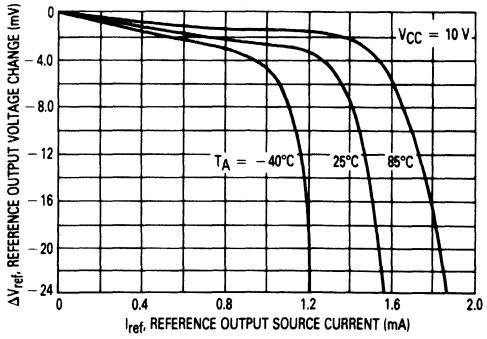


FIGURE 13 — 1.25 V REFERENCE OUTPUT VOLTAGE versus TEMPERATURE

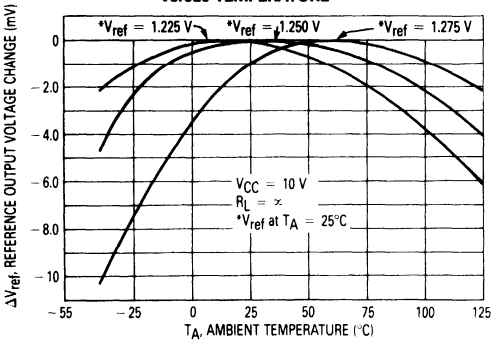


FIGURE 14 — 2.5 V REFERENCE OUTPUT VOLTAGE versus TEMPERATURE

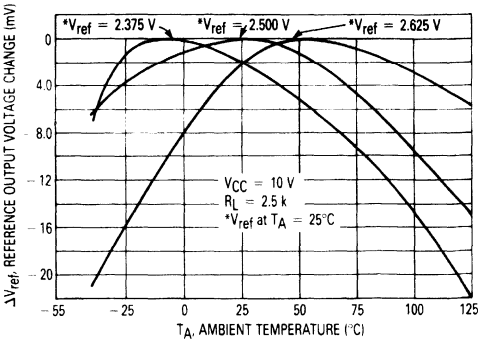


FIGURE 15 — DRIVE OUTPUT SATURATION versus LOAD CURRENT

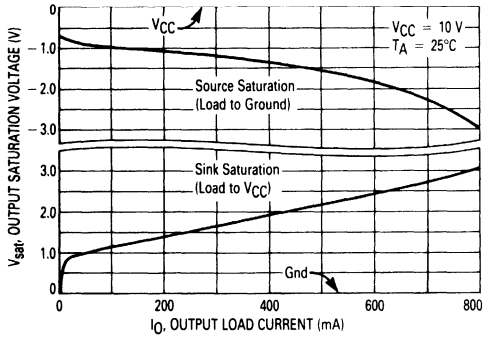


FIGURE 16 — DRIVE OUTPUT WAVEFORM

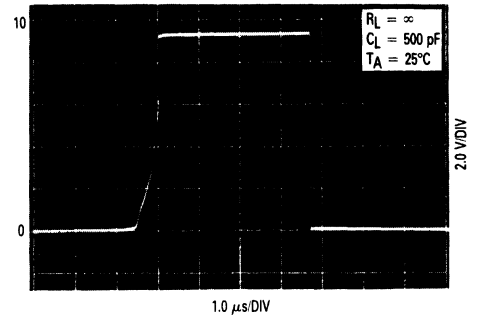
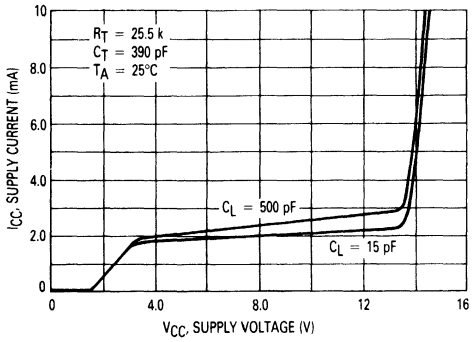


FIGURE 17 — SUPPLY CURRENT versus SUPPLY VOLTAGE



PIN FUNCTION DESCRIPTION

Pin No.	Function	Description
1	Drive Output	This output directly drives the gate of a power MOSFET. Peak currents up to 1.0 A are sourced and sinked by this pin.
2	Drive Ground	This pin is a separate power ground return that is connected back to the power source. It is used to reduce the effects of switching transient noise on the control circuitry.
3	Ramp Input	A voltage proportional to the inductor current is connected to this input. The PWM uses this information to terminate output switch conduction.
4	Sync/Inhibit Input	A rectangular waveform applied to this input will synchronize the Oscillator and limit the maximum Drive Output duty cycle. A dc voltage within the range of 2.0 V to V_{CC} will inhibit the controller.
5	R_T/C_T	The free-running Oscillator frequency and maximum Drive Output duty cycle are programmed by connecting resistor R_T to V_{ref} 2.5 V and capacitor C_T to Ground. Operation to 300 kHz is possible.
6	V_{ref} 2.50 V	This output is derived from V_{ref} 1.25 V. It provides charging current for capacitor C_T through resistor R_T.
7	Ground	This pin is the control circuitry ground return and is connected back to the source ground.
8	V_{ref} 1.25 V	This output furnishes a voltage reference for the Error Amplifier Non-Inverting Input.
9	Error Amp Non-Inverting Input	This is the non-inverting input of the Error Amplifier. It is normally connected to the 1.25 V reference.
10	Error Amp Inverting Input	This is the inverting input of the Error Amplifier. It is normally connected to the switching power supply output through a resistor divider.
11	Feedback/PWM Input	This pin is available for loop compensation. It is connected to the Error Amplifier and Soft-Start Buffer outputs, and the Pulse Width Modulator input.
12	$C_{Soft\text{-}Start}$	A capacitor $C_{Soft\text{-}Start}$ is connected from this pin to Ground for a controlled ramp-up of peak inductor current during start-up.
13	Start/Run Output	This output controls the state of an external bootstrap transistor. During the start mode, operating bias is supplied by the transistor from V_{in}. In the run mode, the transistor is switched off and bias is supplied by an auxiliary power transformer winding.
14	V_{CC}	This pin is the positive supply of the control IC. The controller is functional over a minimum V_{CC} range of 4.2 V to 12 V.

OPERATING DESCRIPTION

The MC34129 series are high performance current mode switching regulator controllers specifically designed for use in low power telecommunication applications. Implementation will allow remote digital telephones and terminals to shed their power cords and derive operating power directly from the twisted pair used for data transmission. Although these devices are primarily intended for use in digital telephone systems, they can be used cost effectively in a wide range of converter applications. A representative block diagram is shown in Figure 18.

OSCILLATOR

The oscillator frequency is programmed by the values selected for the timing components R_T and C_T. Capacitor C_T is charged from the 2.5 V reference through resistor R_T to approximately 1.25 V and discharged by an internal current sink to ground. During the discharge of C_T, the oscillator generates an internal blanking pulse that holds the lower input of the NOR gate high. This causes the Drive Output to be in a low state, thus producing a controlled amount of output deadtime. Figure 1 shows Oscillator Frequency versus R_T and Figure 2, Output Deadtime versus Frequency, both for given values of C_T. Note that many values of R_T and C_T will give the same oscillator frequency but only one combination will yield a specific output deadtime at a given frequency. In many noise sensitive applications it may be desirable to frequency-lock one or more switching regulators to an external system clock. This can be accomplished by applying the clock signal to the Sync/Inhibit Input. For reliable locking, the free-running oscillator frequency should be about 10% less than the clock frequency. Referring to the timing diagram shown in Figure 19, the rising edge of the clock signal applied to the Sync/Inhibit Input, terminates charging of C_T and Drive Output conduction. By tailoring the clock waveform, accurate duty cycle clamping of the Drive Output can be achieved. A circuit method is shown in Figure 20. The Sync/Inhibit Input may also be used as a means for system shutdown by applying a dc voltage that is within the range of 2.0 V to V_{CC}.

PWM COMPARATOR AND LATCH

The MC34129 operates as a current mode controller whereby output switch conduction is initiated by the oscillator and terminated when the peak inductor current reaches a threshold level established by the output of the Error Amp or Soft-Start Buffer (Pin 11). Thus the error signal controls the peak inductor current on a cycle-by-cycle basis. The PWM Comparator-Latch configuration used, ensures that only a single pulse appears at the Drive Output during any given oscillator cycle. The inductor current is converted to a voltage by inserting the ground-referenced resistor R_S in series with the source of output switch Q_1. The Ramp Input adds an offset of 275 mV to this voltage to guarantee that no pulses appear at the Drive Output when Pin 11 is at its lowest state. This occurs at the beginning of the soft-start interval or when the power supply is operating and the load is removed. The peak inductor current under normal operating conditions is controlled by the voltage at Pin 11 where:

$$I_{pk} = \frac{V_{(Pin\ 11)} - 0.275\ V}{R_S}$$

Abnormal operating conditions occur when the power supply output is overloaded or if output voltage sensing is lost. Under these conditions, the voltage at Pin 11 will be internally clamped to 1.95 V by the output of the Soft-Start Buffer. Therefore the maximum peak switch current is:

$$I_{pk(max)} = \frac{1.95\ V - 0.275}{R_S} = \frac{1.675\ V}{R_S}$$

When designing a high power switching regulator it becomes desirable to reduce the internal clamp voltage in order to keep the power dissipation of R_S to a reasonable level. A simple method which adjusts this voltage in discrete increments is shown in Figure 22. This method is possible because the Ramp Input bias current is always negative (typically $-120\ \mu A$). A positive temperature coefficient equal to that of the diode string will be exhibited by $I_{pk(max)}$. An adjustable method that is more precise and temperature stable is shown in Figure 23. Erratic operation due to noise pickup can result if there is an excessive reduction of the clamp voltage. In this situation, high frequency circuit layout techniques are imperative.

A narrow spike on the leading edge of the current waveform can usually be observed and may cause the power supply to exhibit an instability when the output is lightly loaded. This spike is due to the power transformer interwinding capacitance and output rectifier recovery time. The addition of an RC filter on the Ramp Input with a time constant that approximates the spike duration will usually eliminate the instability; refer to Figure 25.

ERROR AMP AND SOFT-START BUFFER

A fully-compensated Error Amplifier with access to both inputs and output is provided for maximum design flexibility. The Error Amplifier output is common with that of the Soft-Start Buffer. These outputs are open-collector (sink only) and are ORed together at the inverting input of the PWM Comparator. With this configuration, the amplifier that demands lower peak inductor current dominates control of the loop. Soft-start is mandatory for stable start-up when power is provided through a high source impedance such as the long twisted pair used in telecommunications. It effectively removes the load from the output of the switching power supply upon initial start-up. The Soft-Start Buffer is configured as a unity gain follower with the non-inverting input connected to Pin 12. An internal 1.0 μA

FIGURE 18 — REPRESENTATIVE BLOCK DIAGRAM

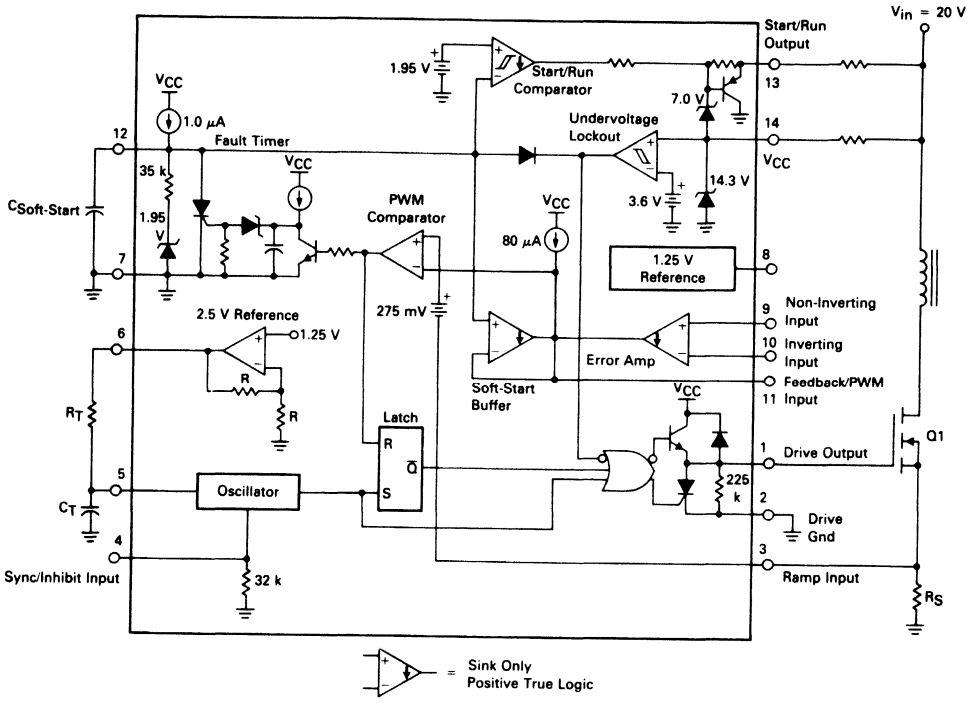
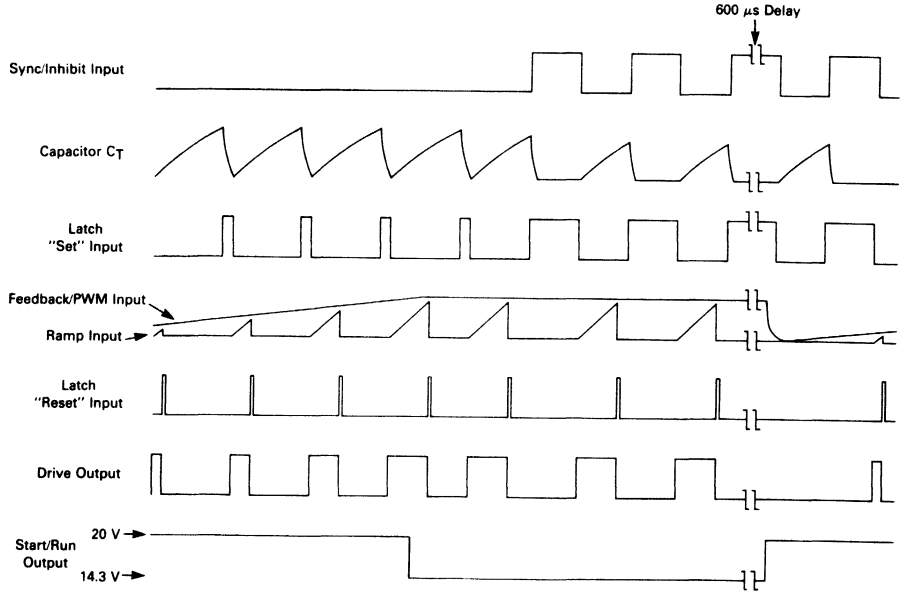


FIGURE 19 — TIMING DIAGRAM



OPERATING DESCRIPTION (continued)

current source charges the soft-start capacitor ($C_{Soft-Start}$) to an internally clamped level of 1.95 V. The rate of change of peak inductor current, during start-up, is programmed by the capacitor value selected. Either the Fault Timer or the Undervoltage Lockout can discharge the soft-start capacitor.

FAULT TIMER

This unique circuit prevents sustained operation in a lockout condition. This can occur with conventional switching control IC's when operating from a power source with a high series impedance. If the power required by the load is greater than that available from the source, the input voltage will collapse, causing the lockout condition. The Fault Timer provides automatic recovery when this condition is detected. Under normal operating conditions, the output of the PWM Comparator will reset the Latch and discharge the internal Fault Timer capacitor on a cycle-by-cycle basis. Under operating conditions where the required power into the load is greater than that available from the source (V_{in}), the Ramp Input voltage (plus offset) will not reach the comparator threshold level (Pin 11), and the output of the PWM Comparator will remain low. If this condition persists for more than 600 μs, the Fault Timer will activate, discharging $C_{Soft-Start}$ and initiating a soft-start cycle. The power supply will operate in a skip cycle or hiccup mode until either the load power or source impedance is reduced. The minimum fault timeout is 200 μs, which limits the useful switching frequency to a minimum of 5.0 kHz.

START/RUN COMPARATOR

A bootstrap start-up circuit is included to improve system efficiency when operating from a high input voltage. The output of the Start/Run Comparator controls the state of an external transistor. A typical application is shown in Figure 21. While $C_{Soft-Start}$ is charging, start-up bias is supplied to V_{CC} (Pin 14) from V_{in} through transistor Q2. When $C_{Soft-Start}$ reaches the 1.95 V clamp level, the Start-Run output switches low (V_{CC} – 50 mV), turning off Q2. Operating bias is now derived from the auxiliary bootstrap winding of the transformer, and all drive power is efficiently converted down from V_{in}. The start time must be long enough for the power supply output to reach regulation. This will ensure that there is sufficient bias voltage at the auxiliary bootstrap winding for sustained operation.

$$t_{Start} = \frac{1.95\ V\ C_{Soft-Start}}{1.0\ \mu A} = 1.95\ C_{Soft-Start\ in\ \mu F}$$

The Start/Run Comparator has 350 mV of hysteresis. The output off-state is clamped to V_{CC} + 7.6 V by the internal zener and PNP transistor base-emitter junction.

DRIVE OUTPUT AND DRIVE GROUND

The MC34129 contains a single totem-pole output stage that was specifically designed for direct drive of power MOSFETs. It is capable of up to ±1.0 A peak drive current and has a typical fall time of 30 ns with a 500 pF load. The totem-pole stage consists of an NPN transistor for turn-on drive and a high speed SCR for turn-off. The SCR design requires less average supply current (I_{CC}) when compared to conventional switching control IC's that use an all NPN totem-pole. The SCR accomplishes this during turn-off of the MOSFET, by utilizing the gate charge as regenerative on-bias, whereas the conventional all transistor design requires continuous base current. Conversion efficiency in low power applications is greatly enhanced with this reduction of I_{CC}. The SCR's low-state holding current (I_H) is typically 225 μA. An internal 225 kΩ pull-down resistor is included to shunt the Drive Output off-state leakage to ground when the Undervoltage Lockout is active. A separate Drive Ground is provided to reduce the effects of switching transient noise imposed on the Ramp Input. This feature becomes particularly useful when the $I_{pk(max)}$ clamp level is reduced. Figure 24 shows the proper implementation of the MC34129 with a current sensing power MOSFET.

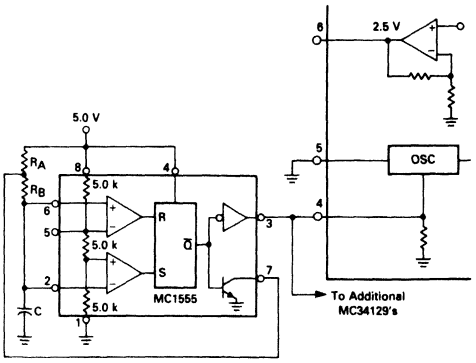
UNDERVOLTAGE LOCKOUT

The Undervoltage Lockout comparator holds the Drive Output and $C_{Soft-Start}$ pins in the low state when V_{CC} is less than 3.6 V. This ensures that the MC34129 is fully functional before the output stage is enabled and a soft-start cycle begins. A built-in hysteresis of 350 mV prevents erratic output behavior as V_{CC} crosses the comparator threshold voltage. A 14.3 V zener is connected as a shunt regulator from V_{CC} to ground. Its purpose is to protect the MOSFET gate from excessive drive voltage during system start-up. An external 9.1 V zener is required when driving low threshold MOSFETs. Refer to Figure 21. The minimum operating voltage range of the IC is 4.2 V to 12 V.

REFERENCES

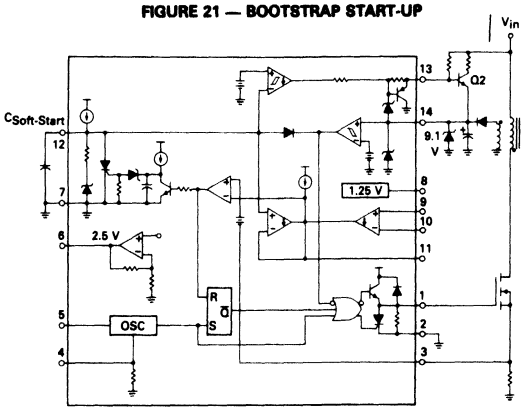
The 1.25 V bandgap reference is trimmed to ±2.0% tolerance at T_A = 25°C. It is intended to be used in conjunction with the Error Amp. The 2.50 V reference is derived from the 1.25 V reference by an internal op amp with a fixed gain of 2.0. It has an output tolerance of ±5.0% at T_A = 25°C and its primary purpose is to supply charging current to the oscillator timing capacitor.

FIGURE 20 — EXTERNAL DUTY CYCLE CLAMP AND MULTI UNIT SYNCHRONIZATION



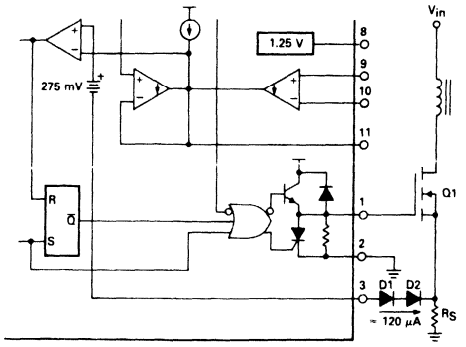
$$f = \frac{1.44}{(R_A + 2R_B)C} \qquad D_{max} = \frac{R_B}{R_A + 2R_B}$$

FIGURE 21 — BOOTSTRAP START-UP



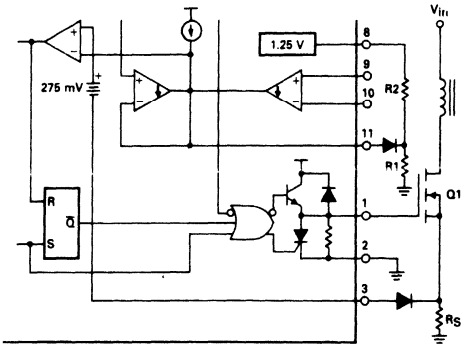
The external 9.1 V zener is required when driving low threshold MOSFETs.

FIGURE 22 — DISCRETE STEP REDUCTION OF CLAMP LEVEL



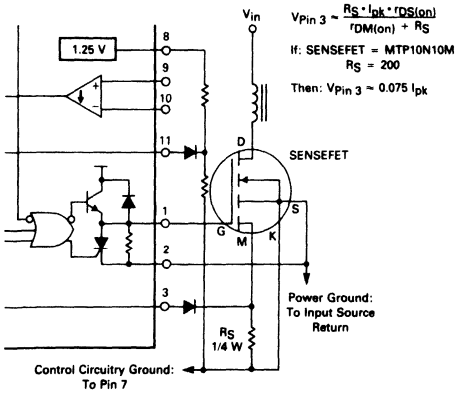
$$I_{pk(max)} = \frac{1.675 - (V_{F(D1)} + V_{F(D2)})}{R_S}$$

FIGURE 23 — ADJUSTABLE REDUCTION OF CLAMP LEVEL



If: $\frac{1.25\ V}{R1 + R2} \geq 1.0\ mA$ Then: $I_{pk(max)} \approx \frac{\frac{1.25}{\left(\frac{R2}{R1} + 1\right)} - 0.275}{R_S}$

FIGURE 24 — CURRENT SENSING POWER MOSFET

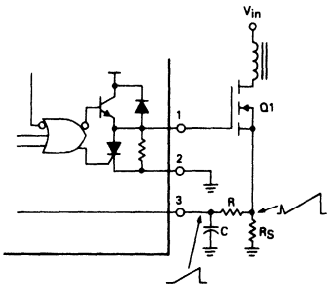


$$V_{Pin\ 3} \approx \frac{R_S \cdot I_{pk} \cdot r_{DS(on)}}{r_{DM(on)} + R_S}$$

If: SENSEFET = MTP10N10M
$R_S = 200$
Then: $V_{Pin\ 3} \approx 0.075\ I_{pk}$

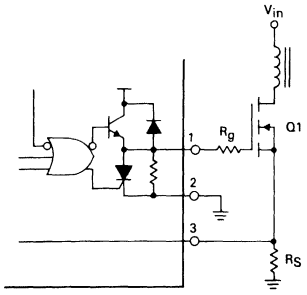
Virtually lossless current sensing can be achieved with the implementation of a SENSEFET power switch.

FIGURE 25 — CURRENT WAVEFORM SPIKE SUPPRESSION



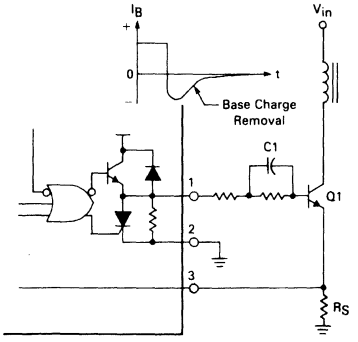
The addition of the RC filter will eliminate instability caused by the leading edge spike on the current waveform.

FIGURE 26 — MOSFET PARASITIC OSCILLATIONS



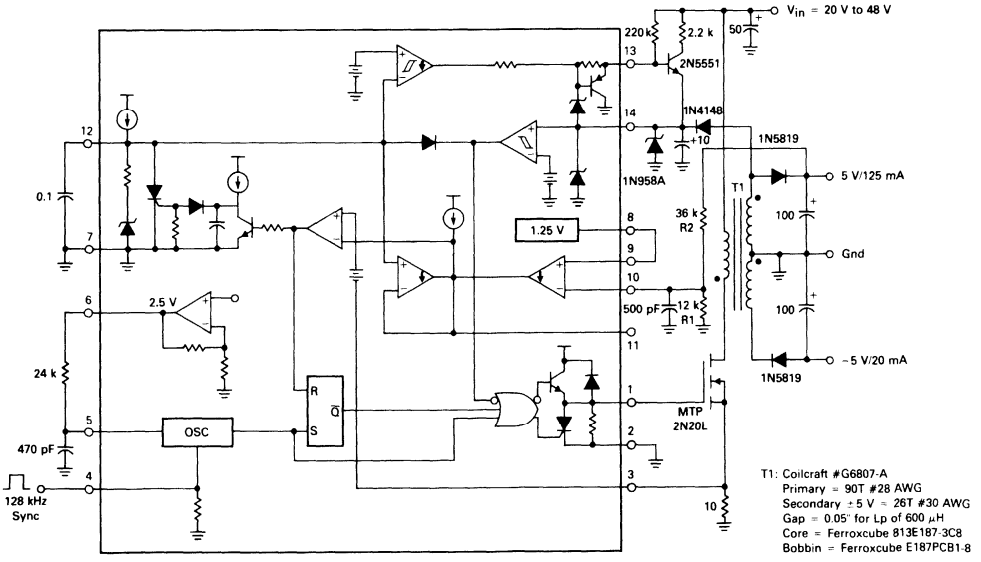
Series gate resistor R_g will damp any high frequency parasitic oscillations caused by the MOSFET input capacitance and any series wiring inductance in the gate-source circuit.

FIGURE 27 — BIPOLAR TRANSISTOR DRIVE



The totem-pole output can furnish negative base current for enhanced transistor turn-off, with the addition of capacitor C1.

FIGURE 28 — NON-ISOLATED 725 mW FLYBACK REGULATOR

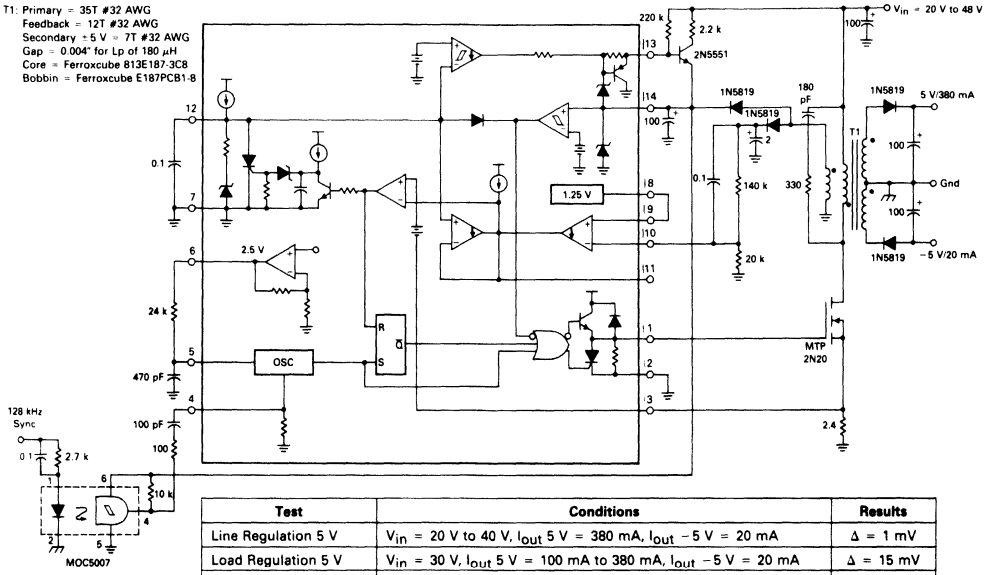


T1: Coilcraft #G6807-A
Primary = 90T #28 AWG
Secondary ±5 V = 26T #30 AWG
Gap = 0.05" for Lp of 600 μH
Core = Ferroxcube 813E187-3C8
Bobbin = Ferroxcube E187PCB1-8

Test	Conditions	Results
Line Regulation 5 V	V_{in} = 20 V to 40 V, I_{out} 5 V = 125 mA, I_{out} −5 V = 20 mA	Δ = 1.0 mV
Load Regulation 5 V	V_{in} = 30 V, I_{out} 5 V = 0 mA to 150 mA, I_{out} −5 V = 20 mA	Δ = 2.0 mV
Output Ripple 5 V	V_{in} = 30 V, I_{out} 5 V = 125 mA, I_{out} −5 V = 20 mA	150 mVp-p
Efficiency	V_{in} = 30 V, I_{out} 5 V = 125 mA, I_{out} −5 V = 20 mA	77%

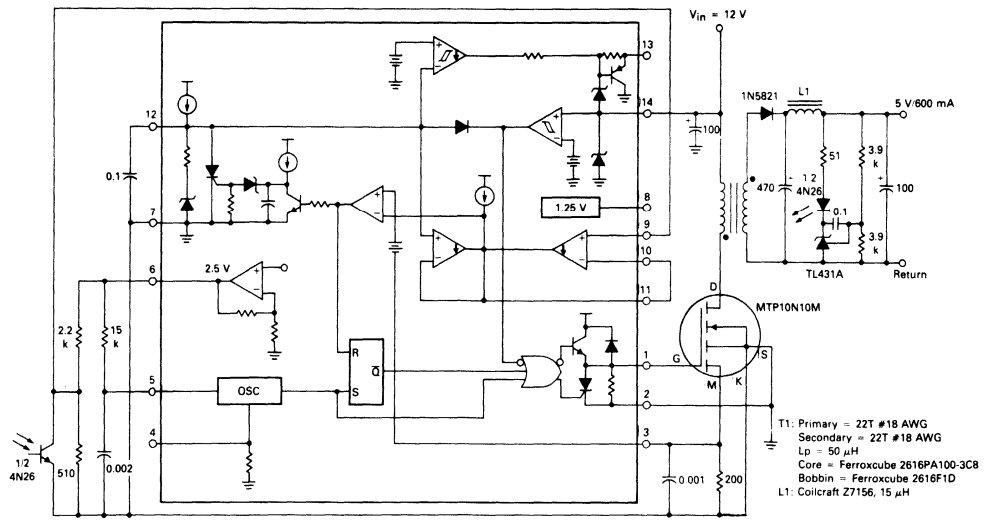
$$V_{out} = 1.25\left(\frac{R2}{R1} + 1\right)$$

FIGURE 29 — ISOLATED 2.0 W FLYBACK REGULATOR



Test	Conditions	Results
Line Regulation 5 V	V_{in} = 20 V to 40 V, I_{out} 5 V = 380 mA, I_{out} −5 V = 20 mA	Δ = 1 mV
Load Regulation 5 V	V_{in} = 30 V, I_{out} 5 V = 100 mA to 380 mA, I_{out} −5 V = 20 mA	Δ = 15 mV
Output Ripple 5 V	V_{in} = 30 V, I_{out} 5 V = 380 mA, I_{out} −5 V = 20 mA	150 mVp-p
Efficiency	V_{in} = 30 V, I_{out} 5 V = 380 mA, I_{out} −5 V = 20 mA	73%

FIGURE 30 — ISOLATED 3.0 W FLYBACK REGULATOR WITH SECONDARY SIDE SENSING



Test	Conditions	Results
Line Regulation	V_{in} = 8 V to 12 V, I_{out} 600 mA	Δ = 1 mV
Load Regulation	V_{in} = 12 V, I_{out} = 100 mA to 600 mA	Δ = 8 mV
Output Ripple	V_{in} = 12 V, I_{out} = 600 mA	20 mVp-p
Efficiency	V_{in} = 12 V, I_{out} = 600 mA	81%

An economical method of achieving secondary sensing is to combine the TL431A with a 4N26 optocoupler.

MOTOROLA

MC34160
MC33160

Product Preview

MICROPROCESSOR VOLTAGE REGULATOR AND SUPERVISORY CIRCUIT

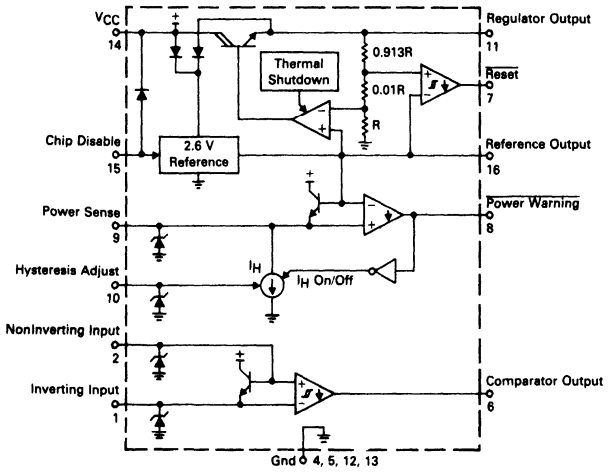
The MC34160 Series is a voltage regulator and supervisory circuit containing many of the necessary monitoring functions required in microprocessor based systems. It is specifically designed for appliance and industrial applications, offering the designer a cost effective solution with minimal external components. These integrated circuits feature a 5.0 V/100 mA regulator with short circuit current limiting, pinned out 2.6 V bandgap reference, low voltage reset comparator, power warning comparator with programmable hysteresis, and an uncommitted comparator ideally suited for microprocessor line synchronization.

Additional features include a chip disable input for low standby current, and internal thermal shutdown for over temperature protection.

These devices are contained in a 16 pin dual-in-line heat tab plastic package for improved thermal conduction.

- 5.0 Volt Regulator Output Current in Excess of 100 mA
- Internal Short Circuit Current Limiting
- Pinned Out 2.6 V Reference
- Low Voltage Reset Comparator
- Power Warning Comparator with Programmable Hysteresis
- Uncommitted Comparator
- Low Standby Current
- Internal Thermal Shutdown Protection
- Heat Tab Power Package

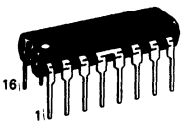
REPRESENTATIVE BLOCK DIAGRAM



This document contains information on a product under development. Motorola reserves the right to change or discontinue this product without notice.

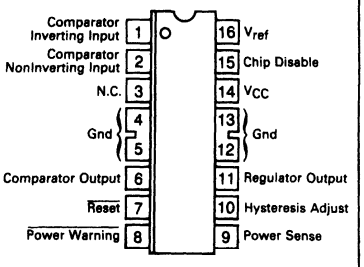
MICROPROCESSOR VOLTAGE REGULATOR/ SUPERVISORY CIRCUIT

SILICON MONOLITHIC INTEGRATED CIRCUIT



P SUFFIX
PLASTIC PACKAGE
CASE 648C-02

PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

Device	Temperature Range	Package
MC34160P	0°C to +70°C	Plastic DIP
MC33160P	−40°C to +85°C	Plastic DIP

MAXIMUM RATING

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	40	V
Chip Disable Input Voltage (Pin 15, Note 1)	V_{CD}	−0.3 to V_{CC}	V
Comparator Input Current (Pin 1, 2, 9)	I_{in}	−2.0 to +2.0	mA
Comparator Output Voltage (Pin 6, 7, 8)	V_O	40	V
Comparator Output Sink Current (Pin 6, 7, 8)	I_{Sink}	10	mA
Power Dissipation and Thermal Characteristics Maximum Power Dissipation @ T_A = 70°C Thermal Resistance Junction to Air Thermal Resistance Junction to Case (Pin 4, 5, 12, 13)	 P_D $R_{\theta JA}$ $R_{\theta JC}$	 1000 80 15	 mW °C/W °C/W
Operating Junction Temperature	T_J	+150	°C
Operating Ambient Temperature MC34160 MC33160	T_A	 0 to +70 −40 to +85	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = 30 V, I_O = 10 mA, I_{ref} = 100 μA) For typical values T_A = 25°C, for min/max values T_A is the operating ambient temperature range that applies [Notes 2 and 3] unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
REGULATOR SECTION					
Total Output Variation (V_{CC} = 7.0 V to 40 V, I_O = 1.0 mA to 100 mA, T_A = T_{low} to T_{high})	V_O	4.75	5.0	5.25	V
Line Regulation (V_{CC} = 7.0 V to 40 V, T_A = 25°C)	Reg_{line}	—	5.0	40	mV
Load Regulation (I_O = 1.0 mA to 100 mA, T_A = 25°C)	Reg_{load}	—	20	50	mV
Ripple Rejection (V_{CC} = 25 V to 35 V, I_O = 40 mA, f = 120 Hz, T_A = 25°C)	RR	50	65	—	dB
REFERENCE SECTION					
Total Output Variation (V_{CC} = 7.0 V to 40 V, I_O = 0.1 mA to 2.0 mA, T_A = T_{low} to T_{high})	V_{ref}	2.47	2.6	2.73	V
Line Regulation (V_{CC} = 5.0 V to 40 V, T_A = 25°C)	Reg_{line}	—	2.0	20	mV
Load Regulation (I_O = 0.1 mA to 2.0 mA, T_A = 25°C)	Reg_{load}	—	4.0	30	mV
RESET COMPARATOR					
Threshold Voltage High State Output (Pin 11 Increasing) Low State Output (Pin 11 Decreasing) Hysteresis	 V_{IH} V_{IL} V_H	 — 4.55 0.02	 (V_O − 0.11) (V_O − 0.18) 0.07	 (V_O − 0.05) — —	V
Output Sink Saturation (V_{CC} = 4.5 V, I_{Sink} = 2.0 mA)	V_{OL}	—	—	0.4	V
Output Off-State Leakage (V_{OH} = 40 V)	I_{OH}	—	—	4.0	μA

Notes:
1. The maximum voltage range is −0.3 V to V_{CC} or +35 V, whichever is less.
2. T_{low} = 0°C for MC34160 = −40°C for MC33160 T_{high} = +70°C for MC34160 = +85°C for MC33160
3. Low duty cycle pulse testing techniques are used during test to maintain junction temperature as close to ambient as possible.

ELECTRICAL CHARACTERISTICS — Continued (V_{CC} = 30 V, I_O = 10 mA, I_{ref} = 100 μA) For typical values T_A = 25°C, for min/max values T_A is the operating ambient temperature range that applies [Notes 2 and 3] unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
POWER WARNING COMPARATOR					
Input Offset Voltage	V_{IO}	—	1.2	10	mV
Input Bias Current ($V_{Pin\ 9}$ = 3.0 V)	I_{IB}	—	—	0.5	μA
Input Hysteresis Current ($V_{Pin\ 9}$ = V_{ref} − 100 mV) $R_{Pin\ 10}$ = 24 k $R_{Pin\ 10}$ = ∞	I_H	 40 4.5	 50 7.5	 60 11	μA
Output Sink Saturation (I_{Sink} = 2.0 mA)	V_{OL}	—	0.13	0.4	V
Output Off-State Leakage (V_{OH} = 40 V)	I_{OH}	—	—	4.0	μA
UNCOMMITTED COMPARATOR					
Input Offset Voltage (Output Transition Low to High)	V_{IO}	—	—	20	mV
Input Hysteresis Voltage (Output Transition High to Low)	I_H	140	200	260	mV
Input Bias Current ($V_{Pin\ 1, 2}$ = 2.6 V)	I_{IB}	—	—	−1.0	μA
Input Common-Mode Voltage Range	V_{ICR}	0.6 to 5.0	—	—	V
Output Sink Saturation (I_{Sink} = 2.0 mA)	V_{OL}	—	0.13	0.4	V
Output Off-State Leakage (V_{OH} = 40 V)	I_{OH}	—	—	4.0	μA
TOTAL DEVICE					
Chip Disable Threshold Voltage (Pin 15) High State (Chip Disabled) Low State (Chip Enabled)	 V_{IH} V_{IL}	 2.5 —	 — —	 — 0.8	V
Chip Disable Input Current (Pin 15) High State (V_{in} = 2.5 V) Low State (V_{in} = 0.8 V)	 I_{IH} I_{IL}	 — —	 — —	 100 30	μA
Chip Disable Input Resistance (Pin 15)	R_{in}	50	100	—	kΩ
Operating Voltage Range V_O (Pin 11) Regulated V_{ref} (Pin 16) Regulated	V_{CC}	 7.0 to 40 5.0 to 40	 — —	 — —	V
Power Supply Current Standby (Chip Disable High State) Operating (Chip Disable Low State)	I_{CC}	 — —	 0.18 1.5	 0.35 3.0	mA

FIGURE 1 — REGULATOR OUTPUT VOLTAGE CHANGE versus SOURCE CURRENT

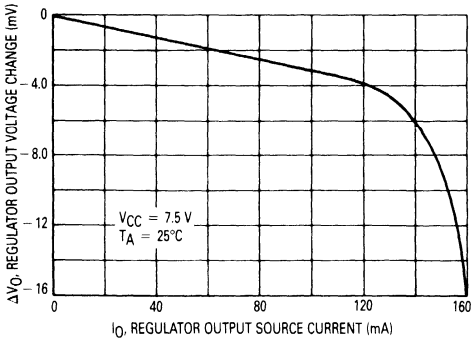


FIGURE 2 — REFERENCE AND REGULATOR OUTPUT versus SUPPLY VOLTAGE

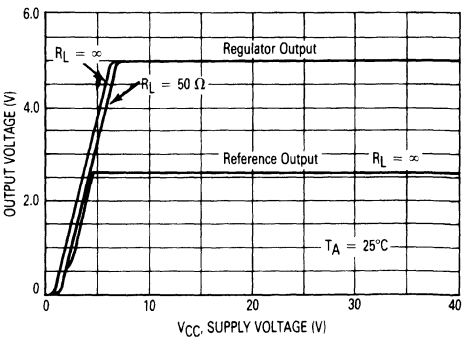


FIGURE 3 — REFERENCE OUTPUT VOLTAGE CHANGE versus SOURCE CURRENT

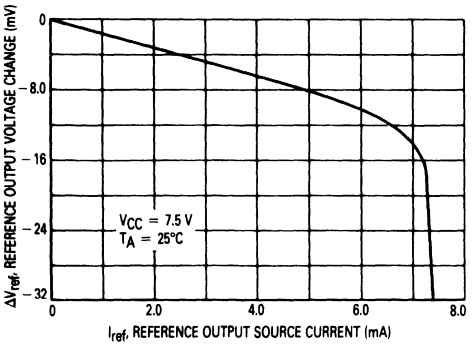


FIGURE 4 — POWER WARNING HYSTERESIS CURRENT versus PROGRAMMING RESISTOR

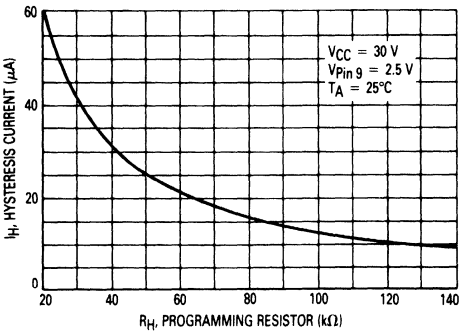


FIGURE 5 — POWER WARNING COMPARATOR DELAY versus TEMPERATURE

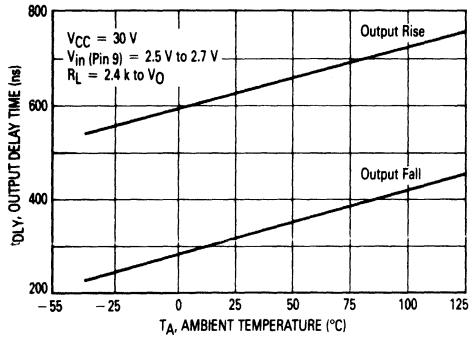


FIGURE 6 — UNCOMMITTED COMPARATOR DELAY versus TEMPERATURE

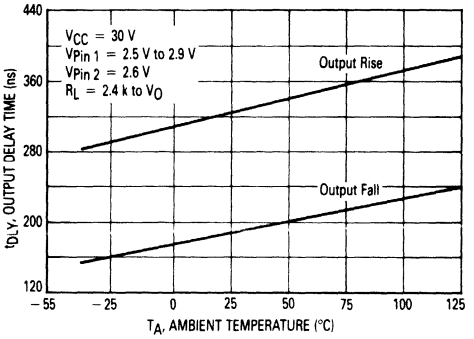


FIGURE 7 — COMPARATOR OUTPUT SATURATION versus SINK CURRENT

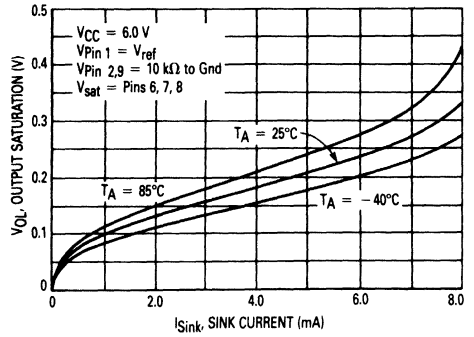
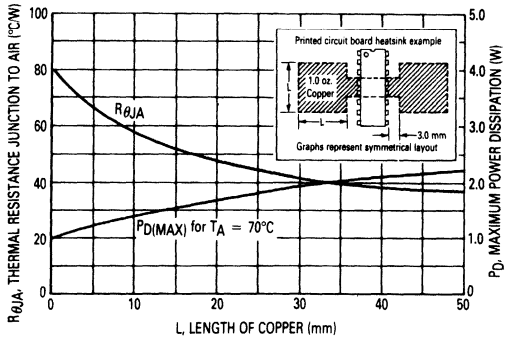


FIGURE 8 — THERMAL RESISTANCE AND MAXIMUM POWER DISSIPATION versus P.C.B. COPPER LENGTH



PIN FUNCTION DESCRIPTION

Pin No.	Function	Description
1	Comparator Inverting Input	This is the Uncommitted Comparator inverting input. It is typically connected to a resistor divider to monitor a voltage.
2	Comparator Noninverting Input	This is the Uncommitted Comparator noninverting input. It is typically connected to a reference voltage.
3	N.C.	No connection. This pin is not internally connected.
4,5,12,13	Gnd	These pins are the control circuit grounds and are connected to the source and load ground returns. They are part of the IC lead frame and can be used for heatsinking.
6	Comparator Output	This is the Uncommitted Comparator output. It is an open collector sink-only output requiring a pull-up resistor.
7	Reset	This is the Reset Comparator output. It is an open collector sink-only output requiring a pull-up resistor.
8	Power Warning	This is the Power Warning Comparator output. It is an open collector sink-only output requiring a pull-up resistor.
9	Power Sense	This is the Power Warning Comparator noninverting input. It is typically connected to a resistor divider to monitor the input power source voltage.
10	Hysteresis Adjust	The Power Warning Comparator hysteresis is programmed by a resistor connected from this pin to ground.
11	Regulator Output	This is the 5.0 V Regulator output.
14	V_{CC}	This pin is the positive supply input of the control IC.
15	Chip Disable	This input is used to switch the IC into a standby mode turning off all outputs.
16	V_{ref}	This is the 2.6 V Reference output. It is intended to be used in conjunction with the Power Warning and Uncommitted comparators.

OPERATING DESCRIPTION

The MC34160 Series is a monolithic voltage regulator and supervisory circuit containing many of the necessary monitoring functions required in microprocessor based systems. It is specifically designed for appliance and industrial applications, offering the designer a cost effective solution with minimal external components. These devices are specified for operation over an input voltage of 7.0 V to 40 V, and with a junction temperature of −40°C to +150°C. A typical microprocessor application is shown in Figure 9.

Regulator

The 5.0 V regulator is designed to source in excess of 100 mA output current and is short circuit protected. The output has a guaranteed tolerance of ±5.0% over line, load, and temperature. Internal thermal shutdown circuitry is included to limit the maximum junction temperature to a safe level. When activated, typically at 170°C, the regulator output turns off.

In specific situations a combination of input and output bypass capacitors may be required for regulator

stability. If the regulator is located an appreciable distance (≥4") from the supply filter, an input bypass capacitor (C_{in}) of 0.33 μF or greater is suggested. Output capacitance values of less than 5.0 nF may cause regulator instability at light load (≤1.0 mA) and cold temperature. An output bypass capacitor of 0.1 μF or greater is recommended to ensure stability under all load conditions. The capacitors selected must provide good high frequency characteristics.

Good construction techniques should be used to minimize ground loops and lead resistance drops since the regulator does not have external sense inputs.

Reference

The 2.6 V bandgap reference is short circuit protected and has a guaranteed output tolerance of ±5.0% over line, load, and temperature. It is intended to be used in conjunction with the Power Warning and Uncommitted Comparator. The reference can source in excess of 2.0 mA and sink a maximum of 10 μA. For additional current sinking capability, an external load resistor to ground must be used.

Reference biasing is internally derived from either V_{CC} or V_O, allowing proper operation if either drops below nominal.

Chip Disable

This input is used to switch the IC into a standby mode. When activated, internal biasing for the entire die is removed causing all outputs to turn off. This reduces the power supply current (I_{CC}) to less than 0.3 mA.

Comparators

Three separate comparators are incorporated for voltage monitoring. Their outputs can provide diagnostic information to the microprocessor, preventing system malfunctions.

The Reset comparator inverting input is internally connected to the 2.6 V reference while the noninverting input monitors V_O. The Reset output is active low when V_O falls approximately 180 mV below its regulated voltage. To prevent erratic operation when crossing the comparator threshold, 70 mV of hysteresis is provided.

The Power Warning comparator is typically used to detect an impending loss of system power. The inverting input is internally connected to the reference, fixing the threshold at 2.6 V. The input power source V_{in} is monitored by the noninverting input through the R_1/R_2 divider (Figure 9). This input features an adjustable 10 μA to 50 μA current sink I_H that is programmed by the value selected for resistor R_H. A default current of 6.5 μA is provided if R_H is omitted. When the comparator input falls below 2.6 V, the current sink is activated. This produces hysteresis if V_{in} is monitored through a series resistor (R_1). The comparator thresholds are defined as follows:

$$V_{th(lower)} = V_{ref}\left(1 + \frac{R_1}{R_2}\right) - I_{IB}\,R_1$$

$$V_{th(upper)} = V_{ref}\left(1 + \frac{R_1}{R_2}\right) + I_H\,R_1$$

The nominal hysteresis current I_H equals 1.2 V/R_H (Figure 4).

The Uncommitted Comparator can be used to synchronize the microprocessor with the ac line signal for timing functions, or for synchronous load switching. It can also be connected as a line loss detector as shown in Figure 10. The comparator contains 200 mV of hysteresis preventing erractic output behavior when crossing the input threshold.

The Power Warning and Uncommitted comparators each have a transistor base-emitter connected across their inputs. The base input normally connects to a voltage reference while the emitter input connects to the voltage to be monitored. The transistor limits the negative excursion on the emitter input to −0.7 V below the base input by supplying current from V_{CC}. This clamp current will prevent forward biasing the IC substrate. Zener diodes are connected to the comparator inputs to enhance the IC's electrostatic discharge capability. Resistors R_1 and R_{in} must limit the input current to a maximum of ±2.0 mA.

Each comparator output consists of an open collector NPN transistor capable of sinking 2.0 mA with a saturation voltage less than 0.4 V, and standing off 40 V with minimal leakage. Internal bias for the Reset and Power Warning comparators is derived from either V_{CC} or the regulator output to ensure functionality when either is below nominal.

Heat Tab Package

The MC34160 is contained in a 16 lead plastic dual-in-line package in which the die is mounted on a special Heat Tab copper alloy lead frame. This tab consists of the four center ground pins that are specifically designed to improve thermal conduction from the die to the surrounding air. The pictorial in Figure 8 shows a simple but effective method of utilizing the printed circuit board medium as a heat dissipator by soldering these tabs to an adequate area of copper foil. This permits the use of standard board layout and mounting practices while having the ability to more than halve the junction to air thermal resistance. The example and graph are for a symmetrical layout on a single sided board with one ounce per square foot copper.

FIGURE 9 — TYPICAL MICROPROCESSOR APPLICATION

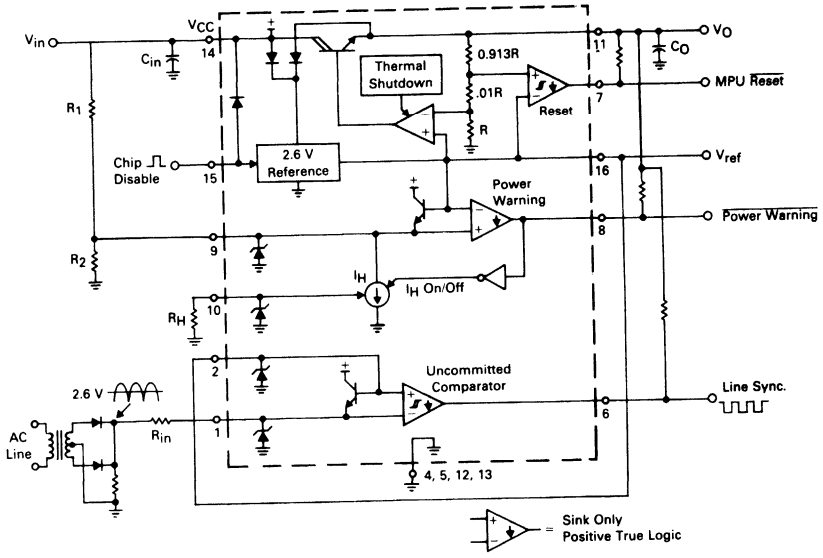
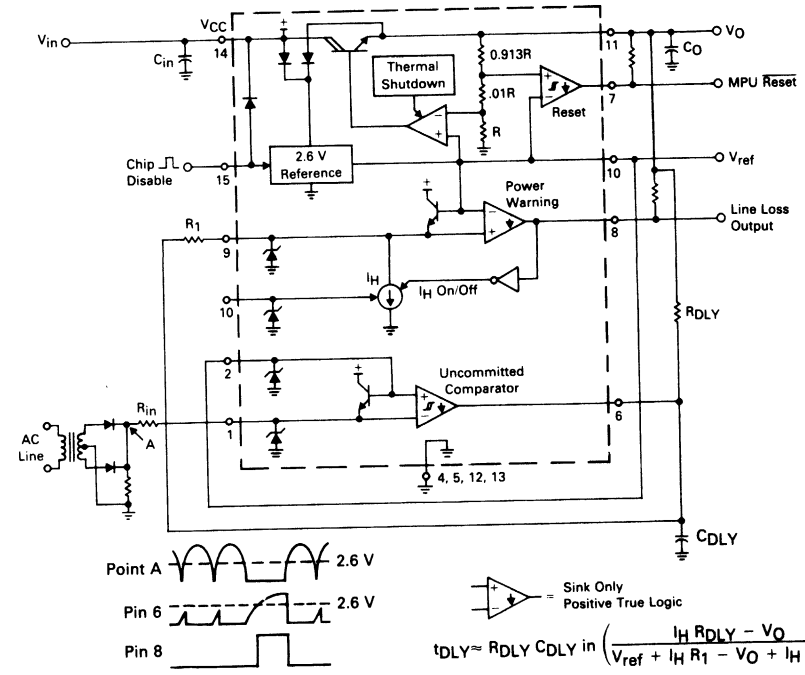
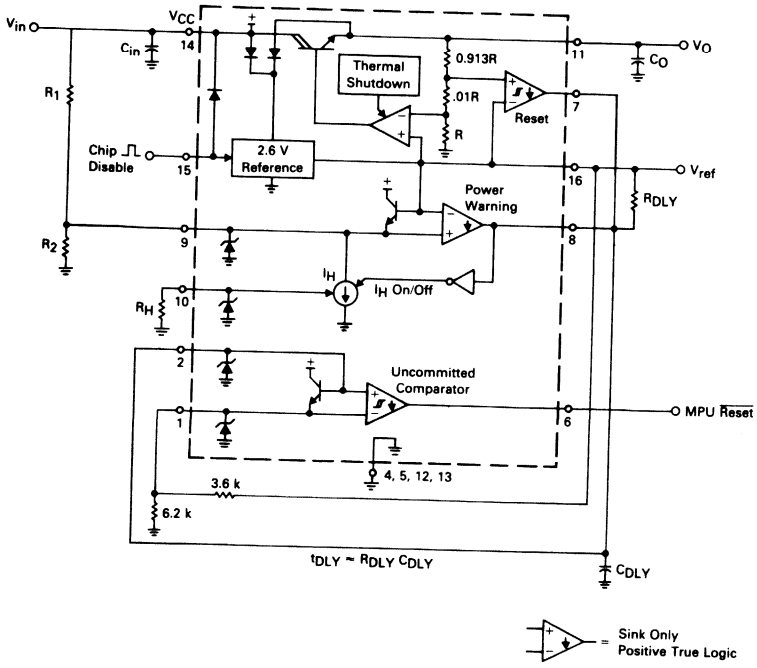


FIGURE 10 — LINE LOSS DETECTOR APPLICATION



$$t_{DLY} \approx R_{DLY}\, C_{DLY} \ln \left(\frac{I_H R_{DLY} - V_O}{V_{ref} + I_H R_1 - V_O + I_H R_{DLY}} \right)$$

FIGURE 11 — TIME DELAYED MICROPROCESSOR RESET



MOTOROLA

MC34163
MC33163

Product Preview

POWER SWITCHING REGULATOR

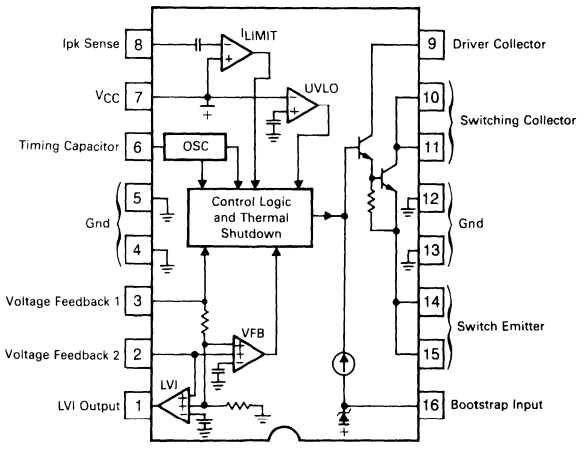
The MC34163 series are monolithic power switching regulators that contain the primary functions required for DC-to-DC converters. This series was specifically designed to be incorporated in Step-Up, Step-Down, and Voltage-Inverting applications with a minimum number of external components.

These devices consist of two high gain voltage feedback comparators, temperature compensated reference, programmable duty cycle oscillator, selectable synchronous output switching logic, driver with bootstrap capability for increased efficiency, and a high current output switch. Protective features consist of cycle-by-cycle current limiting, input undervoltage lockout, and internal thermal shutdown. Also included is a low voltage indicator output designed to interface with microprocessor based systems.

These devices are contained in a 16 pin dual-in-line heat tab plastic package for improved thermal conduction.

- Operation from 2.5 V to 40 V Input
- Low Standby Current
- Precision 2% Reference
- Programmable Duty Cycle Oscillator
- Selectable Synchronous Output Switching Logic
- Driver with Bootstrap Capability for Increased Efficiency
- Output Switch Current in Excess of 3.0 A
- Cycle-By-Cycle Current Limiting
- Input Undervoltage Lockout
- Internal Thermal Shutdown Protection
- Low Voltage Indicator Output for Direct Microprocessor Interface
- Heat Tab Power Package

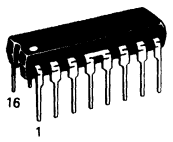
SIMPLIFIED BLOCK DIAGRAM



This document contains information on a product under development. Motorola reserves the right to change or discontinue this product without notice.

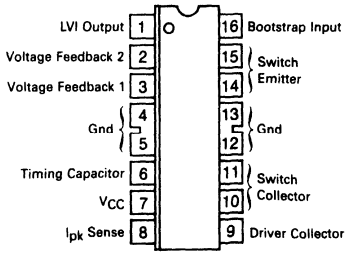
POWER SWITCHING REGULATOR

SILICON MONOLITHIC INTEGRATED CIRCUIT



P SUFFIX
PLASTIC PACKAGE
CASE 648C-02

PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

Device	Temperature Range	Package
MC34163P	0 to +70°C	16 Plastic DIP
MC33163P	−40 to +85°C	16 Plastic DIP

MOTOROLA

MC34164

Product Preview

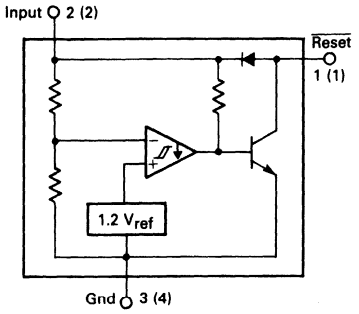
MICROPOWER UNDERVOLTAGE SENSING CIRCUIT

The MC34164 is an undervoltage sensing circuit specifically designed for use as a reset controller in portable microprocessor based systems where extended battery life is required. It offers the designer an economical solution for low voltage detection with a single external resistor. The MC34164 features a bandgap reference, a comparator with precise thresholds and built-in hysteresis to prevent erratic reset operation, an open collector reset output capable of sinking in excess of 7.0 mA, and guaranteed operation down to 1.0 volt input with extremely low standby current. These devices are packaged in 3-pin TO-92 and 8-pin surface mount packages.

Applications include direct monitoring of the 5.0 volt MPU/logic power supply used in appliance, automotive, consumer, and industrial equipment.

- Temperature Compensated Reference
- Comparator Threshold of 4.3 V at 25°C
- Precise Comparator Thresholds Guaranteed Over Temperature
- Comparator Hysteresis Prevents Erratic Reset
- Reset Output Capable of Sinking in Excess of 7.0 mA
- Internal Clamp Diode for Discharging Delay Capacitor
- Guaranteed Reset Operation with 1.0 Volt Input
- Extremely Low Standby Current of 10 μA
- Economical TO-92 and Surface Mount Packages

REPRESENTATIVE BLOCK DIAGRAM



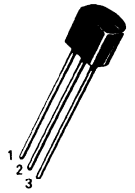
Pin numbers adjacent to terminals are for the 3 pin TO-92 package.
Pin numbers in parenthesis are for the D suffix SO-8 package.

This document contains information on a product under development. Motorola reserves the right to change or discontinue this product without notice.

MICROPOWER UNDERVOLTAGE SENSING CIRCUIT

SILICON MONOLITHIC INTEGRATED CIRCUIT

P SUFFIX
PLASTIC PACKAGE
CASE 29-04
TO-92



Pin 1. $\overline{\text{Reset}}$
2. Input
3. Ground

D SUFFIX
PLASTIC PACKAGE
CASE 751-03
SO-8

Pin 1. $\overline{\text{Reset}}$
2. Input
3. N.C.
4. Ground
5. N.C.
6. N.C.
7. N.C.
8. N.C.

ORDERING INFORMATION

Device	Temperature Range	Package
MC34164P-5	0°C to +70°C	Plastic TO-92
MC34164D-5		Plastic SO-8
MC33164P-5	−40°C to +85°C	Plastic TO-92
MC33164D-5		Plastic SO-8

MOTOROLA

MC34166
MC33166

Product Preview

POWER SWITCHING REGULATOR

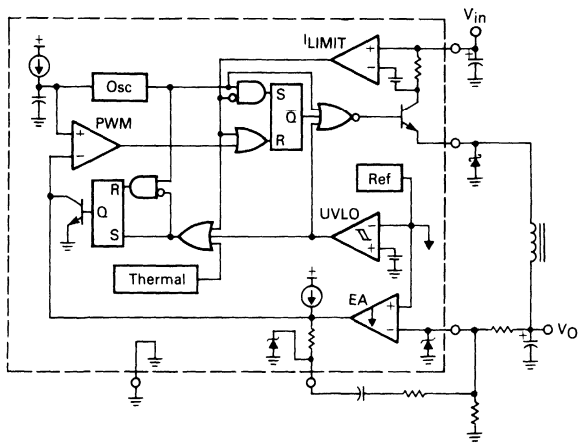
The MC34166, MC33166 series are high performance fixed frequency power switching regulators containing all the active functions required to implement standard DC-to-DC converter configurations. These devices feature an internal temperature compensated reference, fixed frequency oscillator with on-chip timing components, latching pulse width modulator for single pulse metering, high gain error amplifier, and a high current output switch.

Also included are protection features consisting of undervoltage lockout, cycle-by-cycle current limiting, and thermal shutdown.

This series was specifically designed to be incorporated in Step-Down and Voltage-Inverting configurations with a minimum number of external components and can also be used cost effectively in Step-Up applications.

- 8.0 V to 40 V Operation
- Output Switch Current in Excess of 3.0 A
- Fixed Frequency Oscillator with On-Chip Timing Components
- 5.05 V ±3.0% Reference
- High Gain Error Amplifier
- 0% to 95% Output Duty Cycle
- Cycle-By-Cycle Current Limiting
- Undervoltage Lockout with Hysteresis
- Internal Thermal Shutdown

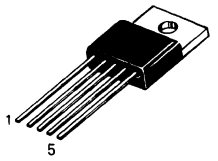
SIMPLIFIED BLOCK DIAGRAM



This document contains information on a product under development. Motorola reserves the right to change or discontinue this product without notice.

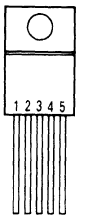
POWER SWITCHING REGULATOR

SILICON MONOLITHIC INTEGRATED CIRCUIT



T SUFFIX
PLASTIC PACKAGE
CASE 314D-02
(5 LEAD TO-220 TYPE)

PIN CONNECTIONS



Pin 1. Voltage Feedback Input
2. Switch Output
3. Ground
4. Input Voltage
5. Compensation

(Heatsink surface connected to Pin 3)

ORDERING INFORMATION

Device	Temperature Range	Package
MC34166T	0 to +70°C	Plastic Power
MC33166T	−40 to +85°C	Plastic Power

MOTOROLA

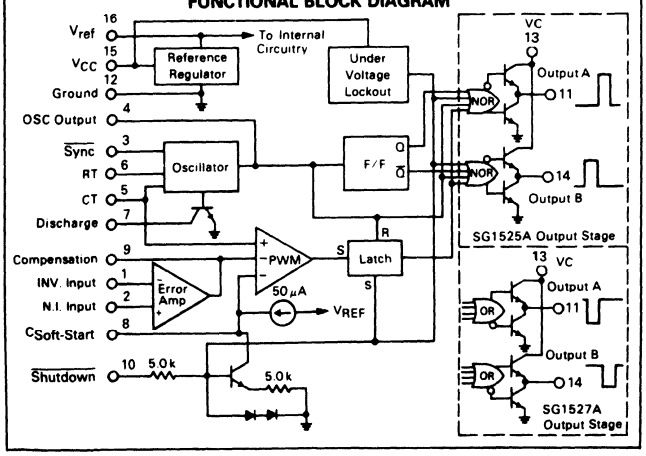
SG1525A/SG1527A
SG2525A/SG2527A
SG3525A/SG3527A

PULSE WIDTH MODULATOR CONTROL CIRCUITS

The SG1525A/1527A series of pulse width modulator control-circuits offer improved performance and lower external parts count when implemented for controlling all types of switching power supplies. The on-chip +5.1 volt reference is trimmed to ±1% and the error amplifier has an input common-mode voltage range that includes the reference voltage, thus eliminating the need for external divider resistors. A sync input to the oscillator enables multiple units to be slaved or a single unit to be synchronized to an external system clock. A wide range of dead time can be programmed by a single resistor connected between the C_T and Discharge pins. These devices also feature built-in soft-start circuitry, requiring only an external timing capacitor. A shutdown pin controls both the soft-start circuitry and the output stages, providing instantaneous turn off through the PWM latch with pulsed shutdown, as well as soft-start recycle with longer shutdown commands. The under voltage lockout inhibits the outputs and the changing of the soft-start capacitor when V_{CC} is below nominal. The output stages are totem-pole design capable of sinking and sourcing in excess of 200 mA. The output stage of the SG1525A series features NOR Logic resulting in a low output for an off state while the SG1527A series utilizes OR Logic which gives a high output when off. The devices are available in Military, Industrial and Commercial temperature ranges.

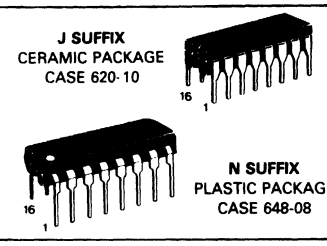
- 8.0 to 35 Volt Operation
- 5.1 Volt ± 1.0% Trimmed Reference
- 100 Hz to 400 kHz Oscillator Range
- Separate Oscillator Sync Pin
- Adjustable Dead Time Control
- Input Undervoltage Lockout
- Latching PWM to Prevent Multiple Pulses
- Pulse-by-Pulse Shutdown
- Dual Source/Sink Outputs: ± 400 mA Peak

FUNCTIONAL BLOCK DIAGRAM

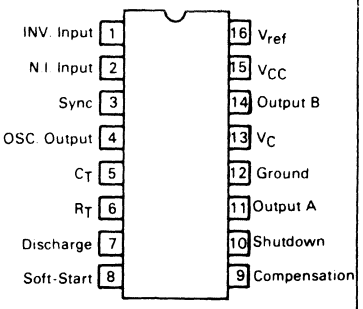


PULSE WIDTH MODULATOR CONTROL CIRCUITS

SILICON MONOLITHIC INTEGRATED CIRCUITS



PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

Device	Temperature Range	Package
SG1525AJ	−55 to +125°C	Ceramic DIP
SG1527AJ	−55 to +125°C	Ceramic DIP
SG2525AJ	−25 to +85°C	Ceramic DIP
SG2525AN	−25 to +85°C	Plastic DIP
SG2527AJ	−25 to +85°C	Ceramic DIP
SG2527AN	−25 to +85°C	Plastic DIP
SG3525AJ	0 to +70°C	Ceramic DIP
SG3525AN	0 to +70°C	Plastic DIP
SG3527AJ	0 to +70°C	Ceramic DIP
SG3527AN	0 to +70°C	Plastic DIP

MAXIMUM RATINGS (Note 1)

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	+40	Vdc
Collector Supply Voltage	V_C	+40	Vdc
Logic Inputs	—	-0.3 to +5.5	V
Analog Inputs	—	-0.3 to V_{CC}	V
Output Current, Source or Sink	I_O	±500	mA
Reference Output Current	I_{ref}	50	mA
Oscillator Charging Current	—	5.0	mA
Power Dissipation (Plastic & Ceramic Package) T_A = +25°C (Note 2) T_C = +25°C (Note 3)	P_D	 1000 2000	mW
Thermal Resistance Junction to Air Plastic and Ceramic Package	$R_{\theta JA}$	100	°C/W
Thermal Resistance Junction to Case Plastic and Ceramic Package	$R_{\theta JC}$	60	°C/W
Operating Junction Temperature	T_J	+150	°C
Storage Temperature Range Ceramic Package Plastic Package	T_{stg}	-65 to +150 -55 to +125	°C
Lead Temperature (Soldering, 10 Seconds)	T_{Solder}	+300	°C

NOTES:
1. Values beyond which damage may occur
2. Derate at 10 mW/°C for ambient temperatures above +50°C
3. Derate at 16 mW/°C for case temperatures above +25°C

RECOMMENDED OPERATING CONDITIONS

Characteristic	Symbol	Min.	Max.	Unit
Supply Voltage	V_{CC}	+8.0	+35	Vdc
Collector Supply Voltage	V_C	+4.5	+35	Vdc
Output Sink/Source Current (Steady State) (Peak)	I_O	 0 0	 ±100 ±400	mA
Reference Load Current	I_{ref}	0	20	mA
Oscillator Frequency Range	f_{osc}	0.1	400	kHz
Oscillator Timing Resistor	R_T	2.0	150	kΩ
Oscillator Timing Capacitor	C_T	0.001	0.2	μF
Deadtime Resistor Range	R_D	0	500	Ω
Operating Ambient Temperature Range SG1525A, SG1527A SG2525A, SG2527A SG3525A, SG3527A	T_A	 -55 -25 0	 +125 +85 +70	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = +20 Vdc, T_A = T_{low} to T_{high} [Note 4], unless otherwise specified)

Characteristic	Symbol	SG1525A/2525A SG1527A/2527A Min	Typ	Max	SG3525A SG3527A Min	Typ	Max	Unit
REFERENCE SECTION								
Reference Output Voltage (T_J = +25°C)	V_{ref}	5.05	5.10	5.15	5.00	5.10	5.20	Vdc
Line Regulation (+8.0 V ≤ V_{CC} ≤ +35 V)	Reg_{line}	—	10	20	—	10	20	mV
Load Regulation (0 mA ≤ I_L ≤ 20 mA)	Reg_{load}	—	20	50	—	20	50	mV
Temperature Stability	$\Delta V_{ref}/\Delta T$	—	20	—	—	20	—	mV
Total Output Variation Includes Line and Load Regulation over Temperature	ΔV_{ref}	5.00	—	5.20	4.95	—	5.25	Vdc
Short Circuit Current (V_{ref} = 0 V, T_J = +25°C)	I_{SC}	—	80	100	—	80	100	mA
Output Noise Voltage (10 Hz ≤ f ≤ 10 kHz, T_J = +25°C)	V_n	—	40	200	—	40	200	μV_{rms}
Long Term Stability (T_J = +125°C) (Note 5)	S	—	20	50	—	20	50	mV/khr
OSCILLATOR SECTION (Note 6, unless otherwise specified)								
Initial Accuracy (T_J = +25°C)	—	—	±2.0	±6.0	—	±2.0	±6.0	%
Frequency Stability with Voltage (+8.0 V ≤ V_{CC} ≤ +35 V)	$\frac{\Delta f_{osc}}{\Delta V_{CC}}$	—	±0.3	±1.0	—	±1.0	±2.0	%
Frequency Stability with Temperature	$\frac{\Delta f_{osc}}{\Delta T}$	—	±3.0	—	—	±3.0	—	%
Minimum Frequency (R_T = 150 kΩ, C_T = 0.2 μF)	f_{min}	—	50	—	—	50	—	Hz
Maximum Frequency (R_T = 2.0 kΩ, C_T = 1.0 nF)	f_{max}	400	—	—	400	—	—	kHz
Current Mirror (I_{R_T} = 2.0 mA)	—	1.7	2.0	2.2	1.7	2.0	2.2	mA
Clock Amplitude	—	3.0	3.5	—	3.0	3.5	—	V
Clock Width (T_J = +25°C)	—	0.3	0.5	1.0	0.3	0.5	1.0	μs
Sync Threshold	—	1.2	2.0	2.8	1.2	2.0	2.8	V
Sync Input Current (Sync Voltage = +3.5 V)	—	—	1.0	2.5	—	1.0	2.5	mA
ERROR AMPLIFIER SECTION (V_{CM} = +5.1 V)								
Input Offset Voltage	V_{IO}	—	0.5	5.0	—	2.0	10	mV
Input Bias Current	I_{IB}	—	1.0	10	—	1.0	10	μA
Input Offset Current	I_{IO}	—	—	1.0	—	—	1.0	μA
DC Open Loop Gain (R_L ≥ 10 MΩ)	A_{VOL}	60	75	—	60	75	—	dB
Low Level Output Voltage	V_{OL}	—	0.2	0.5	—	0.2	0.5	V
High Level Output Voltage	V_{OH}	3.8	5.6	—	3.8	5.6	—	V
Common Mode Rejection Ratio (+1.5 V ≤ V_{CM} ≤ +5.2 V)	CMRR	60	75	—	60.	75	—	dB
Power Supply Rejection Ratio (+8.0 V ≤ V_{CC} ≤ +35 V)	PSRR	50	60	—	50	60	—	dB
PWM COMPARATOR SECTION								
Minimum Duty Cycle	DC_{min}	—	—	0	—	—	0	%
Maximum Duty Cycle	DC_{max}	45	49	—	45	49	—	%
Input Threshold, Zero Duty Cycle (Note 6)	V_{TH}	0.6	0.9	—	0.6	0.9	—	V
Input Threshold, Maximum Duty Cycle (Note 6)	V_{TH}	—	3.3	3.6	—	3.3	3.6	V
Input Bias Current	I_{IB}	—	0.05	1.0	—	0.05	1.0	μA

ELECTRICAL CHARACTERISTICS (Continued)

Characteristic	Symbol	SG1525A/2525A SG1527A/2527A			SG3525A SG3527A			Unit
		Min	Typ	Max	Min	Typ	Max	
SOFT-START SECTION								
Soft-Start Current ($V_{shutdown}$ = 0 V)	—	25	50	80	25	50	80	μA
Soft-Start Voltage ($V_{shutdown}$ = 2.0 V)	—	—	0.4	0.6	—	0.4	0.6	V
Shutdown Input Current ($V_{shutdown}$ = 2.5 V)	—	—	0.4	1.0	—	0.4	1.0	mA
OUTPUT DRIVERS (Each Output, V_{CC} = +20 V)								
Output Low Level	V_{OL}							V
(I_{sink} = 20 mA)		—	0.2	0.4	—	0.2	0.4	
(I_{sink} = 100 mA)		—	1.0	2.0	—	1.0	2.0	
Output High Level	V_{OH}							V
(I_{source} = 20 mA)		18	19	—	18	19	—	
(I_{source} = 100 mA)		17	18	—	17	18	—	
Under Voltage Lockout (V8 and V9 = High)	V_{UL}	6.0	7.0	8.0	6.0	7.0	8.0	V
Collector Leakage, V_C = +35 V (Note 7)	$I_{C(leak)}$	—	—	200	—	—	200	μA
Rise Time (C_L = 1.0 nF, T_J = 25°C)	t_r	—	100	600	—	100	600	ns
Fall Time (C_L = 1.0 nF, T_J = 25°C)	t_f	—	50	300	—	50	300	ns
Shutdown Delay (V_{SD} = +3.0 V, C_S = 0, T_J = +25°C)	t_{ds}	—	0.2	0.5	—	0.2	0.5	μs
Supply Current, (V_{CC} = +35 V)	I_{CC}	—	14	20	—	14	20	mA

NOTES:

4. T_{low} = −55°C for SG1525A/1527A
   −25°C for SG2525A/2527A
   0°C for SG3525A/3527A
   T_{high} = +125°C for SG1525A/1527A
   +85°C for SG2525A/2527A
   +70°C for SG3525A/3527A
5. Since long term stability cannot be measured on each device before shipment, this specification is an engineering estimate of average stability from lot to lot.
6. Tested at f_{osc} = 40 kHz (R_T = 3.6 kΩ, C_T = 0.01 μF, R_D = 0 Ω).
7. Applies to SG1525A/2525A/3525A only, due to polarity of output pulses.

APPLICATION INFORMATION

SHUTDOWN OPTIONS
(See Block Diagram, front page)

Since both the compensation and soft-start terminals (Pins 9 and 8) have current source pull-ups, either can readily accept a pull-down signal which only has to sink a maximum of 100 μA to turn off the outputs. This is subject to the added requirement of discharging whatever external capacitance may be attached to these pins.

An alternate approach is the use of the shutdown circuitry of Pin 10 which has been improved to enhance the available shutdown options. Activating this circuit by applying a positive signal on Pin 10 performs two functions: the PWM latch is immediately set providing the fastest turn-off signal to the outputs; and a 150 μA current sink begins to discharge the external soft-start capacitor. If the shutdown command is short, the PWM signal is terminated without significant discharge of the soft-start capacitor, thus, allowing, for example, a convenient implementation of pulse-by-pulse current limiting. Holding Pin 10 high for a longer duration, however, will ultimately discharge this external capacitor, recycling slow turn-on upon release.

Pin 10 should not be left floating as noise pickup could conceivably interrupt normal operation.

TYPICAL CHARACTERISTICS

FIGURE 1 — SG1525A OSCILLATOR SCHEMATIC

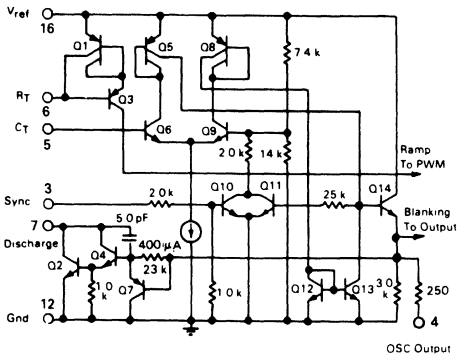


FIGURE 2 — OSCILLATOR CHARGE TIME versus R_T

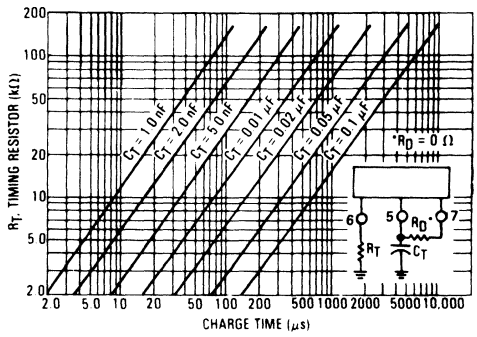


FIGURE 3 — OSCILLATOR DISCHARGE TIME versus R_D

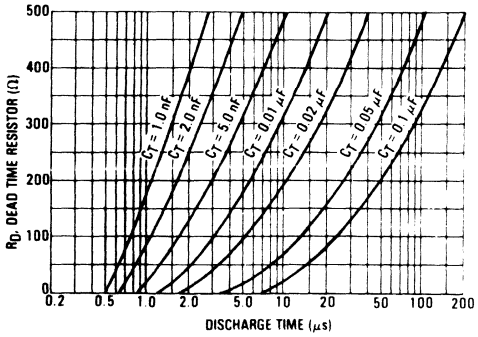


FIGURE 4 — SG1525A ERROR AMPLIFIER SCHEMATIC

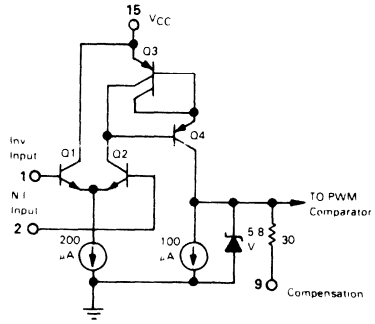


FIGURE 5 — ERROR AMPLIFIER OPEN-LOOP FREQUENCY RESPONSE

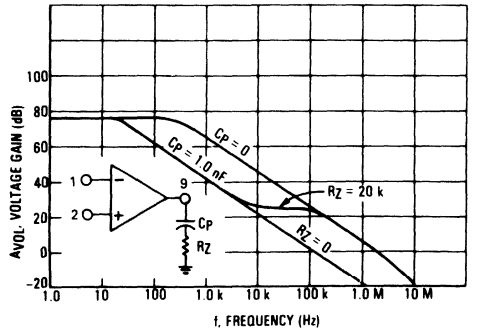


FIGURE 6 — SG1525A OUTPUT CIRCUIT (1/2 CIRCUIT SHOWN)

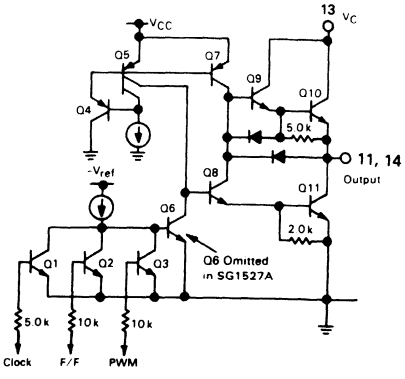


FIGURE 7 — SG1525A/2525A/3525A
OUTPUT SATURATION CHARACTERISTICS

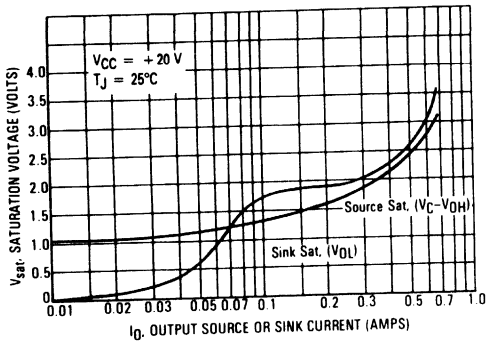
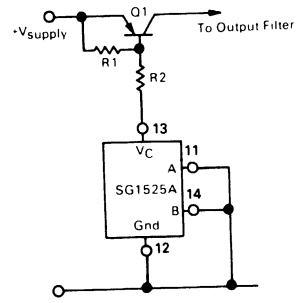
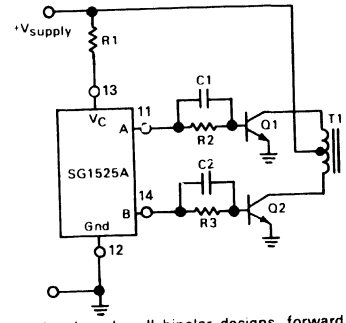


FIGURE 8 — SINGLE ENDED SUPPLY



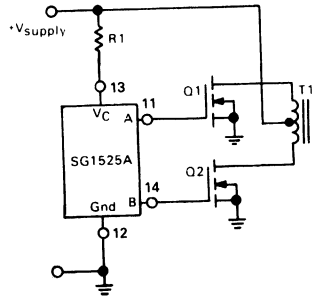
For single-ended supplies, the driver outputs are grounded. The V_C terminal is switched to ground by the totem-pole source transistors on alternate oscillator cycles.

FIGURE 9 — PUSH-PULL CONFIGURATION



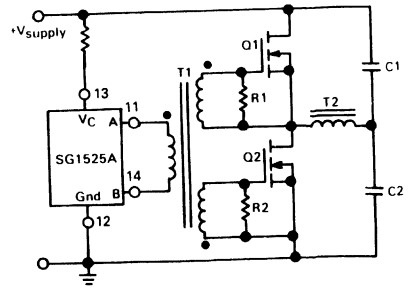
In conventional push-pull bipolar designs, forward base drive is controlled by R1-R3. Rapid turn-off times for the power devices are achieved with speed-up capacitors C1 and C2.

FIGURE 10 — DRIVING POWER FETS



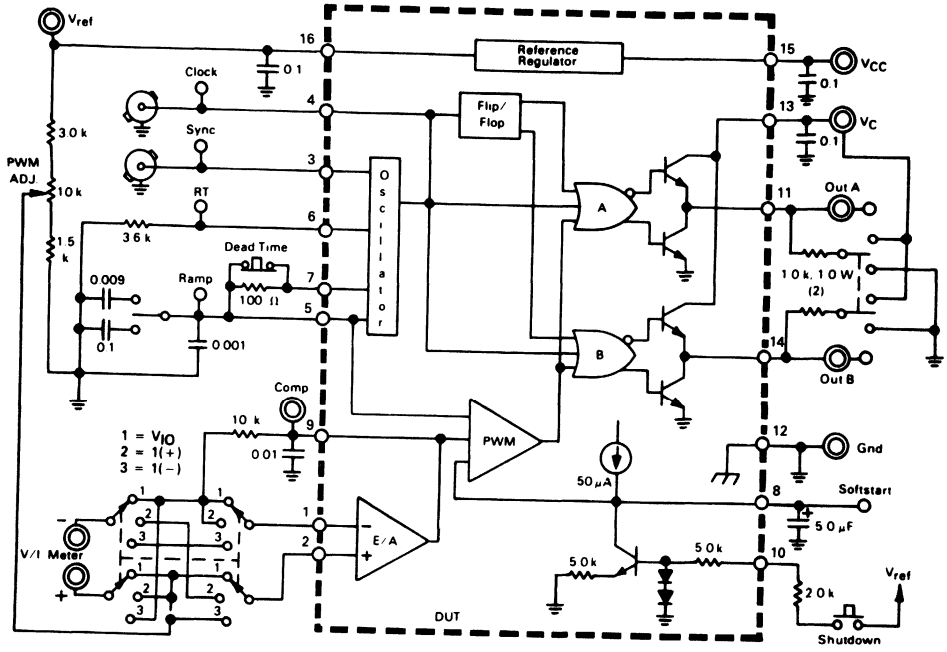
The low source impedance of the output drivers provides rapid charging of power FET input capacitance while minimizing external components.

FIGURE 11 — DRIVING TRANSFORMERS IN A HALF-BRIDGE CONFIGURATION



Low power transformers can be driven directly by the SG1525A. Automatic reset occurs during deadtime, when both ends of the primary winding are switched to ground.

FIGURE 12 — LAB TEST FIXTURE



MOTOROLA

SG1526
SG2526
SG3526

PULSE WIDTH MODULATION CONTROL CIRCUIT

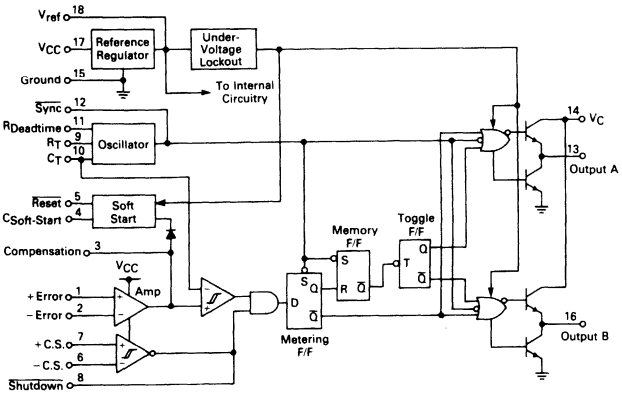
The SG1526 is a high performance pulse width modulator integrated circuit intended for fixed frequency switching regulators and other power control applications.

Functions included in this IC are a temperature compensated voltage reference, sawtooth oscillator, error amplifier, pulse width modulator, pulse metering and steering logic, and two high current totem pole outputs ideally suited for driving the capacitance of power FETs at high speeds.

Additional protective features include soft start and undervoltage lockout, digital current limiting, double pulse inhibit, adjustable dead time and a data latch for single pulse metering. All digital control ports are TTL and B-series CMOS compatible. Active low logic design allows easy wired-OR connections for maximum flexibility. The versatility of this device enables implementation in single-ended or push-pull switching regulators that are transformerless or transformer coupled. The SG1526 is specified over the full military junction temperature range of -55°C to +150°C. The SG2526 is specified over a junction temperature range of -40°C to +150°C while the SG3526 is specified over a range of 0°C to +125°C.

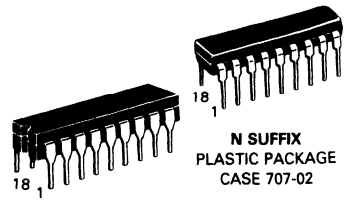
- 8.0 to 35 Volt Operation
- 5.0 Volt ±1% Trimmed Reference
- 1.0 Hz to 400 kHz Oscillator Range
- Dual Source/Sink Current Outputs: ±100 mA
- Digital Current Limiting
- Programmable Dead Time
- Undervoltage Lockout
- Single Pulse Metering
- Programmable Soft Start
- Wide Current Limit Common Mode Range
- Guaranteed 6 Unit Synchronization

BLOCK DIAGRAM



PULSE WIDTH MODULATION CONTROL CIRCUITS

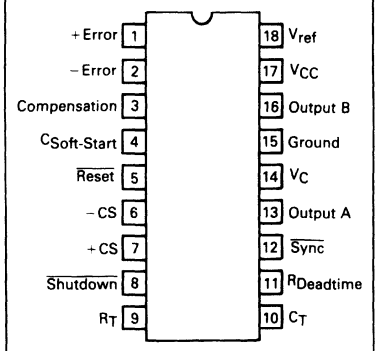
SILICON MONOLITHIC INTEGRATED CIRCUITS



N SUFFIX
PLASTIC PACKAGE
CASE 707-02

J SUFFIX
CERAMIC PACKAGE
CASE 726-04

PIN CONNECTIONS



Top View

ORDERING INFORMATION

Device	Junction Temperature Range	Package
SG1526J	-55 to +150°C	Ceramic DIP
SG2526J SG2526N	-40 to +150°C	Ceramic DIP Plastic DIP
SG3526J SG3526N	0 to +125°C	Ceramic DIP Plastic DIP

MAXIMUM RATINGS (Note 1)

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	+40	Vdc
Collector Supply Voltage	V_C	+40	Vdc
Logic Inputs	—	-0.3 to +5.5	V
Analog Inputs	—	-0.3 to V_{CC}	V
Output Current, Source or Sink	I_O	±200	mA
Reference Load Current (V_{CC} = 40 V, Note 2)	I_{ref}	50	mA
Logic Sink Current	—	15	mA
Power Dissipation (Plastic and Ceramic Package) (Note 3) T_A = +25°C (Note 4) T_C = +25°C	P_D	 1000 3000	mW
Thermal Resistance Junction to Air (Plastic and Ceramic Package)	$R_{\theta JA}$	100	°C/W
Thermal Resistance Junction to Case (Plastic and Ceramic Package)	$R_{\theta JC}$	42	°C/W
Operating Junction Temperature	T_J	+150	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C
Lead Temperature (Soldering, 10 Seconds)	T_{Solder}	±300	°C

Notes:
1. Values beyond which damage may occur
2. Maximum junction temperature must be observed.
3. Derate at 10 mW/°C for ambient temperatures above + 50°C
4. Derate at 24 mW/°C for case temperatures above + 25°C

RECOMMENDED OPERATING CONDITIONS

Characteristic	Symbol	Min	Max	Unit
Supply Voltage	V_{CC}	+8.0	+35	Vdc
Collector Supply Voltage	V_C	+4.5	+35	Vdc
Output Sink/Source Current (Each Output)	I_O	0	±100	mA
Reference Load Current	I_{ref}	0	20	mA
Oscillator Frequency Range	f_{osc}	0.001	400	kHz
Oscillator Timing Resistor	R_T	2.0	150	kΩ
Oscillator Timing Capacitor	C_T	0.001	20	μF
Available Deadtime Range (40 kHz)		3.0	50	%
Operating Junction Temperature Range SG1526 SG2526 SG3526	T_J	 -55 -40 0	 +150 +150 +125	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = +15 Vdc, T_J = T_{low} to T_{high} [Note 5] unless otherwise specified)

Characteristic	Symbol	SG1526/2526			SG3526			Unit
		Min	Typ	Max	Min	Typ	Max	
REFERENCE SECTION (Note 6)								
Reference Output Voltage (T_J = +25°C)	V_{ref}	4.95	5.00	5.05	4.90	5.00	5.10	V
Line Regulation (+8.0 V ≤ V_{CC} ≤ +35 V)	Reg_{line}	—	10	20	—	10	30	mV
Load Regulation, 0 mA ≤ I_L ≤ 20 mA	Reg_{load}	—	10	30	—	10	50	mV
Temperature Stability	$\Delta V_{ref}/\Delta T_J$	—	15	—	—	10	—	mV
Total Reference Output Voltage Variation (+8.0 V ≤ V_{CC} ≤ +35 V, 0 mA ≤ I_L ≤ 20 mA)	ΔV_{ref}	4.90	5.00	5.10	4.85	5.00	5.15	V
Short Circuit Current (V_{ref} = 0 V, Note 2)	I_{SC}	25	80	125	25	80	125	mA
UNDERVOLTAGE LOCKOUT								
$\overline{\text{Reset}}$ Output Voltage (V_{ref} = +3.8 V)	—	—	0.2	0.4	—	0.2	0.4	V
$\overline{\text{Reset}}$ Output Voltage (V_{ref} = +4.8 V)	—	2.4	4.8	—	2.4	4.8	—	V
OSCILLATOR SECTION (Note 7)								
Initial Accuracy (T_J = +25°C)	—	—	±3.0	±8.0	—	±3.0	±8.0	%
Frequency Stability over Power Supply Range (+8.0 V ≤ V_{CC} ≤ +35 V)	$\frac{\Delta f_{osc}}{\Delta V_{CC}}$	—	0.5	1.0	—	0.5	1.0	%
Frequency Stability over Temperature (ΔT_J = T_{low} to T_{high})	$\frac{\Delta f_{osc}}{\Delta T_J}$	—	4.0	—	—	2.0	—	%
Minimum Frequency (R_T = 150 kΩ, C_T = 20 μF)	f_{min}	—	0.5	—	—	0.5	—	Hz
Maximum Frequency (R_T = 2.0 kΩ, C_T = 0.001 μF)	f_{max}	400	—	—	400	—	—	kHz
Sawtooth Peak Voltage (V_{CC} = +35 V)	$V_{osc(P)}$	—	3.0	3.5	—	3.0	3.5	V
Sawtooth Valley Voltage (V_{CC} = +8.0 V)	$V_{osc(V)}$	0.45	0.8	—	0.45	0.8	—	V
ERROR AMPLIFIER SECTION (Note 8)								
Input Offset Voltage (R_S ≤ 2.0 kΩ)	V_{IO}	—	2.0	5.0	—	2.0	10	mV
Input Bias Current	I_{IB}	—	−350	−1000	—	−350	−2000	nA
Input Offset Current	I_{IO}	—	35	100	—	35	200	nA
DC Open Loop Gain (R_L ≥ 10 MΩ)	A_{Vol}	64	72	—	60	72	—	dB
High Output Voltage ($V_{Pin\ 1}$-$V_{Pin\ 2}$ ≥ +150 mV, I_{source} = 100 μA)	V_{OH}	3.6	4.2	—	3.6	4.2	—	V
Low Output Voltage ($V_{Pin\ 2}$-$V_{Pin\ 1}$ ≥ +150 mV, I_{sink} = 100 μA)	V_{OL}	—	0.2	0.4	—	0.2	0.4	V
Common Mode Rejection Ratio (R_S ≤ 2.0 kΩ)	CMRR	70	94	—	70	94	—	dB
Power Supply Rejection Ratio (+12 V ≤ V_{CC} ≤ +18 V)	PSRR	66	80	—	66	80	—	dB

Notes:
5. T_{low} = −55°C for SG1526
   −40°C for SG2526
   0°C for SG3526
   T_{high} = +150°C for SG1526/2526
   +125°C for SG3526
6. I_L = 0 mA unless otherwise noted.
7. f_{osc} = 40 kHz (R_T = 4.12 kΩ ±1%, C_T = 0.01 μF ±1%, R_D = 0 Ω)
8. 0 V ≤ V_{CM} ≤ +5.2 V

ELECTRICAL CHARACTERISTICS (Continued)

Characteristic	Symbol	SG1526/2526			SG3526			Unit
		Min	Typ	Max	Min	Typ	Max	
PWM COMPARATOR SECTION (Note 7)								
Minimum Duty Cycle ($V_{compensation}$ = +0.4 V)	DC_{min}	—	—	0	—	—	0	%
Maximum Duty Cycle ($V_{compensation}$ = +3.6 V)	DC_{max}	45	49	—	45	49	—	%
DIGITAL PORTS (SYNC, SHUTDOWN, RESET)								
Output Voltage — High Logic Level (I_{source} = 40 μA)	V_{OH}	2.4	4.0	—	2.4	4.0	—	V
Output Voltage — Low Logic Level (I_{sink} = 3.6 mA)	V_{OL}	—	0.2	0.4	—	0.2	0.4	V
Input Current — High Logic Level (V_{IH} = +2.4 V)	I_{IH}	—	-125	-200	—	-125	-200	μA
Input Current — Low Logic Level (V_{IL} = +0.4 V)	I_{IL}	—	-225	-360	—	-225	-360	μA
CURRENT LIMIT COMPARATOR SECTION (Note 9)								
Sense Voltage ($R_S \leq 50\ \Omega$)	V_{sense}	90	100	110	80	100	120	mV
Input Bias Current	I_{IB}	—	-3.0	-10	—	-3.0	-10	μA
SOFT-START SECTION								
Error Clamp Voltage ($\overline{Reset}$ = +0.4 V)	—	—	0.1	0.4	—	0.1	0.4	V
Soft-Start Charging Current ($\overline{Reset}$ = +2.4 V)	I_{CS}	50	100	150	50	100	150	μA
OUTPUT DRIVERS (Each Output, V_C = +15 Vdc unless otherwise specified)								
Output High Level	V_{OH}							V
I_{source} = 20 mA		12.5	13.5	—	12.5	13.5	—	
I_{source} = 100 mA		12	13	—	12	13	—	
Output Low Level	V_{OL}							V
I_{sink} = 20 mA		—	0.2	0.3	—	0.2	0.3	
I_{sink} = 100 mA		—	1.2	2.0	—	1.2	2.0	
Collector Leakage, V_C = +40 V	$I_{C(leak)}$	—	50	150	—	50	150	μA
Rise Time (C_L = 1000 pF)	t_r	—	0.3	0.6	—	0.3	0.6	μs
Fall Time (C_L = 1000 pF)	t_f	—	0.1	0.2	—	0.1	0.2	μs
Supply Current ($\overline{Shutdown}$ = +0.4 V, V_{CC} = +35 V, R_T = 4.12 kΩ)	I_{CC}	—	18	30	—	18	30	mA

7. f_{osc} = 40 kHz (R_T = 4.12 kΩ ± 1%, C_T = 0.01 μF ± 1%, R_D = 0 Ω)
8. 0 V ≤ V_{CM} ≤ +5.2 V
9. 0 V ≤ V_{CM} ≤ +12 V

TYPICAL CHARACTERISTICS

FIGURE 1 — SG1526 REFERENCE STABILITY OVER TEMPERATURE

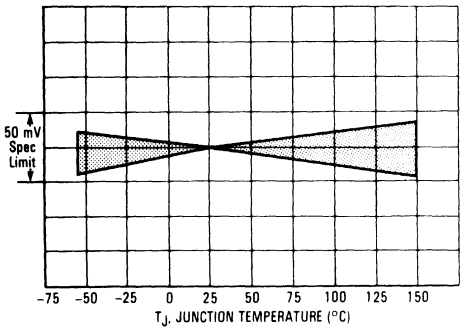


FIGURE 2 — REFERENCE VOLTAGE AS A FUNCTION SUPPLY VOLTAGE

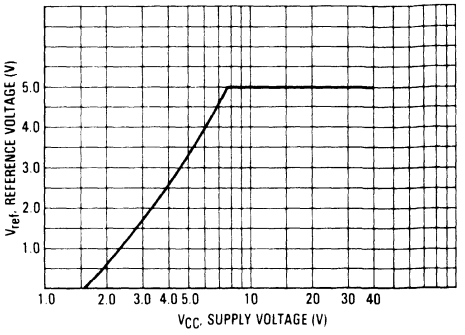


FIGURE 3 — ERROR AMPLIFIER OPEN LOOP FREQUENCY RESPONSE

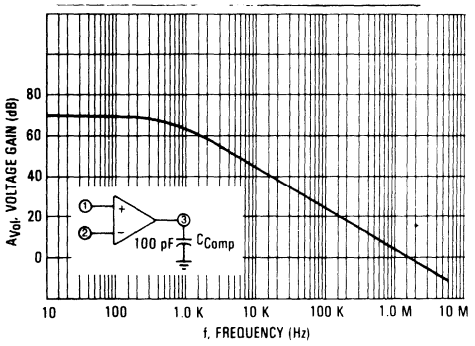


FIGURE 4 — CURRENT LIMIT COMPARATOR THRESHOLD

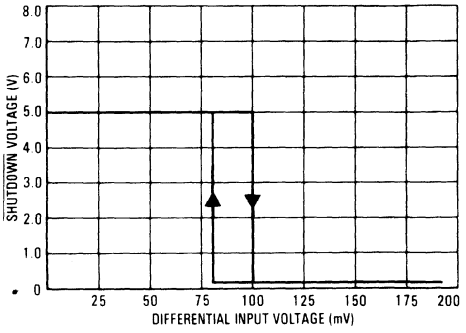


FIGURE 5 — UNDERVOLTAGE LOCKOUT CHARACTERISTIC

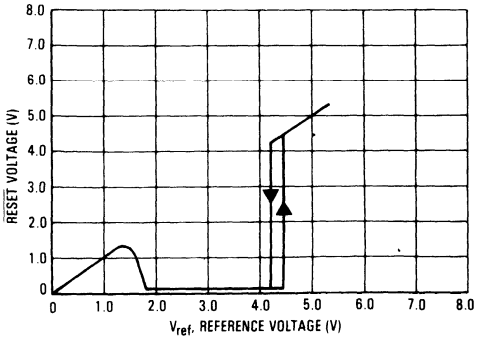


FIGURE 6 — OUTPUT DRIVER SATURATION VOLTAGE AS A FUNCTION OF SINK CURRENT

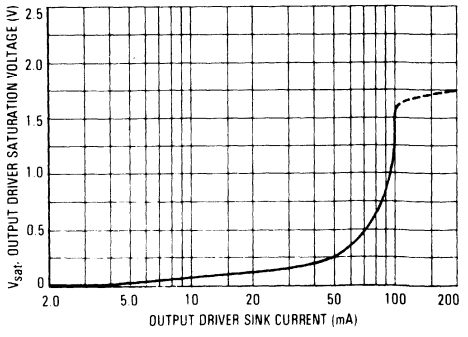


FIGURE 7 — V_C SATURATION VOLTAGE AS A FUNCTION OF SINK CURRENT

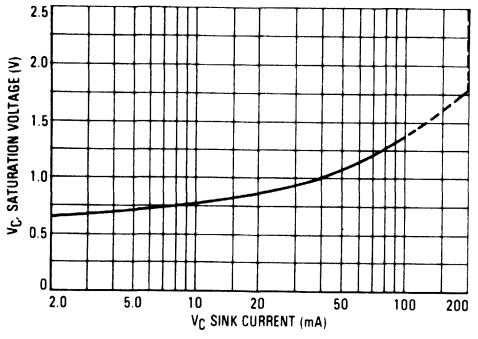


FIGURE 8 — SG1526 OSCILLATOR PERIOD

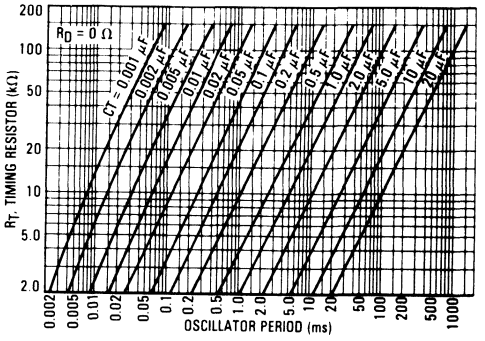


FIGURE 9 — SG1526 ERROR AMPLIFIER

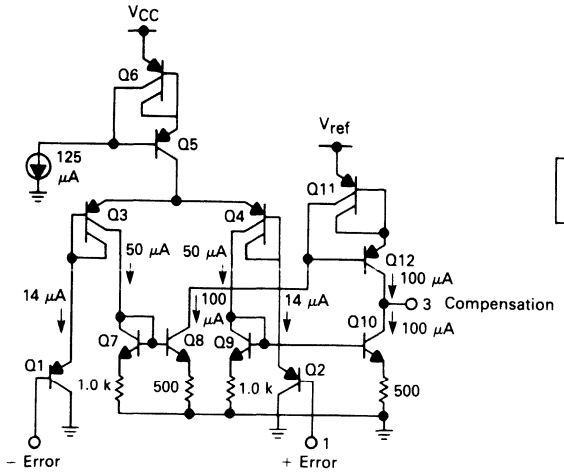


FIGURE 10 — SG1526 UNDERVOLTAGE LOCKOUT

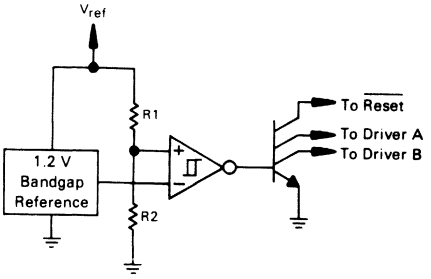
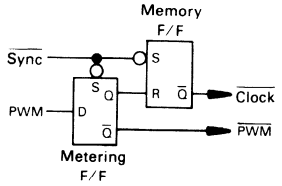


FIGURE 11 — SG1526 PULSE PROCESSING LOGIC

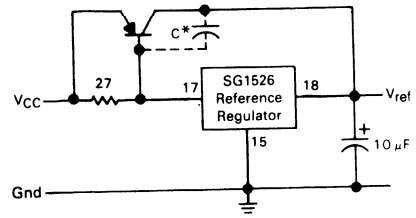


The metering FLIP-FLOP is an asynchronous data latch which suppresses high frequency oscillations by allowing only one PWM pulse per oscillator cycle.

The memory FLIP-FLOP prevents double pulsing in a push-pull configuration by remembering which output produced the last pulse.

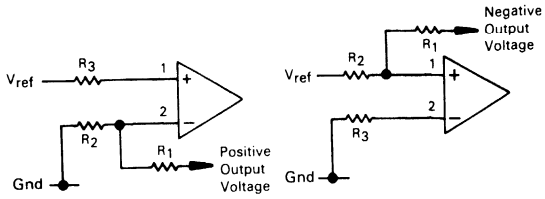
APPLICATIONS INFORMATION

FIGURE 12 — EXTENDING REFERENCE OUTPUT CURRENT CAPABILITY



*May be required with some types of transistors

FIGURE 13 — ERROR AMPLIFIER CONNECTIONS



$V_{out} = V_{ref}\left(\frac{R_1 + R_2}{R_2}\right)$

$V_{out} = V_{ref}\left(\frac{R_1}{R_2}\right)$

$R_3 = \left(\frac{R_1 R_2}{R_1 + R_2}\right)$

FIGURE 14 — OSCILLATOR CONNECTIONS

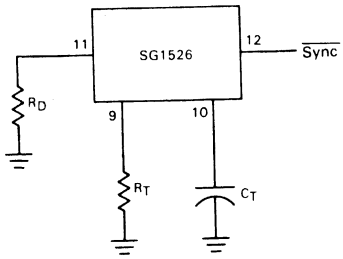
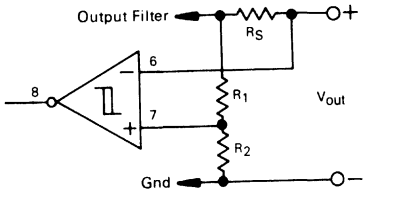


FIGURE 15 — FOLDBACK CURRENT LIMITING



$I_{max} = \frac{\left(0.1\,V + \frac{V_{out} R_1}{R1 + R2}\right)}{R_S}$

$I_{SC} = \left(\frac{0.1\,V}{R_S}\right)$

FIGURE 16 — SG1526 SOFT-START CIRCUITRY

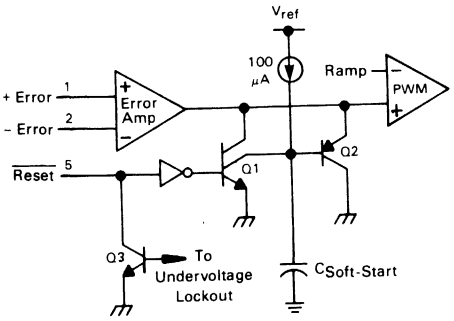
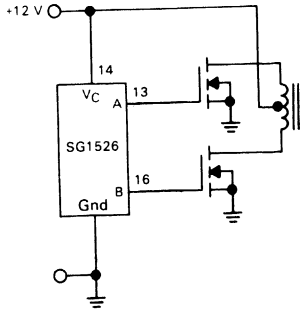


FIGURE 17 — DRIVING VMOS POWER FETS



The totem pole output drivers of the SG1526 are ideally suited for driving the input capacitance of power FETs at high speeds.

FIGURE 18 — HALF-BRIDGE CONFIGURATION

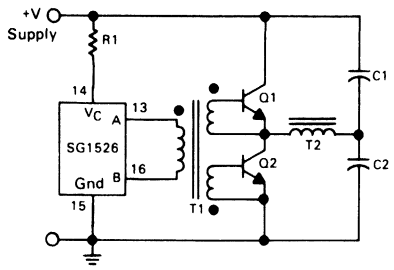
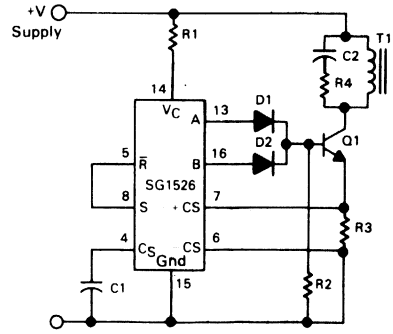


FIGURE 19 — FLYBACK CONVERTER WITH CURRENT LIMITING



In the above circuit, current limiting is accomplished by using the current limit comparator output to reset the soft-start capacitor.

FIGURE 20 — SINGLE-ENDED CONFIGURATION

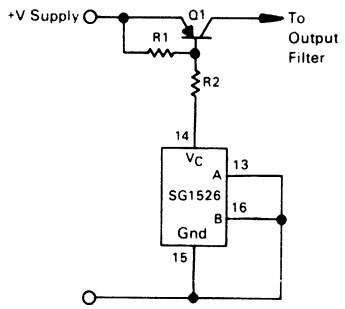
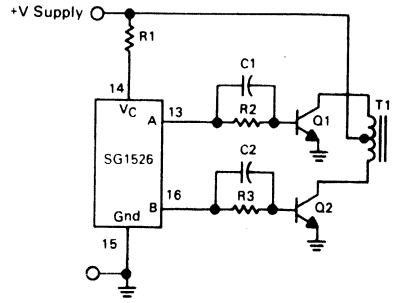


FIGURE 21 — PUSH-PULL CONFIGURATION



MOTOROLA

TCA5600

Advance Information

UNIVERSAL MICROPROCESSOR POWER SUPPLY CONTROLLER

The TCA5600 is a versatile power supply control circuit for microprocessor based systems and mainly intended for automotive applications and battery powered instruments. To cover a wide range of applications, the device offers high circuit flexibility with minimum of external components.

Functions included in this IC are a temperature compensated voltage reference, on chip dc/dc converter, programmable and remote controlled voltage regulator, fixed 5.0 V supply voltage regulator with external PNP power device, undervoltage detection circuit, power-on RESET delay and watchdog feature for safe and hazard free microprocessor operations.

- 6.0 to 30 V Operation Range
- 2.5 V Reference Voltage Accessible for Other Tasks
- Fixed 5.0 V ± 4% Microprocessor Supply Regulator Including Current Limitation, Overvoltage Protection and Undervoltage Monitor
- Programmable 6.0 to 30 V Voltage Regulator Exhibiting High Peak Current (150 mA), Current Limiting and Thermal Protection
- Two Remote Inputs to Select the Regulator's Operation Mode: OFF, 5.0 V, 5.0 V Standby and Programmable Output Voltage
- Self Contained dc/dc Converter Fully Controlled By the Programmable Regulator to Guarantee Safe Operation Under All Working Conditions
- Programmable Power-On RESET Delay
- Watchdog Select Input
- Negative Edge Triggered Watchdog Input
- Low Current Consumption in the V_{CC1} Standby Mode
- All Digital Control Ports are TTL- and MOS-Compatible

APPLICATIONS INCLUDE:

- Microprocessor Systems with E^2PROMs
- High Voltage Crystal and Plasma Displays
- Decentralized Power Supplies in Computer and Telecommunication Systems

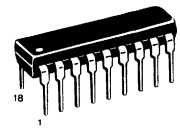
RECOMMENDED OPERATION CONDITIONS

Characteristic	Symbol	Min	Max	Unit
Power Supply Voltage	V_{CC1} V_{CC2}	5.0 5.5	30 30	V
Collector Current	I_C	—	800	mA
Output Voltage	V_{out2}	6.0	30	V
Reference Source Current	I_{ref}	0	2.0	mA

This document contains information on a new product. Specifications and information herein are subject to change without notice.

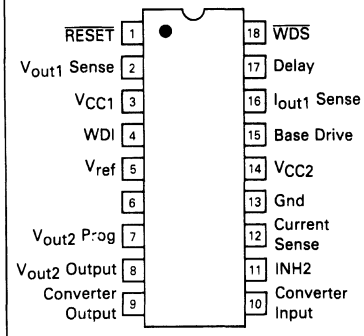
UNIVERSAL MICROPROCESSOR POWER SUPPLY CONTROLLER

SILICON MONOLITHIC INTEGRATED CIRCUITS



N SUFFIX
PLASTIC PACKAGE
CASE 707-02

PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

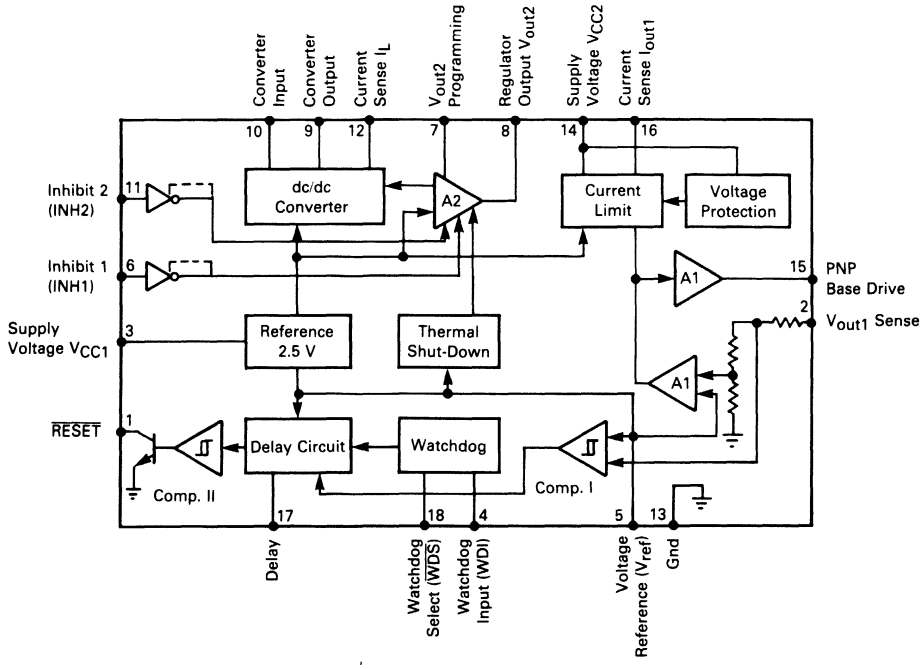
Device	Operating Junction Temperature Range	Package
TCA5600	−40° to +125°C	Plastic DIP

MAXIMUM RATINGS (T_A = +25°C unless otherwise noted, Note 1)

Rating	Symbol	Value	Unit
Power Supply Voltage (Pin 3, 14)	V_{CC1}, V_{CC2}	35	Vdc
Base Drive Current (Pin 15)	I_B	20	mA
Collector Current (Pin 10)	I_C	1.0	A
Forward Rectifier Current (Pin 10–Pin 9)	I_F	1.0	A
Logic Inputs INH1, INH2, $\overline{WDS}$ (Pin 6, 11, 18)	V_{INP}	−0.3 V to V_{CC1}	Vdc
Logic Input Current WDI (Pin 4)	I_{WDI}	±0.5	mA
Output Sink Current $\overline{RESET}$ (Pin 1)	$I_{\overline{RES}}$	10	mA
Analog Inputs (Pin 2) (Pin 7)	— —	−0.3 to 10 −0.3 to 5.0	V
Reference Source Current (Pin 5)	I_{ref}	5.0	mA
Power Dissipation (Note 2) T_A = +85°C	P_D	500	mW
Thermal Resistance (Junction to Air)	$R_{\theta JA}$	100	°C/W
Operating Temperature Range	T_A	−40 to +85°C	°C
Operating Junction Temperature	T_J	+125	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C

NOTES:
1. Values beyond which damage may occur.
2. Derate at 10 mW/°C for ambient temperature above +85°C.

FIGURE 1 — FUNCTIONAL BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS (V_{CC1} = V_{CC2} = 12 V; T_J = 25°C; I_{ref} = 0; I_{out1} = 0 (Note 3); R_{SC} = 0.5 Ω; INH1 = "High"; INH2 = "High"; $\overline{WDS}$ = "High"; I_{out2} = 0 (Note 4); if not otherwise specified)

Characteristic	Figure	Symbol	Min	Typ	Max	Unit
REFERENCE SECTION						
Nominal Reference Voltage	1	$V_{ref\ nom}$	2.42	2.5	2.58	V
Reference Voltage I_{ref} = 0.5 mA, $T_{low} \leq T_J \leq T_{high}$ (Note 5), 6.0 V ≤ V_{CC1} ≤ 18 V		V_{ref}	2.4	—	2.6	V
Line Regulation (6.0 V ≤ V_{CC2} ≤ 18 V)		Reg_{line}	—	2.0	15	mV
Average Temperature Coefficient $T_{low} \leq T_J \leq T_{high}$ (Note 5)	2	$\frac{\Delta V_{ref}}{\Delta T_J}$	—	—	+/−0.5	mV/°C
Ripple Rejection Ratio f = 1.0 kHz, V_{sin} = 1.0 V_{pp}	3	RR	60	70	—	dB
Output Impedance 0 ≤ I_{ref} ≤ 2.0 mA		Z_O	—	1.0	—	Ohm
Standby Current Consumption V_{CC2} = Open	4	I_{CC1}	—	3.0	—	mA
5.0 V MICROPROCESSOR VOLTAGE REGULATOR SECTION						
Nominal Output Voltage		$V_{out1(nom)}$	4.8	5.0	5.2	V
Output Voltage 5.0 mA ≤ I_{out1} ≤ 300 mA, $T_{low} \leq T_J \leq T_{high}$ (Note 5) 6.0 V ≤ V_{CC2} ≤ 18 V	5 6	V_{out1}	4.75	—	5.25	V
Line Regulation (6.0 V ≤ V_{CC2} ≤ 18 V)		Reg_{line}	—	10	50	mV
Load Regulation (5.0 mA ≤ I_{out1} ≤ 300 mA)		Reg_{load}	—	20	100	mV
Base Current Drive (V_{CC2} = 6.0 V, V_{15} = 4.0 V)		I_B	10	15	—	mA
Ripple Rejection Ratio f = 1.0 kHz, V_{sin} = 1.0 V_{pp}	3	RR	50	65	—	dB
Undervoltage Detection Level (R_{SC} = 5.0 Ω)	7	V_{low}	4.5	0.93 x V_{out1}	—	V
Current Limitation Threshold (R_{SC} = 5.0 Ω)		V_{RSC}	210	250	290	mV
Average Temperature Coefficient $T_{low} \leq T_J \leq T_{high}$ (Note 5)		$\frac{\Delta V_{out1}}{\Delta T_J}$	—	—	±1.0	mV/°C

NOTES:

3. The external PNP power transistor satisfies the following minimum specifications:
   $h_{FE} \geq 60$ at I_C = 500 mA and V_{CE} = 5.0 V; $V_{CE(sat)} \leq 300$ mV at I_B = 10 mA and I_C = 300 mA
4. Regulator V_{out2} programmed for nominal 24 V output by means of R4, R5 (see Figure 1)
5. T_{low} = −40°C
   T_{high} = +125°C

Characteristic	Figure	Symbol	Min	Typ	Max	Unit
PROGRAMMABLE VOLTAGE REGULATOR SECTION (Note 6)						
Nominal Output Voltage		$V_{out2(nom)}$	23	24	25	V
Output Voltage 1.0 mA ≤ I_{out2} ≤ 100 mA, T_{low} ≤ T_J ≤ T_{high} (Notes 5, 7)	8	V_{out2}	22.8	—	25.2	V
Load Regulation 1.0 mA ≤ I_{out2} ≤ 100 mA (Note 7)		Reg_{load}	—	40	200	mV
DC Output Current		I_{out2}	100	—	—	mA
Peak Output Current (Internally Limited)		$I_{out2\,p}$	150	200	—	mA
Ripple Rejection Ratio f = 20 kHz, V = 0.4 V_{pp}		RR	45	55	—	dB
Output Voltage (Fixed 5.0 V) 1.0 mA ≤ I_{out2} ≤ 20 mA, T_{low} ≤ T_J ≤ T_{high}, INH1 = "High" (Note 5)		$V_{out2(5.0\ V)}$	4.75	—	5.25	V
OFF State Output Impedance (INH2 = "Low")		R_{out1}	—	10	—	kΩ
Average Temperature Coefficient T_{low} ≤ T_J ≤ T_{high} (Note 5)		$\frac{\Delta V_{out2}}{\Delta T_J V_{out2}}$	—	—	±0.25	mV/°C V
DC/DC CONVERTER SECTION						
Collector Current Detection Level "High" R_C = 10 k "Low"	9	$V_{12}(H)$ $V_{12}(L)$	350 —	400 50	450 —	mV
Collector Saturation Voltage I_C = 600 mA (Note 7)	10	$V_{CE(sat)}$	—	—	1.6	V
Rectifier Forward Voltage Drop I_F = 600 mA (Note 7)	11	V_F	—	—	1.4	V
WATCHDOG AND $\overline{\text{RESET}}$ CIRCUIT SECTION						
Threshold Voltage "High" (static) "Low"		$V_{C5(H)}$ $V_{C5(L)}$	— —	2.5 1.0	— —	V
Current Source T_{low} ≤ T_J ≤ T_{high} (Note 5) Power-Up $\overline{\text{RESET}}$ Watchdog Time Out Watchdog $\overline{\text{RESET}}$		I_{C5}	 −1.8 — —	 −2.5 5xI_{C5} −50xI_{C5}	 −3.2 — —	μA
Watchdog Input Voltage Swing		V_{WDI}	—	—	±5.5	V
Watchdog Input Impedance		r_i	12	15	—	kΩ
Watchdog Reset Pulse Width (C8 = 1.0 nF) (Note 9)		t_p	—	—	10	μs
DIGITAL PORTS: $\overline{\text{WDS}}$, INH 1, INH 2, $\overline{\text{RESET}}$ (Note 8)						
Input Voltage Range		V_{INP}	—	—	−0.3 to V_{CC1}	V
Input HIGH Current 2.0 V ≤ V_{IH} ≤ 5.5 V 5.5 V ≤ V_{IH} ≤ V_{CC1}		I_{IH}	 — —	 — —	 100 150	μA
Input LOW Current −0.3 V ≤ V_{IL} ≤ 0.8 V for INH1, INH2, −0.3 V ≤ V_{IL} ≤ 0.4 V for $\overline{\text{WDS}}$		I_{IL}	 —	 —	 −100	μA
Leakage Current Immunity (INH2, High "Z" State)	12	I_Z	±20	—	—	μA
Output LOW Voltage $\overline{\text{RESET}}$ (I_{OL} = 6.0 mA)		V_{OL}	—	—	0.4	V
Output HIGH Current $\overline{\text{RESET}}$ (V_{OH} = 5.5 V)		V_{OH}	—	—	20	μA

NOTES:
5. T_{low} = −40°C
   T_{high} = +125°C
6. V_9 = 28 V, INH1 = "Low" for this Electrical Characteristic section unless otherwise specified.
7. Pulse tested t_p ≤ 300 μs
8. Temperature range T_{low} ≤ T_J ≤ T_{high} applies to this Electrical Characteristics section.
9. For test purposes, a negative pulse is applied to Pin 4 (−2.5 V ≥ V_4 ≥ −5.5 V).

TYPICAL CHARACTERISTICS

FIGURE 1 — REFERENCE VOLTAGE versus SUPPLY VOLTAGE

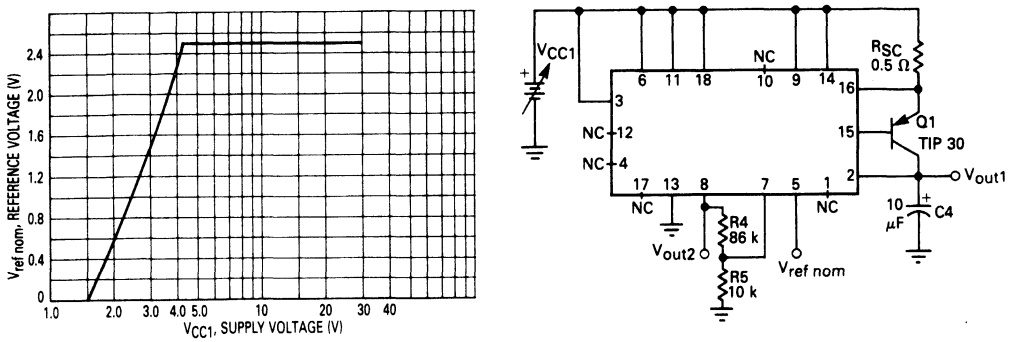


FIGURE 2 — REFERENCE STABILITY versus TEMPERATURE

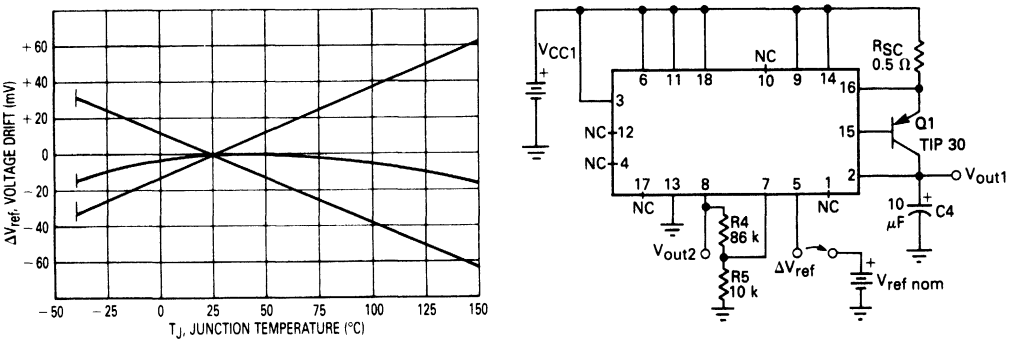


FIGURE 3 — RIPPLE REJECTION versus FREQUENCY

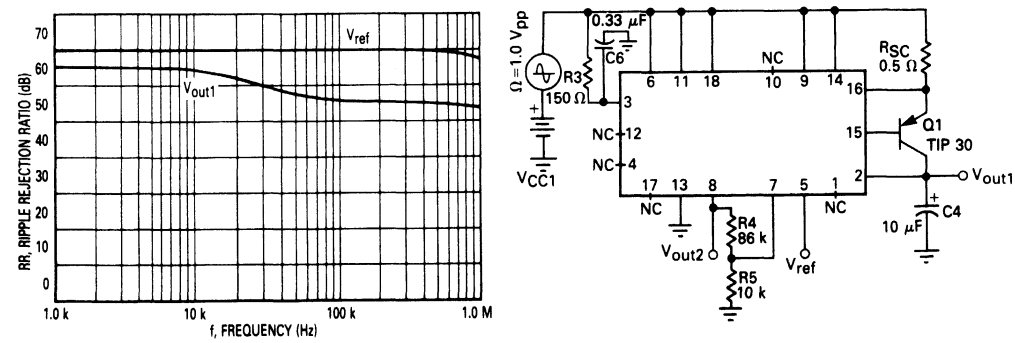


FIGURE 4 — STAND-BY CURRENT versus SUPPLY VOLTAGE

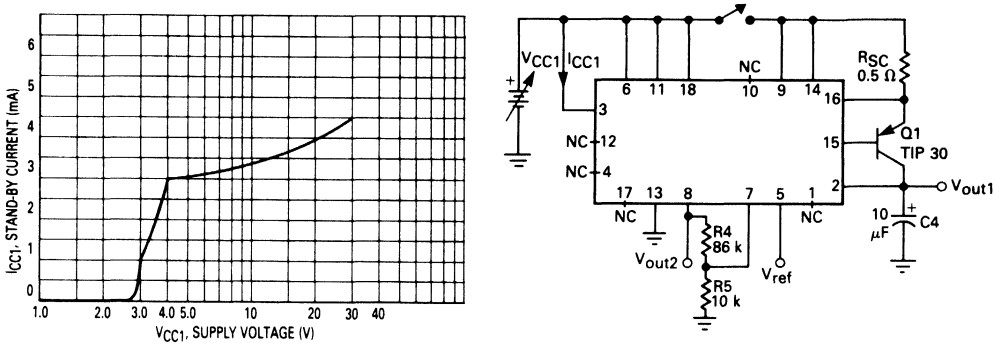


FIGURE 5 — POWER-UP BEHAVIOR OF THE 5.0 V REGULATOR

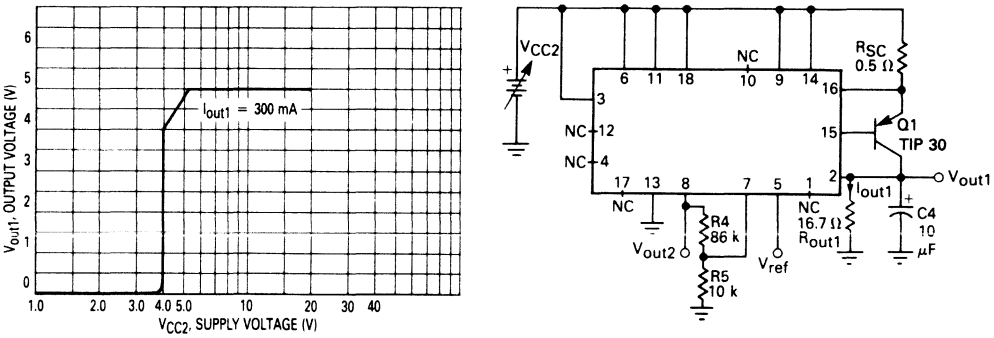


FIGURE 6 — FOLDBACK CHARACTERISTICS OF THE 5.0 V REGULATOR

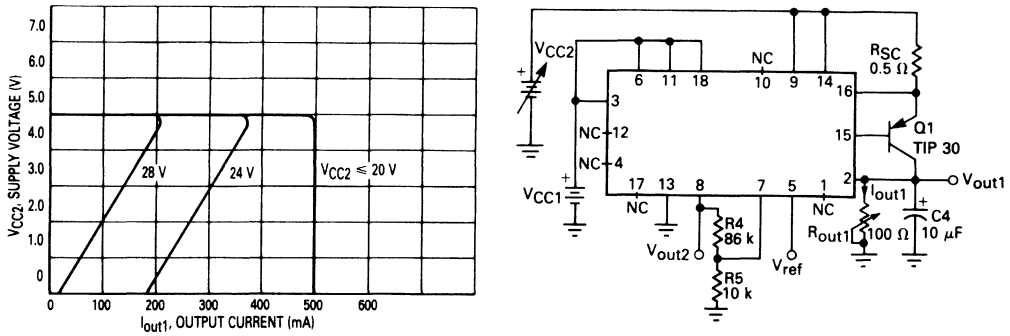


FIGURE 7 — UNDERVOLTAGE LOCKOUT CHARACTERISTICS

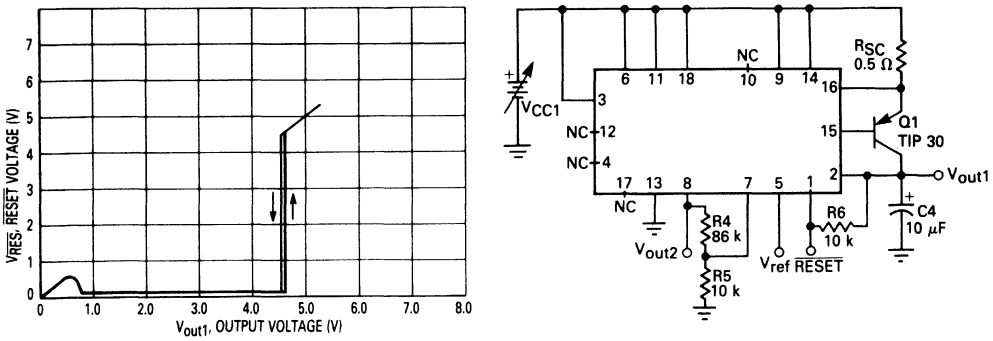


FIGURE 8 — OUTPUT CURRENT CAPABILITY OF THE PROGRAMMING REGULATOR

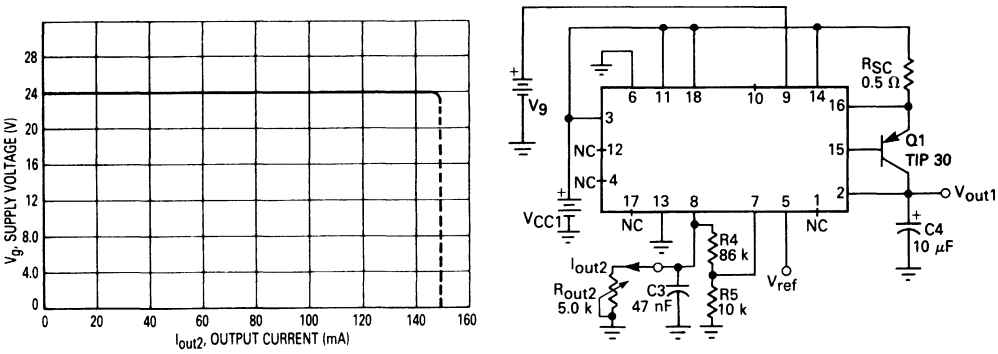


FIGURE 9 — COLLECTOR CURRENT DETECTION LEVEL

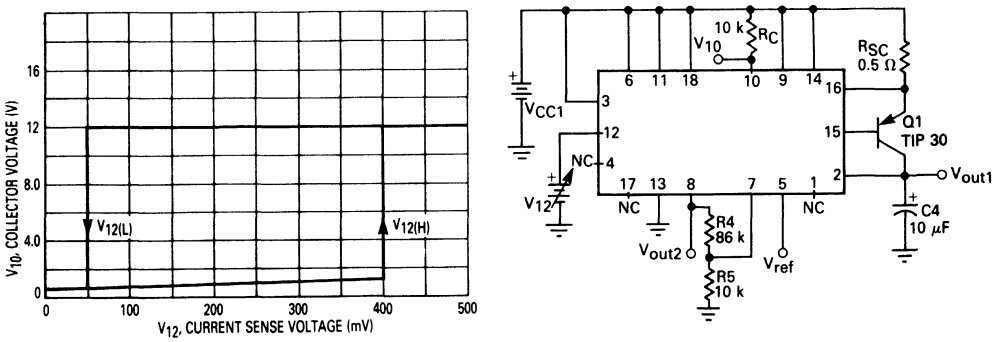


FIGURE 10 — POWER SWITCH CHARACTERISTICS

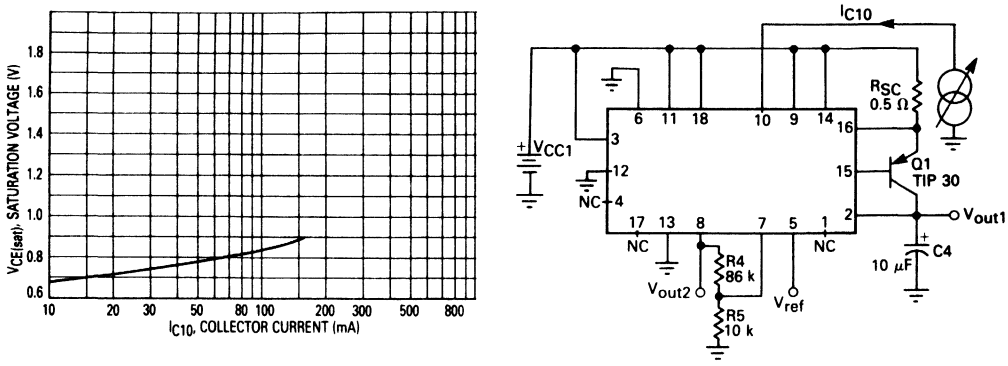


FIGURE 11 — RECTIFIER CHARACTERISTICS

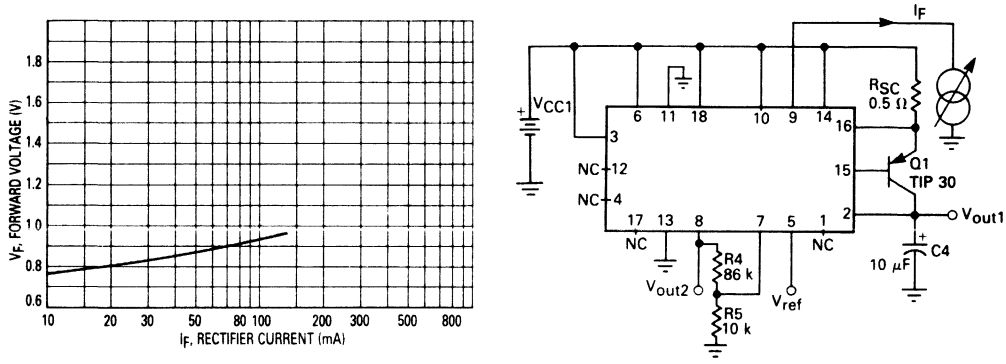
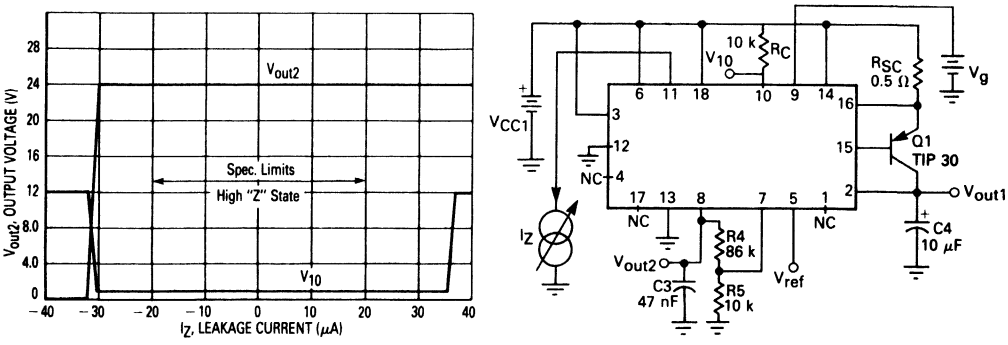


FIGURE 12 — INH 2 LEAKAGE CURRENT IMMUNITY



APPLICATIONS INFORMATION
(See Figure 18)

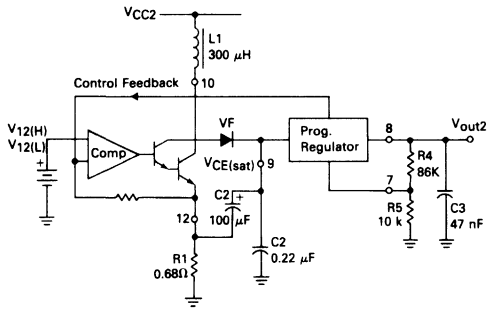
1. VOLTAGE REFERENCE V_{ref}

The voltage reference V_{ref} is based upon a highly stable bandgap voltage reference and is accessible on Pin 5 for additional tasks. This circuit part has its own supply connection on Pin 3 and is therefore able to operate in standby mode. The RC network R3, C6 improves the ripple rejection on both regulators.

2. DC/DC CONVERTER

The dc/dc converter performs according to the fly back principle and does not need a time base circuit. The maximum coil current is well defined by means of the current sensing resistor R1 under all working conditions (start-up phase, circuit overload, wide supply voltage range and extreme load current change). Figure 13 shows the simplified converter schematic:

FIGURE 13 — SIMPLIFIED CONVERTER SCHEMATIC



A simplified method on "how to calculate the coil inductance" is given below. The operation point at min. supply voltage (V_{CC2}) and max. output current (I_{out2}) for a fixed output voltage (V_{out2}) determines the coil data. Figure 14 shows the typical voltage and current wave forms on the coil L1 (coil losses neglected).

The equations (1) and (2) yield the respective coil voltage V_L- and V_L+ (see Figure 14):

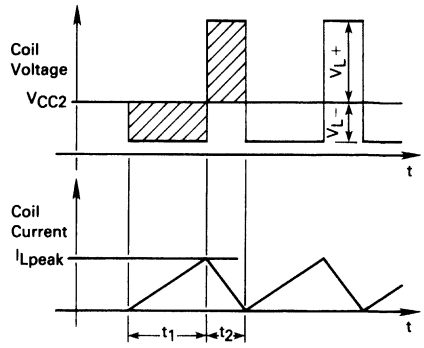
$$V_L+ = V_{out2} + \Delta V_{(Pin\ 9\ -\ Pin\ 8)} + V_F - V_{CC2} \quad (1)$$

$$V_L- = V_{CC2} - V_{CE(sat)} - V_{12(H)} \quad (2)$$

($\Delta V_{(Pin\ 9\ -\ Pin\ 8)}$: input/output voltage drop of the regulator, 2.5 V typical)

(V_F, $V_{CE(sat)}$, $V_{12(H)}$: see electrical characteristics)

FIGURE 14 — VOLTAGE AND CURRENT WAVEFORM ON THE COIL (not to scale)



The time ratio α for the charging time to dumping time is defined by equation (3):

$$\alpha = \frac{t_1}{t_2} = \frac{V_L+}{V_L-} \quad (3)$$

The coil charging time t_1 is found using equation (4):

$$t_1 = \frac{1}{(1 + \frac{1}{\alpha}) \cdot f} \quad (4)$$

(f : min. oscillation frequency which should be chosen above the audio frequency band (e.g. 20 kHz))

Knowing the dc output current I_{out2} of the programmable regulator, the peak coil current $I_{L(peak)}$ can now be calculated:

$$I_{L(peak)} = 2 \cdot I_{out2} \cdot (1 + \alpha) \quad (5)$$

The coil inductance L1 of the nonsaturated coil is given by equation (6):

$$L1 = \frac{t_1}{I_{L(peak)}} \cdot V_L- \quad (6)$$

The formula (6a) yields the current sensing resister R1 for a defined peak coil current $I_{L(peak)}$:

$$R1 = \frac{V_{12(H)}}{I_{L(peak)}} \quad (6a)$$

In order to limit the by-pass current through capacitor C7 during the energy dumping phase the value C2>>C7 should be implemented.

For all other operation conditions, the feedback signal from the programmable voltage regulator controls the activity of the converter.

3. PROGRAMMABLE VOLTAGE REGULATOR

This series voltage regulator is programmable by the voltage divider R4, R5 for a nominal output voltage 6.0 V ≤ V_{out2} ≤ 30 V.

$$R4 = \frac{(V_{out2} - V_{ref\ nom}) \cdot R5}{V_{ref\ nom}} \quad (7)$$

(R5 = 10 k, $V_{ref\ nom}$ = 2.5 V)

Current limitation and thermal shutdown capability are standard features of this regulator. The voltage drop $\Delta V_{(Pin\ 9\ -\ Pin\ 8)}$ across the series pass transistor generates the feedback signal to control the dc/dc converter (see Figure 13).

4. CONTROL INPUTS INH1, INH2

The dc/dc converter and/or the regulator V_{out2} are remote controllable through the TTL, MOS compatible inhibit inputs INH1 and INH2 where the latter is a 3-level detector (Logic "0", high impedance "Z", Logic "1"). Both inputs are setup to provide the following truth table:

FIGURE 15 — INH1, INH2 TRUTH TABLE

Mode	INH1	INH2	V_{out2}	dc/dc
1	0	0	OFF	INT
2	0	High "Z"	V_{out2}	ON
3	0	1	V_{out2}	INT
4	1	0	OFF	INT
5	1	High "Z"	5.0 V	ON
6	1	1	5.0 V	INT

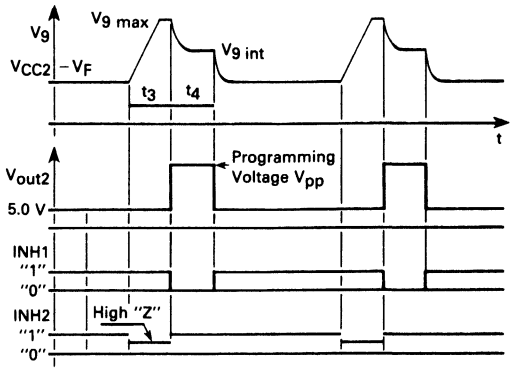
INT: Intermittent operation of the converter means that the converter operates only if $V_{CC2} < V_{out2}$.
ON: The converter loads the storage capacitor C2 to its full charge (V_9 = 33 V), allowing fast response time of the regulator V_{out2} when addressed by the control software.
OFF: High impedance (internal resistor 10 k to ground)

Figure 16 represents a typical timing diagram for an E²PROM programming sequence in a microprocessor based system. The high "Z" state enables the dc/dc converter to ramp during t_3 to the voltage V_9 at Pin 9 to a high level before the write cycle takes place in the memory.

5. MICROPROCESSOR SUPPLY REGULATOR

Together with an external PNP power transistor (Q1), a 5.0 V supply exhibiting low voltage drop is obtained to power microprocessor systems and auxilliary circuits. Using a power Darlington with adequate heat sink in the output stage boosts the output current I_{out1} above 1 amp.

FIGURE 16 — TYPICAL E²PROM PROGRAMMING SEQUENCE (not to scale)



The current limitation circuit measures the emitter current of Q1 by means of the sensing resistor R_{SC}.

$$R_{SC} = \frac{V_{RSC}}{I_E} \quad (8)$$

(I_E: emitter current of Q1)

(V_{RSC}: threshold voltage (see electrical characteristics))

The voltage protection circuit performs a fold-back characteristic above a nominal operating voltage V_{CC2} ≥ 18 V.

6. DELAY AND WATCHDOG CIRCUIT

The under voltage monitor supervises the power supply V_{out1} and releases the delay circuit $\overline{RESET}$ as soon as the regulator output reaches the microprocessor operating range (e.g. $V_{LOW} \geq 0.93 \cdot V_{out1(nom)}$). The $\overline{RESET}$ output has an open-collector and may be connected in a "wired-OR" configuration.

The watchdog circuit consists of a retriggerable monostable with a negative edge sensitive control input WDI. The watchdog feature may be disabled by means of the watchdog select input $\overline{WDS}$ driven to a "1". Figure 17 displays the typical $\overline{RESET}$ timing diagram.

The commuted current source I_{C5} on Pin 17, threshold voltage $V_{C5(L)}$, $V_{C5(H)}$ and an external capacitor C5 define the $\overline{RESET}$ delay and the watchdog timing. The relationship of the timing signals are indicated by the equations (9) to (11).

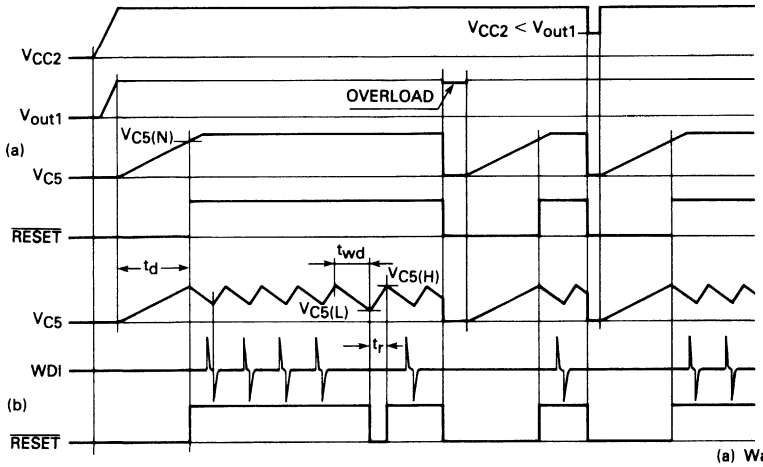
$\overline{RESET}$ delay: $$t_d = \frac{C5 \cdot V_{C5(H)}}{|I_{C5}|} \quad (9)$$

Watchdog time-out: $$t_{wd} = \frac{C5 \cdot (V_{C5(H)} - V_{C5(L)})}{5 \cdot I_{C5}} \quad (10)$$

Watchdog $\overline{RESET}$: $$t_r = \frac{C5 \cdot (V_{C5(H)} - V_{C5(L)})}{50 \cdot |I_{C5}|} \quad (11)$$

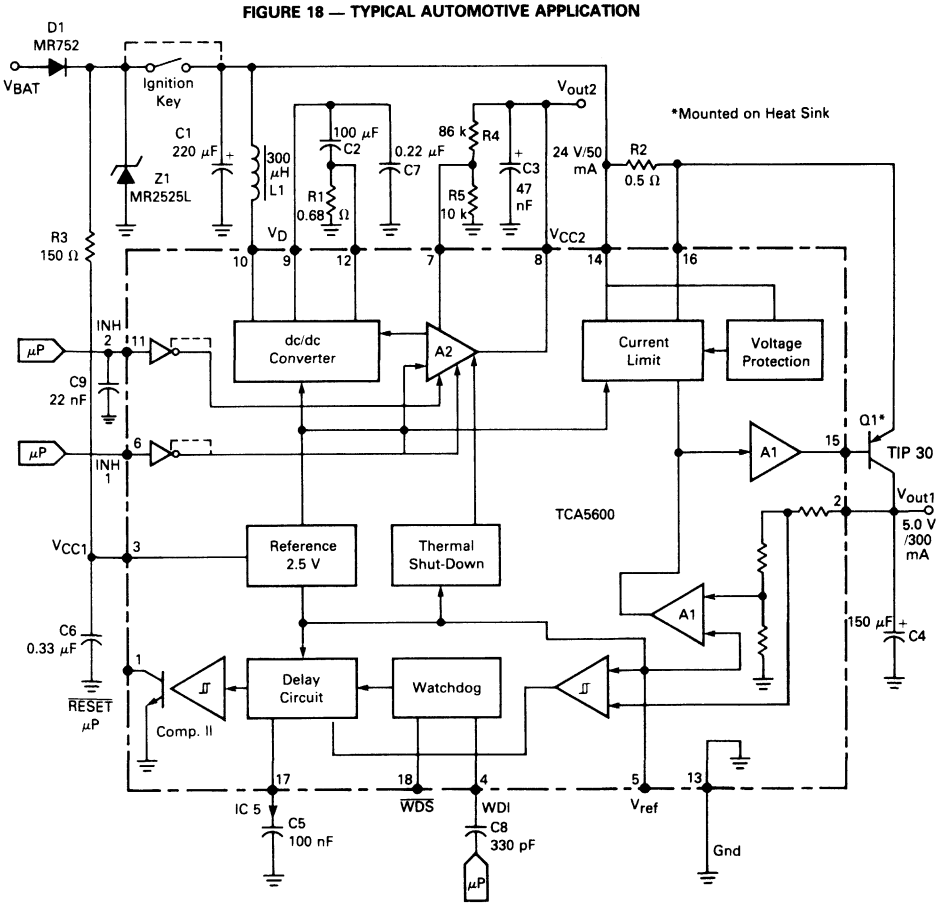
(I_{C5}, $V_{C5(H)}$, $V_{C5(L)}$: see electrical characteristics.)

FIGURE 17 — TYPICAL $\overline{\text{RESET}}$ TIMING DIAGRAM
(not to scale)



(a) Watchdog inhibited, $\overline{\text{WDS}}$ = "1"
(b) Watchdog operational, $\overline{\text{WDS}}$ = "0"

FIGURE 18 — TYPICAL AUTOMOTIVE APPLICATION



MOTOROLA

TDA4601,B

Advance Information

CONTROL IC FOR LINE-ISOLATED FREE RUNNING FLYBACK CONVERTER

The bipolar integrated circuit TDA4601,B drives, regulates and monitors the switching transistor in a power supply based on the ringing choke flyback principle.

Due to the wide regulating range and the high voltage stability during large load changes, SMPS for Hi-Fi equipment and active loudspeakers can be realized as well as applications in TV receivers and video recorders.

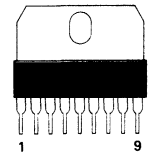
The TDA4601,B is available in a 9-pin power SIP and an 18-pin plastic medium power dual-in-line package. The operating temperature range is −15°C to +85°C.

- Wide Operational Range
- High Voltage Stability Even at High Load Changes
- Direct Control of Switching Transistor
- Low Start-Up Current
- Linear Foldback of the Overload Characteristic
- Base Drive Proportional to the Current Through the Power Switching Transistor
- Stand-By Mode 3.5 W into the External Load
- Inhibit Capability (TTL Compatible)
- Undervoltage Lockout

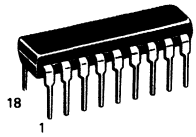
For Application Details See ANE002

FLYBACK CONVERTER CONTROL CIRCUIT

SILICON MONOLITHIC INTEGRATED CIRCUIT

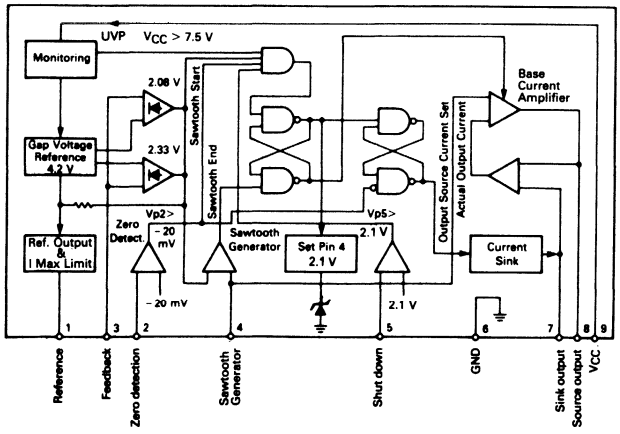


PLASTIC MEDIUM POWER PACKAGE
CASE 762-01

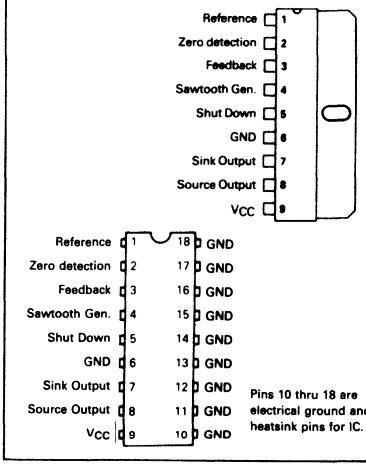


B SUFFIX
PLASTIC PACKAGE
CASE 707-02

BLOCK DIAGRAM



PIN ASSIGNMENTS



Pins 10 thru 18 are electrical ground and heatsink pins for IC.

ORDERING INFORMATION

Device	Temperature Range	Package
TDA4601	−15°C to +85°C	Plastic SIP
TDA4601B		Plastic DIP

This document contains information on a new product. Specifications and information herein are subject to change without notice.

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage	V_9	20	V
Sink Output Voltage	V_7 V_7–V_8	0 to V_9 ±6.0	V V
Reference Output	I_1	−10 to +1.0	mA
Zero Crossing	I_2	−3.0 to +3.0	mA
Control Amplifier	I_3	−3.0 to 0	mA
Collector Current	I_4	−2.0 to +5.0	mA
Trigger Input	I_5	−2.0 to +3.0	mA
Sink Output	I_7	−1.5	A
Junction Temperature	T_J	+150	°C
Storage Temperature	T_{stg}	−40 to +125	°C
Thermal Resistance (Junction to Air)	θ_{JA}	70	°C/W
Thermal Resistance (Junction to Case)	θ_{JC}	15	°C/W

ELECTRICAL CHARACTERISTICS (T_A = +25°C unless otherwise stated)

Range of Operation	Symbol	Fig. No.	Min	Typ	Max	Unit
Supply Voltage	V_9		—	15	18	V
Ambient Temperature	T_A		−15	—	85	°C
START OPERATION T_A = 25°C						
Current Consumption (V_1 Not Yet Switched)	I_9	1				mA
V_9 = 3.0 V			—	—	0.5	
V_9 = 5.0 V			—	1.5	2.0	
V_9 = 10 V			—	2.0	3.2	
Turn-On Point for V_1	V_9	1	11.3	11.8	12.3	V
V_4 Before Start-Up (V_9 < 11.8 V)	V_4	1	6.0	6.7	—	V
REGULATION MODE V_9 = 15 V T_A = 25°C						
Current Consumption V_{reg} = −10 V	I_9	1	110	135	160	mA
V_{reg} = 0			55	85	110	
Reference Voltage I_1 < 0.1 mA	V_1	1	4.0	4.2	4.5	V
I_1 = 5.0 mA			4.0	4.2	4.4	
Reference Voltage Temperature Coefficient	TC_1	1	—	100	—	ppm/°C
$V_{Pin\ 4}$ Low Static Voltage	V_4	1	1.8	2.08	2.5	V
$V_{Pin\ 4}$ Regulation Peak Voltage	$V_{4\ peak}$	1				V
$I_{Pin\ 3}$ = 5.0 μA			4.0	4.2	4.5	
$I_{Pin\ 3}$ = 1.3 mA			—	2.4	3.0	
$V_{Pin\ 3}$	V_3	1				V
Full Fold Back $I_{Pin\ 3}$ = 1.3 mA			—	3.7	4.0	
Fold Back $I_{Pin\ 3}$ = 0.5 mA			—	2.5	3.0	
Overload Decision $I_{Pin\ 3}$ = 1.0 μA			—	2.4	2.9	
$V_{Pin\ 3}$ Regulation			—	2.11	—	
$I_{Pin\ 3}$ Regulation	I_3	1	—	1.0	—	μA
$I_{Pin\ 3}$ Leakage at $V_{Pin\ 3}$ = 1.5 V			—	0.4	—	
$V_{Pin\ 7}$ Peak High	$V_{7\ peak}$	1				V
V_R = 0 V (Full Fold Back)			—	3.5	—	
V_R = −10 V (Regulation)			—	4.0	—	
V_R = −15 V (Standby)			—	5.0	—	
$V_{Pin\ 7}$ Peak Low	$V_{7\ peak}$	1				V
V_R = 0 V			—	1.4	—	
V_R = −10 V			—	1.45	—	
V_R = −15 V			—	1.57	—	

ELECTRICAL CHARACTERISTICS (continued) T_A = 25°C

Range of Operation	Symbol	Fig. No.	Min	Typ	Max	Unit
REGULATION MODE (continued) V_9 = 15 V T_A = 25°C						
$I_{Pin\ 7}$ Sink Peak V_R = −15 V	$I_{7\ peak}$	1	—	+0.7	—	A
$I_{Pin\ 8}$ Source Peak V_R = −15 V	$I_{8\ peak}$	1	—	−0.8	—	A
$V_{Pin\ 2}$ $I_{Pin\ 2}$ = −3.0 mA = −0.3 mA +3.0 mA +0.3 mA	V_2	1	 — — — —	 −0.3 −0.2 +0.7 +0.8	 — — — —	V
PROTECTIVE OPERATION V_9 = 15 V T_A = 25°C						
Current Consumption (V_5 < 1.8 V)	I_9	1	14	20	26	mA
Turn-Off Voltage (V_5 < 1.8 V)	V_7 V_4	1 1	1.3 1.8	1.5 2.1	1.8 2.5	V
External Trigger Input Enable Voltage (V_{reg} = 0 V) Disabled Voltage (V_{reg} = 0 V)	V_5	1	 — 2.0	 2.2 2.2	 2.4 —	V
Supply Voltage Disabling V_8 and V_1	V_9	1	6.7	7.4	7.8	V
$V_{Pin\ 5}$ Zener Voltage (Pin 5 Open)	V_5	1	6.5	7.3	7.8	V
$I_{Pin\ 5}$ $V_{Pin\ 5}$ = 3.0 V $V_{Pin\ 5}$ = 0 V	I_5	1	— —	1.4 −11	— —	μA
Turn-On Time (Secondary Voltages)	t_{on}	2	—	350	450	ms
Voltage Change When S_3 = Closed (ΔP_3 = 19 W) When S_2 = Closed (ΔP_2 = 15 W)	ΔV_2	2	 — —	 100 500	 500 1000	mV
Standby Operation (Minimum Secondary Power: 3.0 Watts) When S_1 = Open	ΔV_2	2	—	20	30	V
Switching Frequency During Standby Mode	f	2	70	75	—	kHz
Primary Power Consumption During Standby Mode The heat sink must be optimized, taking the maximum data (T_J, θ_{JC}, T_A) into consideration	P_{prim}	2	—	10	15	VA

CIRCUIT DESCRIPTION

The TDA4601 regulates, controls and protects the switching transistor in flyback converter power supplies at starting-up, normal, and overload operation.

A. Start-Up Sequence

During start-up there are three consecutive operations:

1. An internal reference voltage is created. It supplies the voltage regulator and enables the supply to the coupling electrolytic capacitor and the switching transistor. For a supply voltage (V_9) of 12 V, the current is less than 3.2 mA.
2. Activation of the internal reference voltage V_1 = 4.0 V. This voltage is suddenly available when V_9 reaches 12 V and enables all parts of the IC to be supplied from the control logic including thermal and overload protection.
3. Activation of the control logic. As soon as the reference voltage is available, the control is switched on through an additional stabilization circuit.

This start-up sequence is necessary for smoothly driving the switching transistor through the coupling electrolytic capacitor.

FIGURE 1 — TEST CONFIGURATION

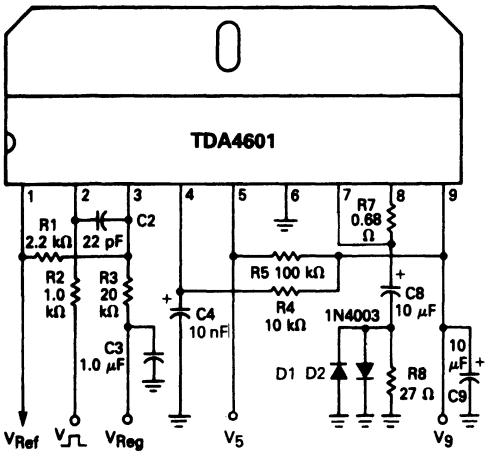
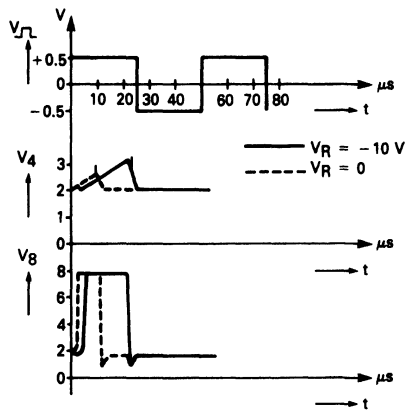


FIGURE 2 — TEST DIAGRAM: NORMAL OPERATION



B. Normal Operation

Zero crossing detection is sensed on Pin 2 and linked to the control logic.

The signal picked up on the feedback winding is applied, after filtering, to Pin 3 (used for input regulation and for overload protection). The regulating section works with an input voltage of about 2.0 V for normal regulation and a current of about 1.4 mA for foldback operation. Together with the collector current simulation Pin 4, the overload recognition defines the operating region of the regulating amplifier depending on the internal reference voltage. The simulation of the collector current is generated by an external RC network at Pin 4 and an internally set voltage level.

For a constant line voltage and for a given output power on the load (t on fixed) less than the maximum output power, a decrease of C4 produces an increase of the current sent to the base of the power switching transistor. So the foldback point is reached earlier. The regulation range starts from a 2.0 Vdc level which is the bottom of a sawtooth waveform; the maximum is limited at 4.0 V (reference voltage).

A secondary load of 19 W produces a switching frequency of about 50 kHz at an almost constant duty cycle (approximately 3). Furthermore, when the switchmode power supply delivers approximately 3.0 W, the switching frequency jumps to about 70 kHz at a duty cycle of approximately 11. At the same time, the collector peak current falls below 1.0 A.

The comparison of the output level of the regulating amplifier, the overload detection and the collector current simulation drives the control logic. An additional steering control and blocking possibility is offered thru Pin 5. When the voltage applied on Pin 5 falls below 2.2 V then the source output (Pin 8) is blocked.

The control logic is set according to the start-up circuit, the zero crossing detection and the trigger enabling. This logic drives the base current amplifier and the base current shutdown. The base current amplifier drives the source output (Pin 8) proportionally to the sawtooth voltage (Pin 4). A current feedback is performed by an external shunt inserted between Pin 8 and the base of the switching power transistor. This resistor determines the maximum amplitude of the base current drive.

C. Protective Features

The base current shut-down, released by the control logic, clamps the sink output (Pin 7) at 1.6 V, turning off the switching transistor. This feature will be released if the voltage on Pin 9 is less than 7.4 V, or if the applied voltage on Pin 5 is less than 2.2 V. In case of a short circuit of the secondary windings, the TDA4601 continuously monitors the fault condition.

In standby operation the circuit is set to a high duty cycle. The total power consumption of the power supply is held below 6.0 to 10 W.

FIGURE 3 — FREQUENCY versus OUTPUT POWER

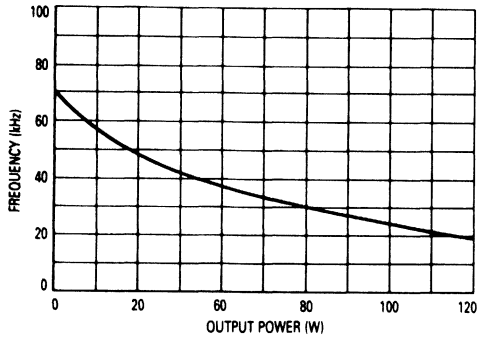


FIGURE 4 — EFFICIENCY versus OUTPUT POWER

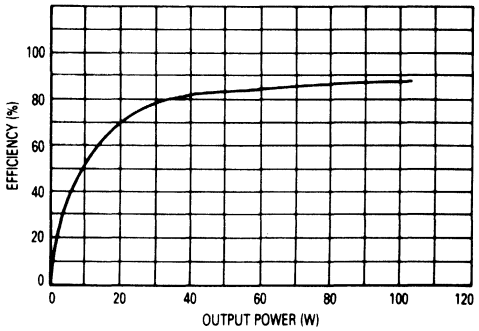


FIGURE 5 — OUTPUT VOLTAGE (V_2) versus OUTPUT CURRENT (I_{q2})

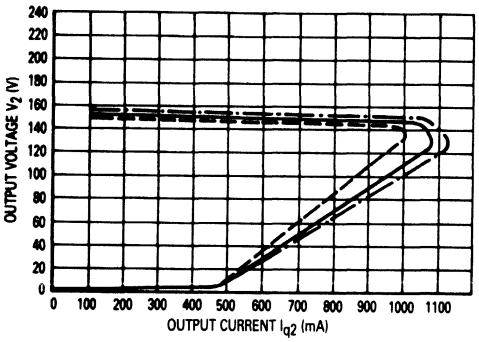
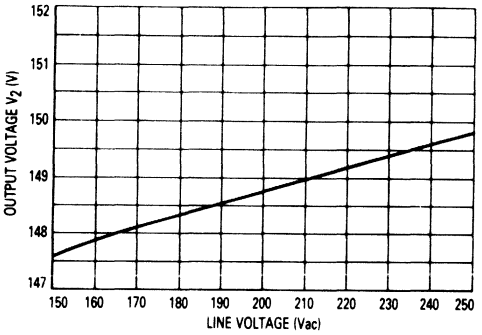


FIGURE 6 — OUTPUT VOLTAGE (V_2) versus LINE VOLTAGE



TEST CIRCUIT AND TYPICAL APPLICATION (See Figure 7)

This application circuit shown in Figure 2 represents a blocking converter for color TV sets with 30 W to 120 W of output power and line voltages from 160 to 270 V.

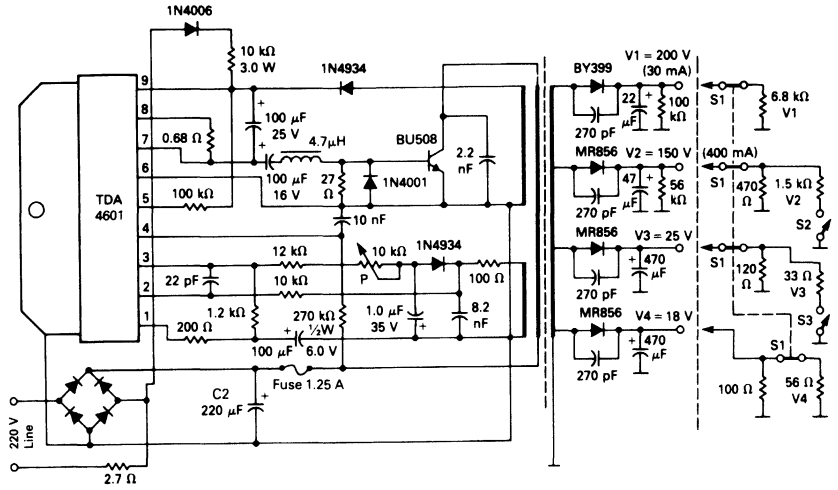
In spite of regulation on the primary side, good voltage stability of the various secondary voltages is achieved even with large load changes.

For line voltage isolation and transformation to the desired secondary voltages, a transformer with ferrite core is used.

SPECIAL FEATURES OF THE FLYBACK CONVERTER POWER, SUPPLY USING THE TDA4601

- Direct driving of the power switching transistor
- Low starting current, defined starting behavior also at slowly rising line voltage
- Short circuit proof and open-loop resistant circuit. In both cases a power of only 6.0 to 10 W is consumed. Linear foldback characteristic at overload.
- Automatic restart after elimination of the overload.
- Efficiency of more than 80% at an output power of 40 to 100 W.
- Frequency of oscillation between 20 kHz (100 W) and 70 kHz (without load).
- Simple RF1 suppression
- Good regulation of load current and line voltage variations. At a line voltage variation between 170 and 240 V the output voltage of 150 V will change approximately 2.0 V.

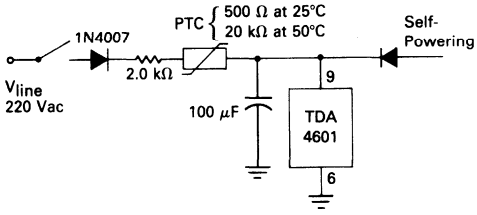
FIGURE 7 — TYPICAL APPLICATION



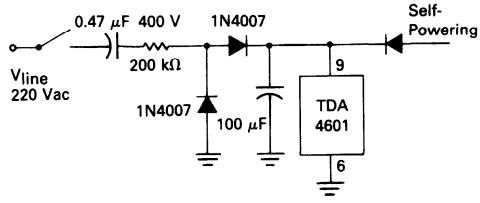
Note:
P is used to adjust the secondary voltage
C2 must be discharged before IC change

FIGURE 8 — ALTERNATIVE START-UP CIRCUIT

A. Thermal Kick Starter



B. Lossless Start-Up Pump



Note: For more application information refer to ANE002

MOTOROLA

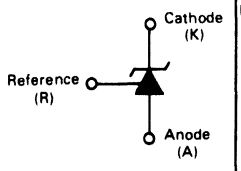
TL431,A Series

Specifications and Applications Information

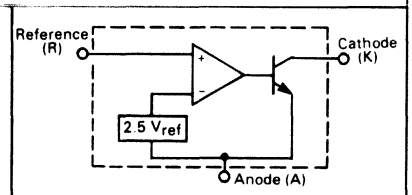
PROGRAMMABLE PRECISION REFERENCES

The TL431,A integrated circuits are three-terminal programmable shunt regulator diodes. These monolithic IC voltage references operate as a low temperature coefficient zener which is programmable from V_{ref} to 36 volts with two external resistors. These devices exhibit a wide operating current range of 1.0 to 100 mA with a typical dynamic impedance of 0.22 Ω. The characteristics of these references make them excellent replacements for zener diodes in many applications such as digital voltmeters, power supplies, and op amp circuitry. The 2.5 volt reference makes it convenient to obtain a stable reference from 5.0 volt logic supplies, and since the TL431,A operates as a shunt regulator, it can be used as either a positive or negative voltage reference.

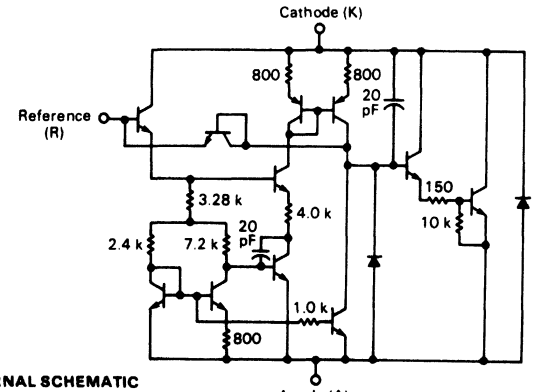
- Programmable Output Voltage to 36 Volts
- Voltage Reference Tolerance: ± 1.0% (TL431,A)
- Low Dynamic Output Impedance, 0.22 Ω Typical
- Sink Current Capability of 1.0 to 100 mA
- Equivalent Full-Range Temperature Coefficient of 50 ppm/°C Typical
- Temperature Compensated for Operation over Full Rated Operating Temperature Range
- Low Output Noise Voltage



SYMBOL



FUNCTIONAL BLOCK DIAGRAM

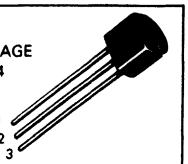


INTERNAL SCHEMATIC
Component values are nominal

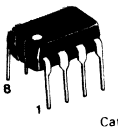
PROGRAMMABLE PRECISION REFERENCES

SILICON MONOLITHIC INTEGRATED CIRCUITS

LP SUFFIX
PLASTIC PACKAGE
CASE 29-04

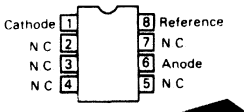


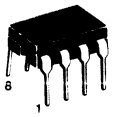
Pin 1. Reference
2. Anode
3. Cathode



P SUFFIX
PLASTIC PACKAGE
CASE 626-05

(Top View)





JG SUFFIX
CERAMIC PACKAGE
CASE 693-02

D SUFFIX
PLASTIC PACKAGE
CASE 751-03
SOP-8

PIN 1. CATHODE
2. ANODE
3. ANODE
4. N.C.
5. N.C.
6. ANODE
7. ANODE
8. REFERENCE

SOP-8 is an internally modified SO-8 Package. Pins 2, 3, 6 and 7 are electrically common to the die attach flag. This internal lead frame modification decreases package thermal resistance and increases power dissipation capability when appropriately mounted on a printed circuit board. SOP-8 conforms to all external dimensions of the standard SO-8 Package.

ORDERING INFORMATION

Device	Temperature Range	Package
TL431CLP,ACLP	0 to +70°C	Plastic TO-92
TL431CP,ACP	0 to +70°C	Plastic DIP
TL431CD,ACD	0 to +70°C	SOP-8
TL431CJG	0 to +70°C	Ceramic DIP
TL431ILP,AILP	−40 to +85°C	Plastic TO-92
TL431IP,AIP	−40 to +85°C	Plastic DIP
TL431IJG	−40 to +85°C	Ceramic DIP
TL431MJG	−55 to +125°C	Ceramic DIP

MAXIMUM RATINGS (Full operating ambient temperature range applies unless otherwise noted.)

Rating	Symbol	Value	Unit
Cathode To Anode Voltage	V_{KA}	37	V
Cathode Current Range, Continuous	I_K	−100 to +150	mA
Reference Input Current Range, Continuous	I_{ref}	−0.05 to +10	mA
Operating Junction Temperature	T_J	150	°C
Operating Ambient Temperature Range TL431M TL431I, TL431AI TL431C, TL431AC	T_A	 −55 to +125 −40 to +85 0 to +70	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C
Total Power Dissipation @ T_A = 25°C Derate above 25°C Ambient Temperature D, LP Suffix Plastic Package P Suffix Plastic Package JG Suffix Ceramic Package	P_D	 0.70 1.10 1.25	W
Total Power Dissipation @ T_C = 25°C Derate above 25°C Case Temperature D, LP Suffix Plastic Package P Suffix Plastic Package JG Suffix Ceramic Package	P_D	 1.5 3.0 3.3	W

THERMAL CHARACTERISTICS

Characteristics	Symbol	D, LP Suffix Package	P Suffix Package	JG Suffix package	Unit
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	178	114	100	°C/W
Thermal Resistance, Junction to Case	$R_{\theta JC}$	83	41	38	°C/W

RECOMMENDED OPERATING CONDITIONS

Condition/Value	Symbol	Min	Max	Unit
Cathode To Anode Voltage	V_{KA}	V_{ref}	36	V
Cathode Current	I_K	1.0	100	mA

ELECTRICAL CHARACTERISTICS (Ambient temperature at 25°C unless otherwise noted)

Characteristic	Symbol	TL431M			TL431I			TL431C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Reference Input Voltage (Figure 1) V_{KA} = V_{ref}, I_K = 10 mA T_A = +25°C T_A = T_{low} to T_{high} (Note 1)	V_{ref}	 2.440 2.396	 2.495 —	 2.550 2.594	 2.440 2.410	 2.495 —	 2.550 2.580	 2.440 2.423	 2.495 —	 2.550 2.567	V
Reference Input Voltage Deviation Over Temperature Range (Figure 1, Note 1, 2, 4) V_{KA} = V_{ref}, I_K = 10 mA	ΔV_{ref}	—	15	44	—	7.0	30	—	3.0	17	mV
Ratio of Change in Reference Input Voltage to Change in Cathode to Anode Voltage I_K = 10 mA (Figure 2), ΔV_{KA} = 10 V to V_{ref} ΔV_{KA} = 36 V to 10 V	$\frac{\Delta V_{ref}}{\Delta V_{KA}}$	 — —	 −1.4 −1.0	 −2.7 −2.0	 — —	 −1.4 −1.0	 −2.7 −2.0	 — —	 −1.4 −1.0	 −2.7 −2.0	mV/V
Reference Input Current (Figure 2) I_K = 10 mA, R1 = 10 k, R2 = ∞ T_A = +25°C T_A = T_{low} to T_{high} (Note 1)	I_{ref}	 — —	 1.8 —	 4.0 7.0	 — —	 1.8 —	 4.0 6.5	 — —	 1.8 —	 4.0 5.2	μA
Reference Input Current Deviation Over Temperature Range (Figure 2, Note 1, 4) I_K = 10 mA, R1 = 10 k, R2 = ∞	ΔI_{ref}	—	1.0	3.0	—	0.8	2.5	—	0.4	1.2	μA
Minimum Cathode Current For Regulation V_{KA} = V_{ref} (Figure 1)	I_{min}	—	0.5	1.0	—	0.5	1.0	—	0.5	1.0	mA
Off-State Cathode Current (Figure 3) V_{KA} = 36 V, V_{ref} = 0 V	I_{off}	—	2.6	1000	—	2.6	1000	—	2.6	1000	nA
Dynamic Impedance (Figure 1, Note 3) V_{KA} = V_{ref}, ΔI_K = 1.0 mA to 100 mA f ≤ 1.0 kHz	$\lvert Z_{ka} \rvert$	—	0.22	0.5	—	0.22	0.5	—	0.22	0.5	Ω

ELECTRICAL CHARACTERISTICS (Ambient temperature at 25°C unless otherwise noted)

Characteristic	Symbol	TL431AI			TL431AC			Unit
		Min	Typ	Max	Min	Typ	Max	
Reference Input Voltage (Figure 1) $V_{KA} = V_{ref}$, I_K = 10 mA	V_{ref}							V
T_A = +25°C		2.470	2.495	2.520	2.470	2.495	2.520	
$T_A = T_{low}$ to T_{high} (Note 4)		2.440	—	2.550	2.453	—	2.537	
Reference Input Voltage Deviation Over Temperature Range (Figure 1, Note 1, 2) $V_{KA} = V_{ref}$, I_K = 10 mA	ΔV_{ref}	—	7.0	30	—	3.0	17	mV
Ratio of Change in Reference Input Voltage to Change in Cathode to Anode Voltage I_K = 10 mA (Figure 2), ΔV_{KA} = 10 V to V_{ref}	$\frac{\Delta V_{ref}}{\Delta V_{KA}}$	—	−1.4	−2.7	—	−1.4	−2.7	mV/V
ΔV_{KA} = 36 V to 10 V		—	−1.0	−2.0	—	−1.0	−2.0	
Reference Input Current (Figure 2) I_K = 10 mA, R1 = 10 k, R2 = ∞	I_{ref}							μA
T_A = +25°C		—	1.8	4.0	—	1.8	4.0	
$T_A = T_{low}$ to T_{high} (Note 1)		—	—	6.5	—	—	5.2	
Reference Input Current Deviation Over Temperature Range (Figure 2, Note 1) I_K = 10 mA, R1 = 10 k, R2 = ∞	ΔI_{ref}	—	0.8	2.5	—	0.4	1.2	μA
Minimum Cathode Current For Regulation $V_{KA} = V_{ref}$ (Figure 1)	I_{min}	—	0.5	1.0	—	0.5	1.0	mA
Off-State Cathode Current (Figure 3) V_{KA} = 36 V, V_{ref} = 0 V	I_{off}	—	2.6	1000	—	2.6	1000	nA
Dynamic Impedance (Figure 1, Note 3) $V_{KA} = V_{ref}$, ΔI_K = 1.0 mA to 100 mA f ≤ 1.0 kHz	$\lvert Z_{ka} \rvert$	—	0.22	0.5	—	0.22	0.5	Ω

Note 1:
T_{low} = −55°C for TL431MJG
= −40°C for TL431AIP, TL431AILP, TL431IP, TL431ILP, TL431IJG
= 0°C for TL431ACP, TL431ACLP, TL431CP, TL431CLP, TL431CJG, TL431CD, TL431ACD

T_{high} = +125°C for TL431MJG
= +85°C for TL431AIP, TL431AILP, TL431IP, TL431ILP, TL431IJG
= +70°C for TL431ACP, TL431ACLP, TL431CP, TL431CLP, TL431CJG, TL431CD, TL431ACD

FIGURE 1 — TEST CIRCUIT FOR $V_{KA} = V_{ref}$

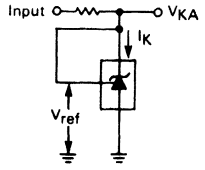


FIGURE 2 — TEST CIRCUIT FOR $V_{KA} > V_{ref}$

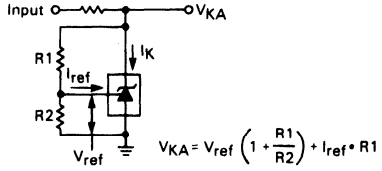
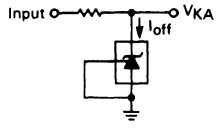
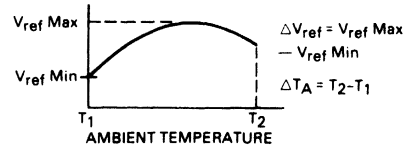


FIGURE 3 — TEST CIRCUIT FOR I_{off}



Note 2:
The deviation parameter ΔV_{ref} is defined as the differences between the maximum and minimum values obtained over the full operating ambient temperature range that applies.



The average temperature coefficient of the reference input voltage, αV_{ref}, is defined as:

$$\alpha V_{ref} \frac{ppm}{°C} = \frac{\left(\frac{\Delta V_{ref}}{V_{ref} @ 25°C}\right) \times 10^6}{\Delta T_A} = \frac{\Delta V_{ref} \times 10^6}{\Delta T_A (V_{ref} @ 25°C)}$$

αV_{ref} can be positive or negative depending on whether V_{ref} Min or V_{ref} Max occurs at the lower ambient temperature. (Refer to Figure 6)

Example: ΔV_{ref} = 8.0 mV and slope is positive, V_{ref} @ 25°C = 2.495 V, ΔT_A = 70°C

$$\alpha V_{ref} = \frac{0.008 \times 10^6}{70\,(2.495)} = 45.8\ ppm/°C$$

Note 3:

The dynamic impedance Z_{ka} is defined as:

$$|Z_{ka}| = \frac{\Delta V_{KA}}{\Delta I_K}$$

When the device is programmed with two external resistors, R1 and R2, (refer to Figure 2) the total dynamic impedance of the circuit is defined as:

$$|Z_{ka}'| \approx |Z_{ka}| \left(1 + \frac{R1}{R2}\right)$$

Note 4:

This test is not applicable to surface mount (D suffix) devices.

FIGURE 4 — CATHODE CURRENT versus CATHODE VOLTAGE

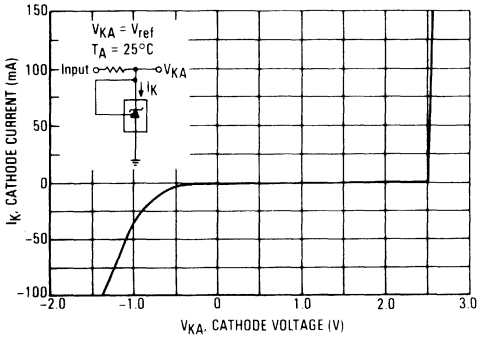


FIGURE 5 — CATHODE CURRENT versus CATHODE VOLTAGE

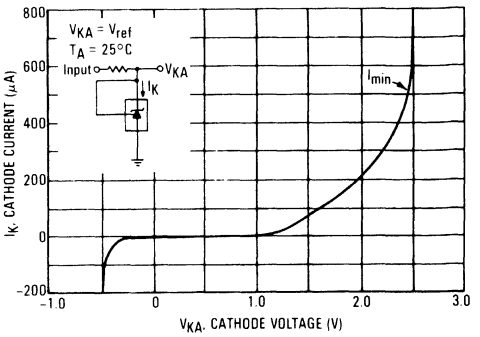


FIGURE 6 — REFERENCE INPUT VOLTAGE versus AMBIENT TEMPERATURE

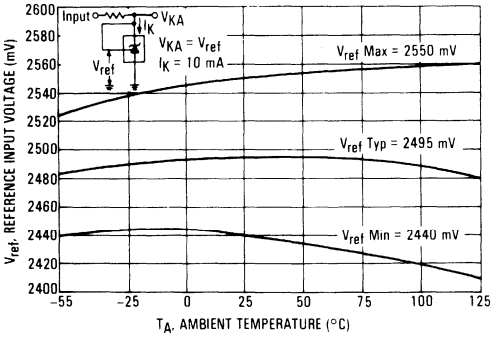


FIGURE 7 — REFERENCE INPUT CURRENT versus AMBIENT TEMPERATURE

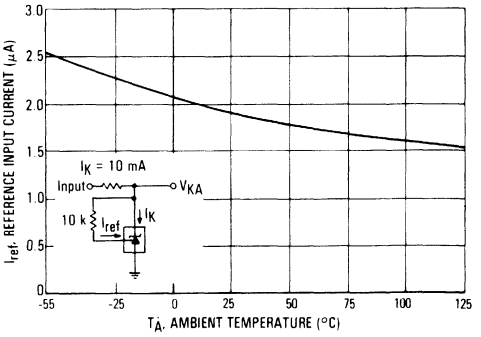


FIGURE 8 — CHANGE IN REFERENCE INPUT VOLTAGE versus CATHODE VOLTAGE

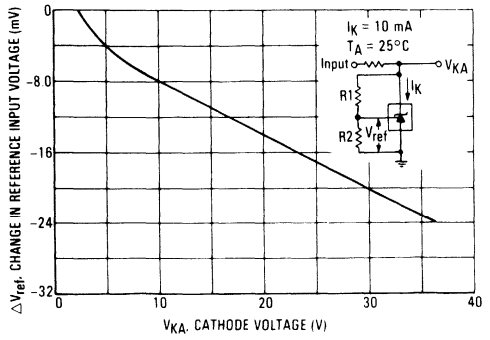


FIGURE 9 — OFF-STATE CATHODE CURRENT versus AMBIENT TEMPERATURE

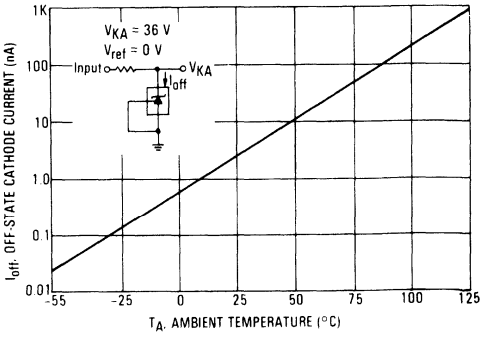


FIGURE 10 — DYNAMIC IMPEDANCE versus FREQUENCY

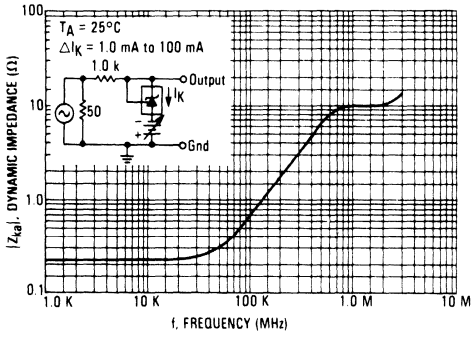


FIGURE 11 — DYNAMIC IMPEDANCE versus AMBIENT TEMPERATURE

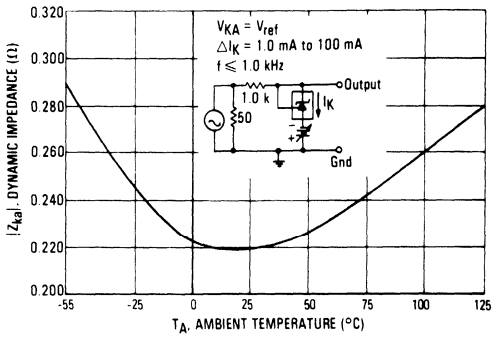


FIGURE 12 — OPEN LOOP VOLTAGE GAIN versus FREQUENCY

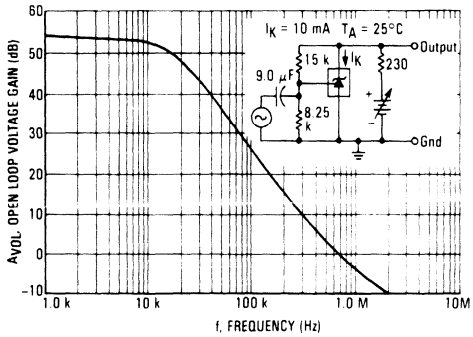


FIGURE 13 — SPECTRAL NOISE DENSITY

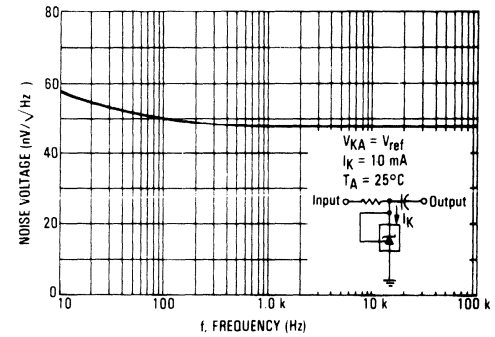


FIGURE 14 — PULSE RESPONSE

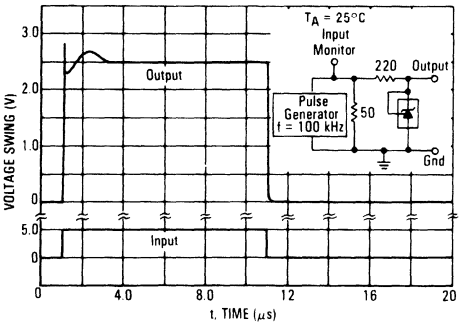


FIGURE 15 — STABILITY BOUNDARY CONDITIONS

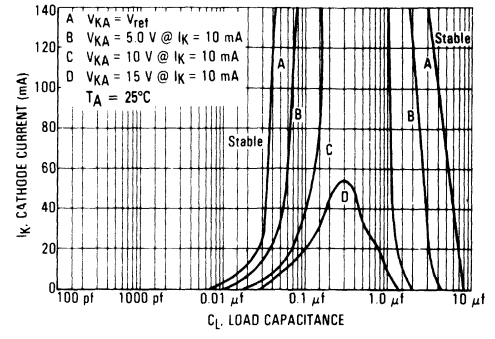


FIGURE 16 — TEST CIRCUIT FOR CURVE A OF STABILITY BOUNDARY CONDITIONS

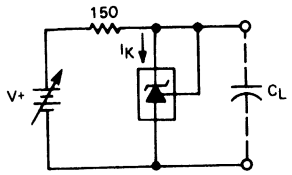
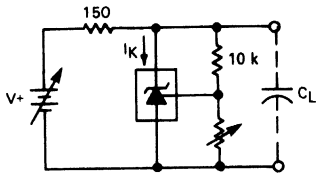
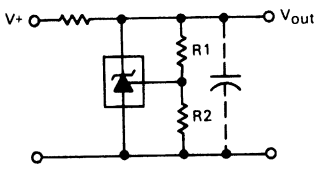


FIGURE 17 — TEST CIRCUIT FOR CURVES B, C, AND D OF STABILITY BOUNDARY CONDITIONS



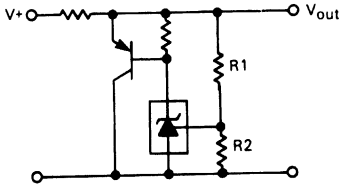
TYPICAL APPLICATIONS

FIGURE 18 — SHUNT REGULATOR



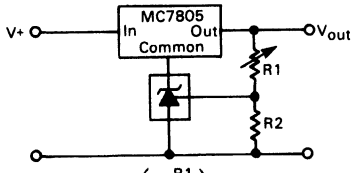
$$V_{out} = \left(1 + \frac{R1}{R2}\right) V_{ref}$$

FIGURE 19 — HIGH CURRENT SHUNT REGULATOR



$$V_{out} = \left(1 + \frac{R1}{R2}\right) V_{ref}$$

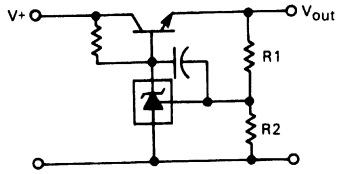
FIGURE 20 — OUTPUT CONTROL OF A THREE-TERMINAL FIXED REGULATOR



$$V_{out} = \left(1 + \frac{R1}{R2}\right) V_{ref}$$

V_{out} Min = V_{ref} + 5.0 V

FIGURE 21 — SERIES PASS REGULATOR



$$V_{out} = \left(1 + \frac{R1}{R2}\right) V_{ref}$$

V_{out} Min = V_{ref} + V_{be}

FIGURE 22 — CONSTANT CURRENT SOURCE

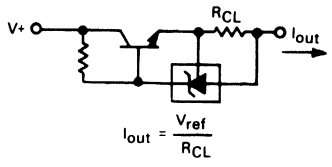


FIGURE 23 — CONSTANT CURRENT SINK

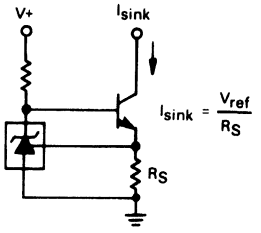


FIGURE 24 — TRIAC CROWBAR

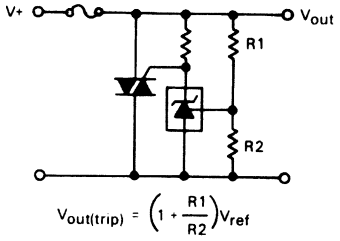


FIGURE 25 — SCR CROWBAR

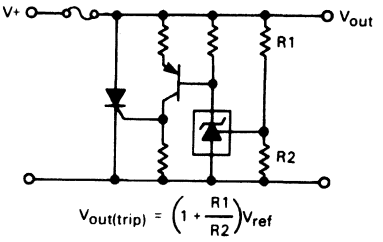
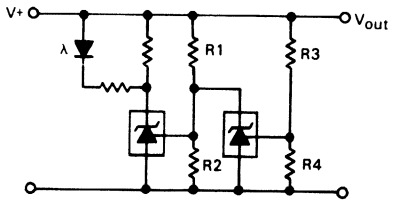


FIGURE 26 — VOLTAGE MONITOR

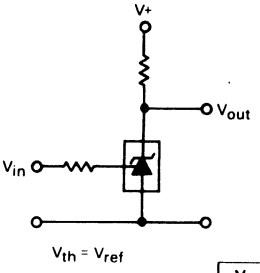


L.E.D. indicator is 'on' when V+ is between the upper and lower limits.

$$\text{Lower Limit} = \left(1 + \frac{R1}{R2}\right)V_{ref}$$

$$\text{Upper Limit} = \left(1 + \frac{R3}{R4}\right)V_{ref}$$

FIGURE 27 — SINGLE-SUPPLY COMPARATOR WITH TEMPERATURE-COMPENSATED THRESHOLD



V_{in}	V_{out}
$<V_{ref}$	V+
$>V_{ref}$	≈ 2.0 V

FIGURE 28 — LINEAR OHMMETER

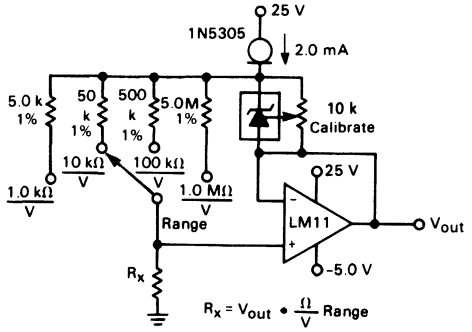


FIGURE 29 — SIMPLE 400 mW PHONO AMPLIFIER

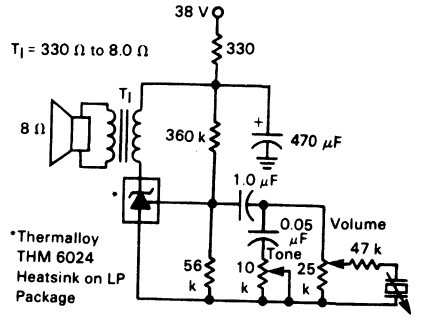
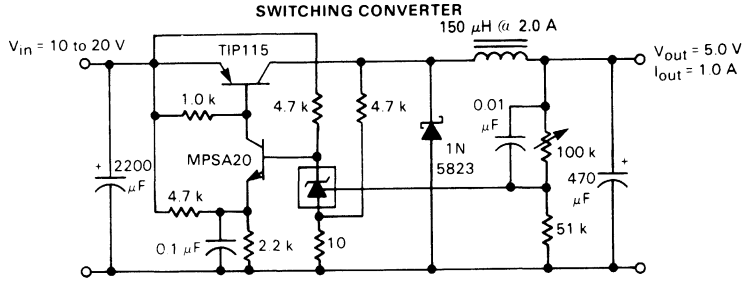


FIGURE 30 — HIGH EFFICIENCY STEP-DOWN SWITCHING CONVERTER



TEST	CONDITIONS	RESULTS
Line Regulation	V_{in} = 10 V to 20 V, I_O = 1.0 A	53 mV (1.1%)
Load Regulation	V_{in} = 15 V, I_O = 0A to 1.0 A	25 mV (0.5%)
Output Ripple	V_{in} = 10 V, I_O = 1.0 A	50 mV_{p-p} P.A.R.D.
Output Ripple	V_{in} = 20 V, I_O = 1.0 A	100 mV_{p-p} P.A.R.D.
Efficiency	V_{in} = 15 V, I_O = 1.0 A	82%

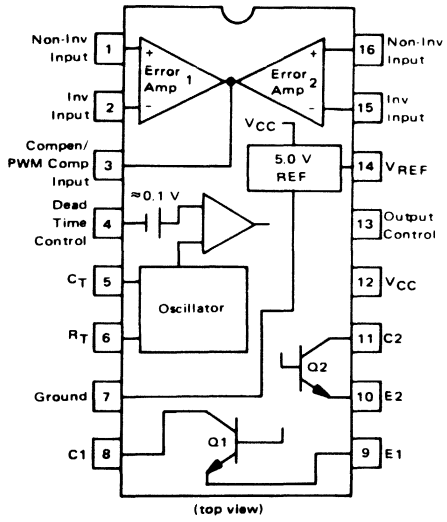
MOTOROLA

TL494

SWITCHMODE PULSE WIDTH MODULATION CONTROL CIRCUITS

The TL494 is a fixed frequency, pulse width modulation control circuit designed primarily for Switchmode power supply control. This device features:

- Complete Pulse Width Modulation Control Circuitry
- On-Chip Oscillator With Master Or Slave Operation
- On-Chip Error Amplifiers
- On-Chip 5 Volt Reference
- Adjustable Dead-Time Control
- Uncommitted Output Transistors Rated to 500 mA Source Or Sink
- Output Control For Push-Pull Or Single-Ended Operation
- Undervoltage Lockout

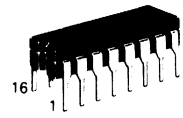


(top view)

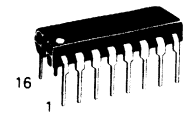
The TL494C is specified over the commercial operating range of 0°C to 70°C. The TL494I is specified over the industrial range of −25°C to 85°C. The TL494M is specified over the full military range of −55°C to 125°C.

SWITCHMODE PULSE WIDTH MODULATION CONTROL CIRCUITS

SILICON MONOLITHIC INTEGRATED CIRCUITS



J SUFFIX
CERAMIC PACKAGE
CASE 620-10



N SUFFIX
PLASTIC PACKAGE
CASE 648-08

ORDERING INFORMATION

Device	Temperature Range	Package
TL494CN	0° to +70°C	Plastic DIP
TL494CJ	0° to +70°C	Ceramic DIP
TL494IN	−25° to +85°C	Plastic DIP
TL494IJ	−25° to +85°C	Ceramic DIP
TL494MJ	−55° to +125°C	Ceramic DIP

FIGURE 1 — BLOCK DIAGRAM

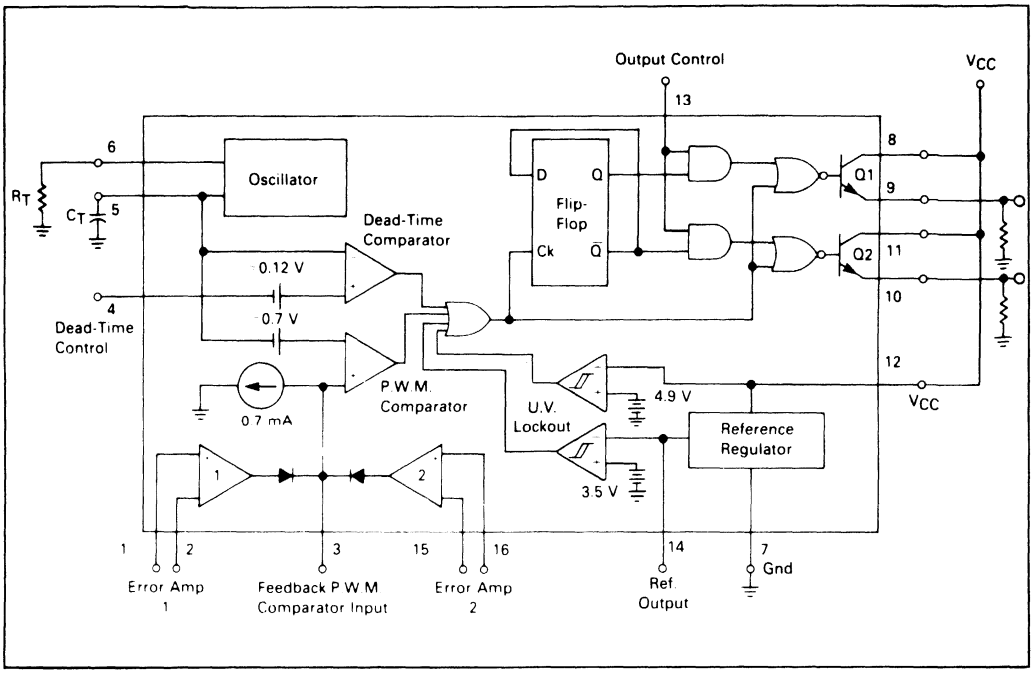
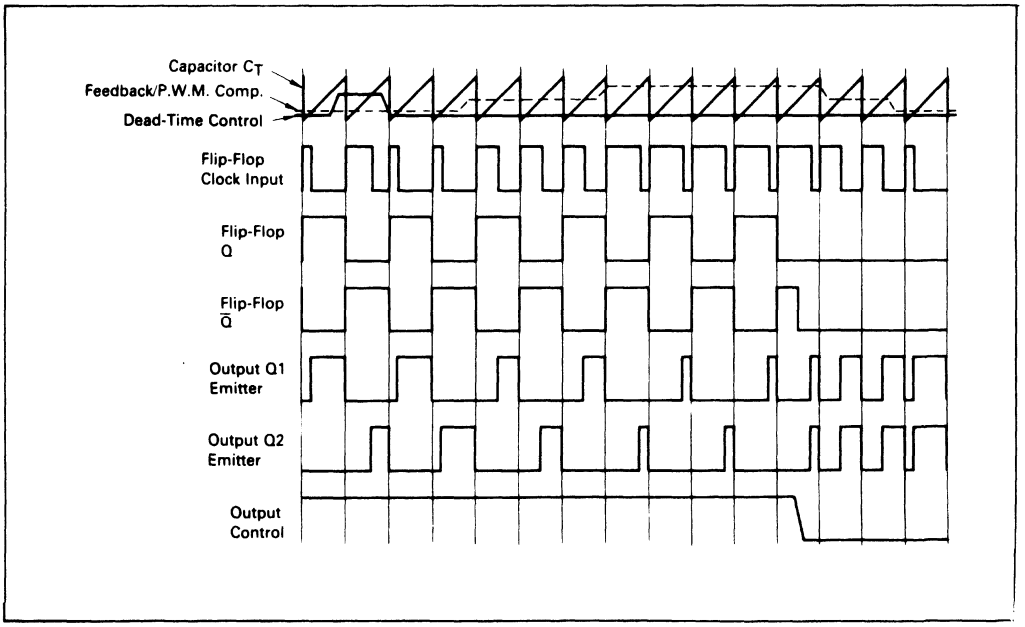


FIGURE 2 — TIMING DIAGRAM



MAXIMUM RATINGS (Full operating ambient temperature range applies unless otherwise noted)

Rating	Symbol	TL494C	TL494I	TL494M	Unit
Power Supply Voltage	V_{CC}	42	42	42	V
Collector Output Voltage	V_{C1}, V_{C2}	42	42	42	V
Collector Output Current (each transistor) (1)	I_{C1}, I_{C2}	500	500	500	mA
Amplifier Input Voltage Range	V_{IR}	−0.3 to 42	−0.3 to 42	−0.3 to 42	V
Power Dissipation @ $T_A \leq 45°C$	P_D	1000	1000	1000	mW
Operating Junction Temperature Plastic Package Ceramic Package	T_J	 125 150	 125 150	 — 150	°C °C °C
Operating Ambient Temperature Range	T_A	0 to 70	−25 to 85	−55 to 125	°C
Storage Temperature Range Plastic Package Ceramic Package	T_{stg}	 −55 to 125 −65 to 150	 −55 to 125 −65 to 150	 — −65 to 150	°C

NOTE 1: Maximum thermal limits must be observed.

THERMAL CHARACTERISTICS

Characteristics	Symbol	N Suffix Plastic Package	J Suffix Ceramic Package	Unit
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	80	100	°C/W
Derating Ambient Temperature	T_A	45	50	°C

RECOMMENDED OPERATING CONDITIONS

Condition/Value	Symbol	TL494			Unit
		Min	Typ	Max	
Power Supply Voltage	V_{CC}	7.0	15	40	V
Collector Output Voltage	V_{C1}, V_{C2}	—	30	40	V
Collector Output Current (each transistor)	I_{C1}, I_{C2}	—	—	200	mA
Amplifier Input Voltage	V_{in}	−0.3	—	V_{CC} − 2.0	V
Current Into Feedback Terminal	I_{fb}	—	—	0.3	mA
Reference Output Current	I_{ref}	—	—	10	mA
Timing Resistor	R_T	1.8	30	500	kΩ
Timing Capacitor	C_T	0.0047	0.001	10	μF
Oscillator Frequency	f_{osc}	1.0	40	200	kHz

ELECTRICAL CHARACTERISTICS (V_{CC} = 15 V, C_T = 0.01 μF, R_T = 12 kΩ unless otherwise noted.)
For typical values T_A = 25°C, for min/max values T_A is the operating ambient temperature range that applies unless otherwise noted.

*Characteristic	Symbol	TL494C,I			TL494M			Unit
		Min	Typ	Max	Min	Typ	Max	
REFERENCE SECTION								
Reference Voltage (I_O = 1.0 mA)	V_{ref}	4.75	5.0	5.25	4.75	5.0	5.25	V
Line Regulation (V_{CC} = 7.0 V to 40 V)	Reg_{line}	—	2.0	25	—	2.0	25	mV
Load Regulation (I_O = 1.0 mA to 10 mA)	Reg_{load}	—	3.0	15	—	3.0	15	mV
Short-Circuit Output Current (V_{ref} = 0 V)	I_{SC}	15	35	75	15	35	75	mA

ELECTRICAL CHARACTERISTICS (V_{CC} = 15 V, C_T = 0.01 μF, R_T = 12 kΩ unless otherwise noted.)
For typical values T_A = 25°C, for min/max values T_A is the operating ambient temperature range that applies unless otherwise noted.

Characteristic	Symbol	TL494C,I			TL494M			Unit
		Min	Typ	Max	Min	Typ	Max	
OUTPUT SECTION								
Collector Off-State Current (V_{CC} = 40 V, V_{CE} = 40 V)	$I_{C(off)}$	—	2.0	100	—	2.0	100	μA
Emitter Off-State Current (V_{CC} = 40 V, V_C = 40 V, V_E = 0 V)	$I_{E(off)}$	—	—	−100	—	—	−150	μA
Collector-Emitter Saturation Voltage (2) Common-Emitter (V_E = 0 V, I_C = 200 mA)	$V_{SAT(C)}$	—	1.1	1.3	—	1.1	1.5	V
Emitter-Follower (V_C = 15 V, I_E = −200 mA)	$V_{SAT(E)}$	—	1.5	2.5	—	1.5	2.5	V
Output Control Pin Current Low State (V_{OC} ≤ 0.4 V)	I_{OCL}	—	10	—	—	10	—	μA
High State (V_{OC} = V_{ref})	I_{OCH}	—	0.2	3.5	—	0.2	3.5	mA
Output Voltage Rise Time Common-Emitter (See Figure 13)	t_r	—	100	200	—	100	200	ns
Emitter-Follower (See Figure 14)		—	100	200	—	100	200	ns
Output Voltage Fall Time Common-Emitter (See Figure 13)	t_f	—	25	100	—	25	100	ns
Emitter-Follower (See Figure 14)		—	40	100	—	40	100	ns

Characteristic	Symbol	TL494			Unit
		Min	Typ	Max	
ERROR AMPLIFIER SECTIONS					
Input Offset Voltage (V_O (Pin 3) = 2.5 V)	V_{IO}	—	2.0	10	mV
Input Offset Current (V_O (Pin 3) = 2.5 V)	I_{IO}	—	5.0	250	nA
Input Bias Current (V_O (Pin 3) = 2.5 V)	I_{IB}	—	−0.1	−1.0	μA
Input Common-Mode Voltage Range (V_{CC} = 40 V, T_A = 25°C)	V_{ICR}	−0.3 to V_{CC} − 2.0	—	—	V
Open-Loop Voltage Gain (ΔV_O = 3.0 V, V_O = 0.5 to 3.5 V, R_L = 2.0 kΩ)	A_{VOL}	70	95	—	dB
Unity-Gain Crossover Frequency (V_O = 0.5 to 3.5 V, R_L = 2.0 kΩ)	f_C	—	350	—	kHz
Phase Margin at Unity-Gain (V_O = 0.5 to 3.5 V, R_L = 2.0 kΩ)	θm	—	65	—	deg.
Common-Mode Rejection Ratio (V_{CC} = 40 V)	CMRR	65	90		dB
Power Supply Rejection Ratio (ΔV_{CC} = 33 V, V_O = 2.5 V, R_L = 2.0 kΩ)	PSRR	—	100	—	dB
Output Sink Current (V_O (Pin 3) = 0.7 V)	I_O^-	0.3	0.7	—	mA
Output Source Current (V_O (Pin 3) = 3.5 V)	I_O^+	−2.0	−4.0	—	mA

NOTE 2: Low duty cycle pulse techniques are used during test to maintain junction temperature as close to ambient temperatures as possible.

ELECTRICAL CHARACTERISTICS (V_{CC} = 15 V, C_T = 0.01 μF, R_T = 12 kΩ unless otherwise noted.)
For typical values T_A = 25°C, for min/max values T_A is the operating ambient temperature range that applies unless otherwise noted.

Characteristic	Symbol	TL494			Unit
		Min	Typ	Max	
PWM COMPARATOR SECTION (Test Circuit Figure 12)					
Input Threshold Voltage (Zero duty cycle)	V_{TH}	—	3.5	4.5	V
Input Sink Current ($V_{(Pin\ 3)}$ = 0.7 V)	I_I-	0.3	0.7	—	mA
DEAD-TIME CONTROL SECTION (Test Circuit Figure 12)					
Input Bias Current (Pin 4) ($V_{Pin\ 4}$) = 0 to 5.25 V)	I_{IB} (DT)	—	−2.0	−10	μA
Maximum Duty Cycle, Each Output, Push-Pull Mode ($V_{Pin\ 4}$ = 0 V, C_T = 0.01 μF, R_T = 12 kΩ) ($V_{Pin\ 4}$ = 0 V, C_T = 0.001 μF, R_T = 30 kΩ)	DC_{max}	 45 —	 48 45	 50 50	%
Input Threshold Voltage (Pin 4) (Zero Duty Cycle) (Maximum Duty Cycle)	V_{TH}	 — 0	 2.8 —	 3.3 —	V
OSCILLATOR SECTION					
Frequency (C_T = 0.001 μF, R_T = 30 kΩ)	f_{osc}	—	40	—	kHz
Standard Deviation of Frequency* (C_T = 0.001 μF, R_T = 30 kΩ)	σf_{osc}	—	3.0	—	%
Frequency Change with Voltage (V_{CC} = 7.0 V to 40 V, T_A = 25°C)	Δf_{osc} (ΔV)	—	0.1	—	%
Frequency Change with Temperature (ΔT_A = T_{low} to T_{high}) (C_T = 0.01 μF, R_T = 12 kΩ)	Δf_{osc} (ΔT)	—	—	12	%
UNDERVOLTAGE LOCKOUT SECTION					
Turn-On Threshold (V_{CC} Increasing, I_{ref} = 1.0 mA)	V_{th}	5.5	6.43	7.0	V
TOTAL DEVICE					
Standby Supply Current (Pin 6 at V_{ref}, All Other Inputs and Outputs Open) (V_{CC} = 15 V) (V_{CC} = 40 V)	I_{CC}	 — —	 5.5 7.0	 10 15	mA
Average Supply Current ($V_{(Pin\ 4)}$ = 2.0 V) (See Figure 12) (C_T = 0.01 μF, R_T = 12 kΩ, V_{CC} = 15 V)	—	—	7.0	—	mA

* Standard deviation is a measure of the statistical distribution about the mean as derived from the formula, $\sigma = \sqrt{\frac{\sum_{n=1}^{N} (X_n - \bar{X})^2}{N-1}}$

FIGURE 4 — OSCILLATOR FREQUENCY versus TIMING RESISTANCE

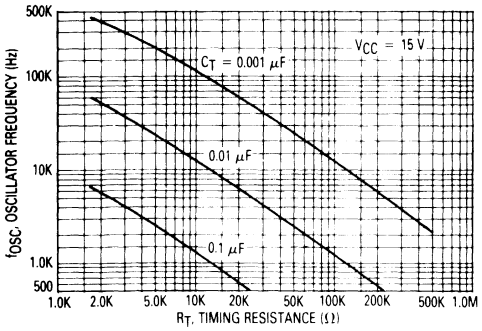


FIGURE 5 — OPEN-LOOP VOLTAGE GAIN AND PHASE versus FREQUENCY

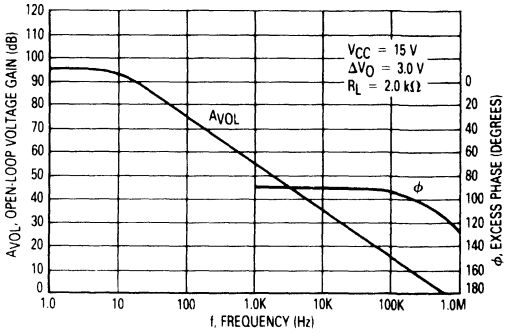


FIGURE 6 — PERCENT DEAD-TIME versus OSCILLATOR FREQUENCY

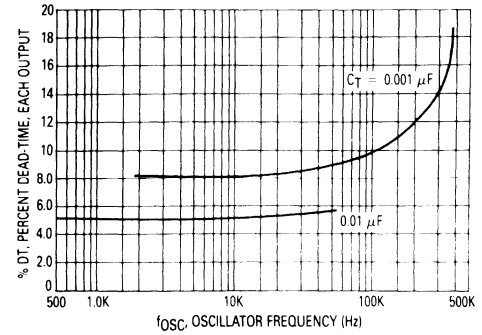


FIGURE 7 — PERCENT DUTY CYCLE versus DEAD-TIME CONTROL VOLTAGE

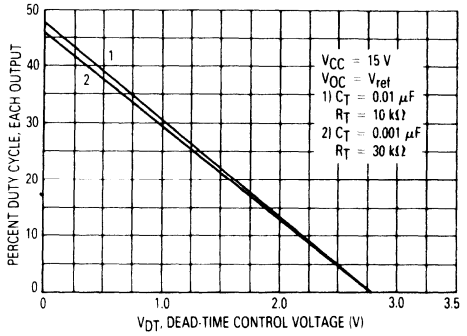


FIGURE 8 — EMITTER FOLLOWER CONFIGURATION OUTPUT SATURATION VOLTAGE versus EMITTER CURRENT

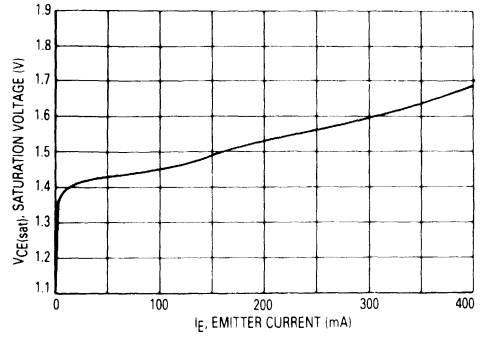


FIGURE 9 — COMMON EMITTER CONFIGURATION OUTPUT SATURATION VOLTAGE versus COLLECTOR CURRENT

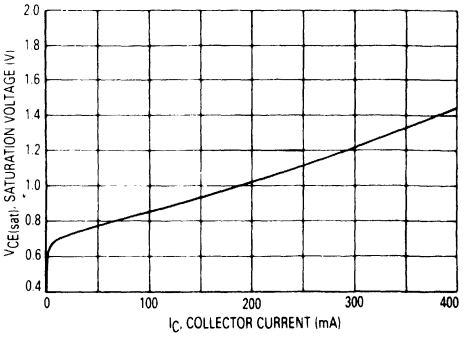


FIGURE 10 — STANDBY SUPPLY CURRENT versus SUPPLY VOLTAGE

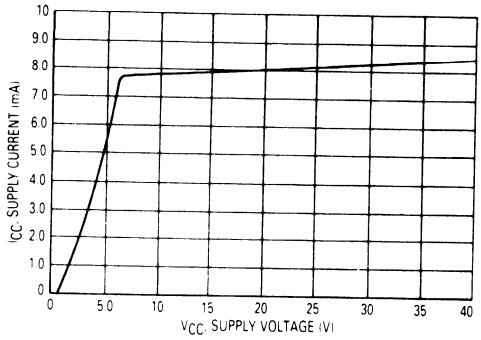


FIGURE 11 — ERROR AMPLIFIER CHARACTERISTICS

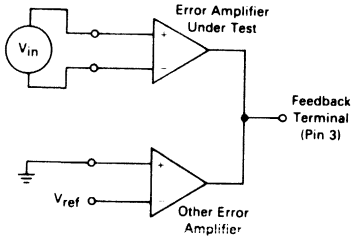


FIGURE 12 — DEAD-TIME AND FEEDBACK CONTROL TEST CIRCUIT

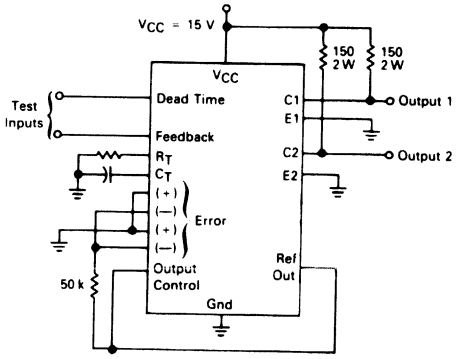


FIGURE 13 — COMMON-EMITTER CONFIGURATION TEST CIRCUIT AND WAVEFORM

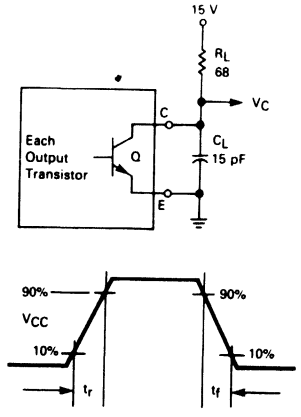


FIGURE 14 — EMITTER-FOLLOWER CONFIGURATION TEST CIRCUIT AND WAVEFORM

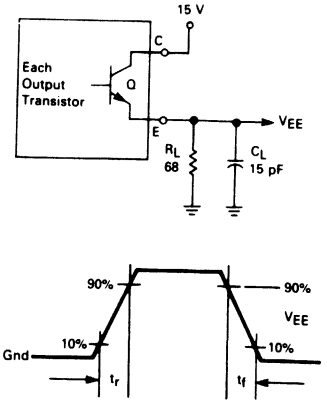
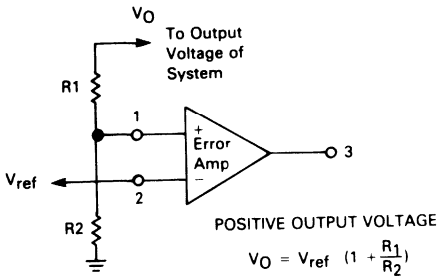


FIGURE 15 — ERROR-AMPLIFIER SENSING TECHNIQUES



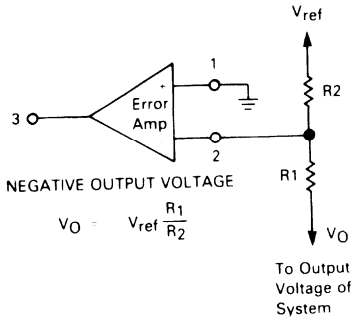


FIGURE 16 — DEAD-TIME CONTROL CIRCUIT

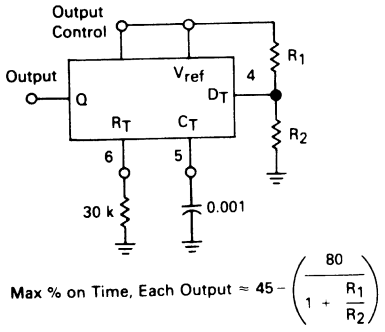


FIGURE 17 — SOFT-START CIRCUIT

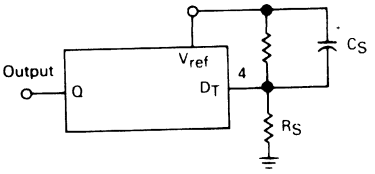
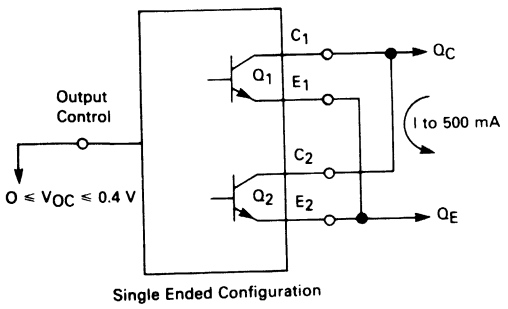


FIGURE 18 — OUTPUT CONNECTIONS FOR SINGLE-ENDED AND PUSH-PULL CONFIGURATIONS



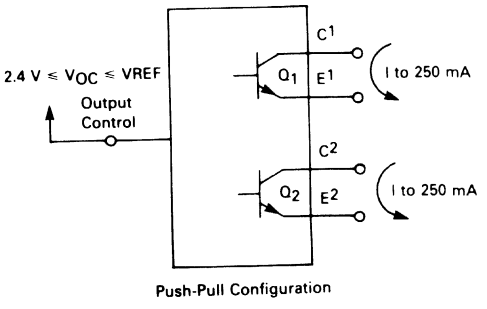


FIGURE 19 — SLAVING TWO OR MORE CONTROL CIRCUITS

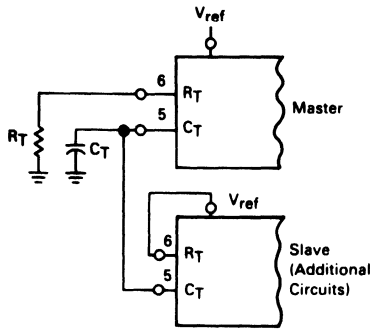


FIGURE 20 — OPERATION WITH V_{IN} > 40 V USING EXTERNAL ZENER

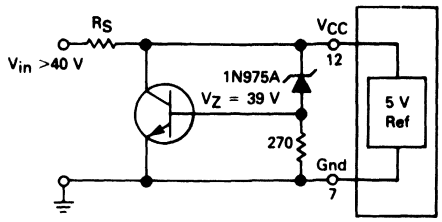
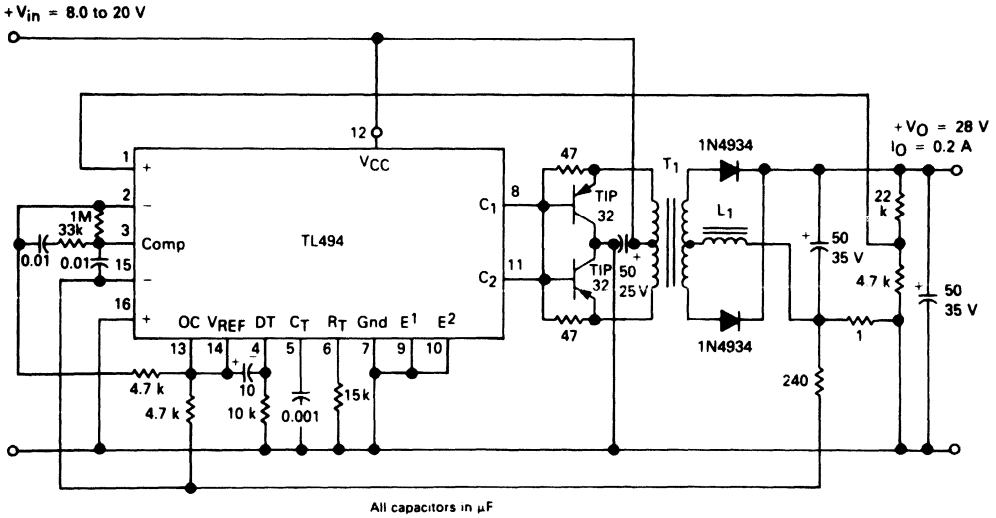


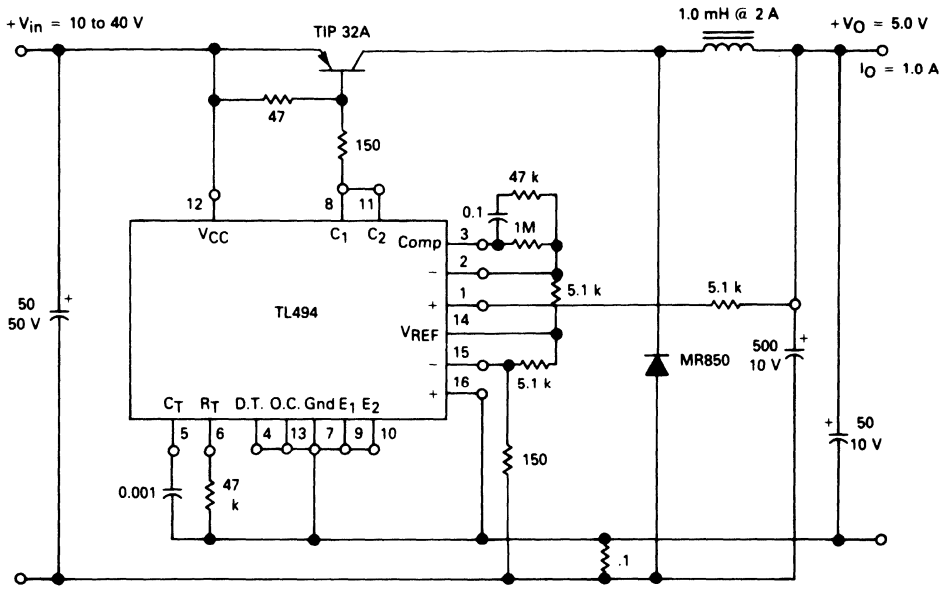
FIGURE 21 — PULSE-WIDTH MODULATED PUSH-PULL CONVERTER



L1 — 3.5 mH @ 0.3 A
T1 — Primary: 20T C.T. #28 AWG
Secondary: 120T C.T. #36 AWG
Core: Ferroxcube 1408P-L00-3C8

TEST	CONDITIONS	RESULTS
Line Regulation	V_{in} = 10 V to 40 V	14 mV 0.28%
Load Regulation	V_{in} = 28 V, I_O = 1 mA to 1 A	3.0 mV 0.06%
Output Ripple	V_{in} = 28 V, I_O = 1.0 A	65 mV P-P P.A.R.D.
Short Circuit Current	V_{in} = 28 V, R_L = 0.1 Ω	1.6 amps
Efficiency	V_{in} = 28 V, I_O = 1 A	71%

FIGURE 22 — PULSE-WIDTH MODULATED STEP-DOWN CONVERTER



TEST	CONDITIONS	RESULTS
Line Regulation	V_{in} = 8.0 to 40 V	3.0 mV 0.01%
Load Regulation	V_{in} = 12.6 V, I_O = 0.2 to 200 mA •	5.0 mV 0.02%
Output Ripple	V_{in} = 12.6 V, I_O = 200 mA	40 mV p-P P.A.R.D.
Short Circuit Current	V_{in} = 12.6 V, R_L = 0.1 Ω	250 mA
Efficiency	V_{in} = 12.6 V, I_O = 200 mA	72%

Description

The TL494 is a fixed-frequency pulse width modulation control circuit, incorporating the primary building blocks required for the control of a switching power supply. (See Figure 1.) An internal-linear sawtooth oscillator is frequency-programmable by two external components, R_T and C_T. The approximate oscillator frequency is determined by:

$$f_{osc} \approx \frac{1.1}{R_T \bullet C_T}$$

For more information refer to Figure 4.

Output pulse width modulation is accomplished by comparison of the positive sawtooth waveform across capacitor C_T to either of two control signals. The NOR gates, which drive output transistors Q1 and Q2, are enabled only when the flip-flop clock-input line is in its low state. This happens only during that portion of time when the sawtooth voltage is greater than the control signals. Therefore, an increase in control-signal amplitude causes a corresponding linear decrease of output pulse width. (Refer to the timing diagram shown in Figure 2.)

The control signals are external inputs that can be fed into the dead-time control, the error amplifier inputs, or the feedback input. The dead-time control comparator has an effective 120 mV input offset which limits the minimum output dead time to approximately the first 4% of the sawtooth-cycle time. This would result in a maximum duty cycle on a given output of 96% with the output control grounded, and 48% with it connected to the reference line. Additional dead time may be imposed on the output by setting the dead time-control input to a fixed voltage, ranging between 0 to 3.3 V.

The pulse width modulator comparator provides a means for the error amplifiers to adjust the output pulse width from the maximum percent on-time, established by the dead time control input, down to zero, as the voltage at the feedback pin varies from 0.5 to 3.5 V. Both error amplifiers have a common-mode input range from −0.3 V to (V_{CC} − 2 V), and may be used to sense power-supply output voltage and current. The error-amplifier outputs are active high and are ORed together at the non-inverting input of the pulse-width modulator comparator. With this configuration, the amplifier that demands minimum output on time, dominates control of the loop.

When capacitor C_T is discharged, a positive pulse is generated on the output of the dead-time comparator, which clocks the pulse-steering flip-flop and inhibits the output transistors, Q1 and Q2. With the output-control connected to the reference line, the pulse-steering flip-flop directs the modulated pulses to each of the two output transistors alternately for push-pull operation. The output frequency is equal to half that of the oscillator. Output drive can also be taken from Q1 or Q2, when single-ended operation with a maximum on-time of less than 50% is required. This is desirable when the output transformer has a ringback winding with a catch diode used for snubbing. When higher output-drive currents are required for single-ended operation, Q1 and Q2 may be connected in parallel, and the output-mode pin must be tied to ground to disable the flip-flop. The output frequency will now be equal to that of the oscillator.

The TL494 has an internal 5 V reference capable of sourcing up to 10 mA of load current for external bias circuits. The reference has an internal accuracy of ±1.5% with a typical thermal drift of less than 50 mV over an operating temperature range of 0 to 70°C.

FIGURE 3 — FUNCTIONAL TABLE

Input Output Control	Output Function	$\frac{f_{out}}{f_{osc}}$ =
Grounded	Single-ended P.W.M. at Q1 and Q2	1
At V_{ref}	Push-pull operation	0.5

MOTOROLA

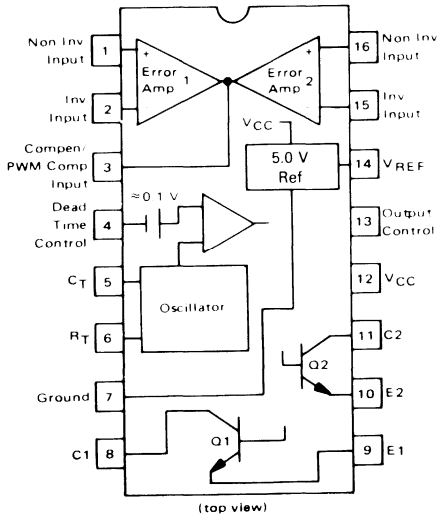
TL594

Advance Information

PRECISION SWITCHMODE PULSE WIDTH MODULATION CONTROL CIRCUIT

The TL594 is a fixed frequency, pulse width modulation control circuit designed primarily for Switchmode power supply control. This device features:

- Complete Pulse Width Modulation Control Circuitry
- On-Chip Oscillator With Master Or Slave Operation
- On-Chip Error Amplifiers
- On-Chip 5 Volt Reference, 1.5% Accuracy
- Adjustable Dead-Time Control
- Uncommitted Output Transistors Rated to 500 mA Source Or Sink
- Output Control For Push-Pull Or Single-Ended Operation
- Undervoltage Lockout

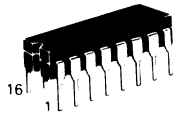


(top view)

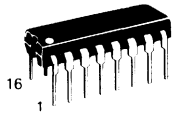
The TL594C is specified over the commercial operating range of 0°C to 70°C. The TL594I is specified over the industrial range of −25°C to 85°C. The TL594M is specified over the full military range of −55°C to 125°C.

PRECISION SWITCHMODE PULSE WIDTH MODULATION CONTROL CIRCUIT

SILICON MONOLITHIC INTEGRATED CIRCUITS



J SUFFIX
CERAMIC PACKAGE
CASE 620-10



N SUFFIX
PLASTIC PACKAGE
CASE 648-08

ORDERING INFORMATION

Device	Temperature Range	Package
TL594CN	0° to +70°C	Plastic DIP
TL594IN	−25° to +85°C	Plastic DIP
TL594MJ	−55° to +125°C	Ceramic DIP

This document contains information on a new product. Specifications and information herein are subject to change without notice.

FIGURE 1 — BLOCK DIAGRAM

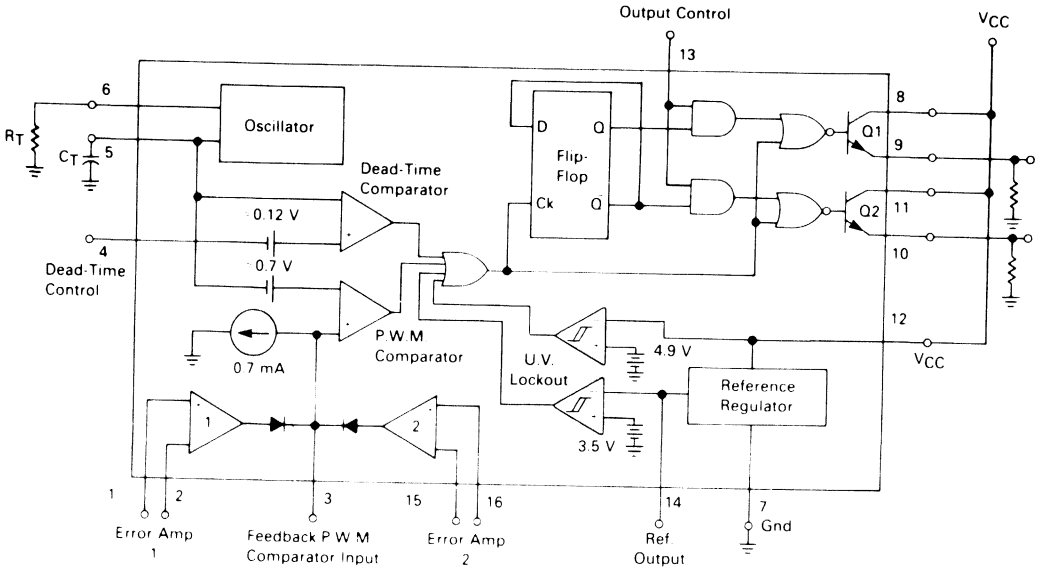
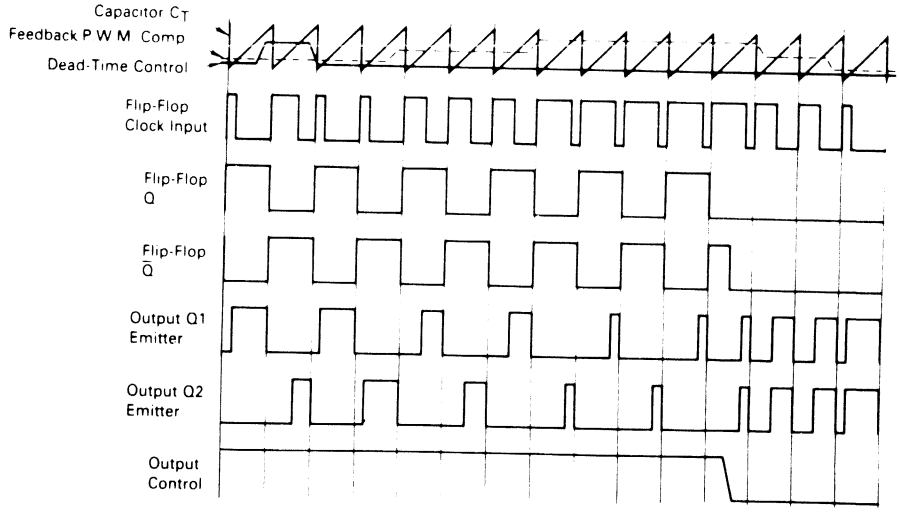


FIGURE 2 — TIMING DIAGRAM



Description

The TL594 is a fixed-frequency pulse width modulation control circuit, incorporating the primary building blocks required for the control of a switching power supply. (See Figure 1.) An internal-linear sawtooth oscillator is frequency-programmable by two external components, R_T and C_T. The approximate oscillator frequency is determined by:

$$f_{osc} \approx \frac{1.2}{R_T \bullet C_T}$$

For more information refer to Figure 4.

Output pulse width modulation is accomplished by comparison of the positive sawtooth waveform across capacitor C_T to either of two control signals. The NOR gates, which drive output transistors Q1 and Q2, are enabled only when the flip-flop clock-input line is in its low state. This happens only during that portion of time when the sawtooth voltage is greater than the control signals. Therefore, an increase in control-signal amplitude causes a corresponding linear decrease of output pulse width. (Refer to the timing diagram shown in Figure 2.)

The control signals are external inputs that can be fed into the dead-time control, the error amplifier inputs, or the feedback input. The dead-time control comparator has an effective 120 mV input offset which limits the minimum output dead time to approximately the first 4% of the sawtooth-cycle time. This would result in a maximum duty cycle on a given output of 96% with the output control grounded, and 48% with it connected to the reference line. Additional dead time may be imposed on the output by setting the dead time-control input to a fixed voltage, ranging between 0 to 3.3 V.

The pulse width modulator comparator provides a means for the error amplifiers to adjust the output pulse width from the maximum percent on-time, established by the dead time control input, down to zero, as the voltage at the feedback pin varies from 0.5 to 3.5 V. Both error amplifiers have a common-mode input range from −0.3 V to (V_{CC} − 2 V), and may be used to sense power-supply output voltage and current. The error-amplifier outputs are active high and are ORed together at the non-inverting input of the pulse-width modulator comparator. With this configuration, the amplifier that demands minimum output on time, dominates control of the loop.

When capacitor C_T is discharged, a positive pulse is generated on the output of the dead-time comparator, which clocks the pulse-steering flip-flop and inhibits the output transistors, Q1 and Q2. With the output-control connected to the reference line, the pulse-steering flip flop directs the modulated pulses to each of the two output transistors alternately for push-pull operation. The output frequency is equal to half that of the oscillator. Output drive can also be taken from Q1 or Q2, when single-ended operation with a maximum on-time of less than 50% is required. This is desirable when the output transformer has a ringback winding with a catch diode used for snubbing. When higher output-drive currents are required for single-ended operation, Q1 and Q2 may be connected in parallel, and the output-mode pin must be tied to ground to disable the flip-flop. The output frequency will now be equal to that of the oscillator.

The TL594 has an internal 5.0 V reference capable of sourcing up to 10 mA of load current for external bias circuits. The reference has an internal accuracy of ±1.5% with a typical thermal drift of less than 50 mV over an operating temperature range of 0 to 70°C.

FIGURE 3 — FUNCTIONAL TABLE

Input Output Control	Output Function	$\frac{f_{out}}{f_{osc}}$ =
Grounded	Single-ended P.W.M. at Q1 and Q2	1
At V_{ref}	Push-pull operation	0.5

MAXIMUM RATINGS (Full operating ambient temperature range applies unless otherwise noted)

Rating	Symbol	TL594C	TL594I	TL594M	Unit
Power Supply Voltage	V_{CC}	42	42	42	V
Collector Output Voltage	V_{C1}, V_{C2}	42	42	42	V
Collector Output Current (each transistor) (Note 1)	I_{C1}, I_{C2}	500	500	500	mA
Amplifier Input Voltage Range	V_{IR}	0.3 to 42	0.3 to 42	0.3 to 42	V
Power Dissipation @ T_A = 45 C	P_D	1000	1000	1000	mW
Operating Junction Temperature Plastic Package Ceramic Package	T_J	 125 —	 125 —	 — 150	C
Operating Ambient Temperature Range	T_A	0 to 70	25 to 85	55 to 125	C
Storage Temperature Range Plastic Package Ceramic Package	T_{stg}	 55 to 125 —	 55 to 125 —	 — 65 to 150	C

NOTE 1. Maximum thermal limits must be observed

THERMAL CHARACTERISTICS

Characteristics	Symbol	N Suffix Plastic Package	J Suffix Ceramic Package	Unit
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	80	100	C W
Derating Ambient Temperature	T_A	45	50	C

RECOMMENDED OPERATING CONDITIONS

Condition/Value	Symbol	TL594			Unit
		Min	Typ	Max	
Power Supply Voltage	V_{CC}	7.0	15	40	V
Collector Output Voltage	V_{C1}, V_{C2}	—	30	40	V
Collector Output Current (each transistor)	I_{C1}, I_{C2}	—	—	200	mA
Amplifier Input Voltage	V_{in}	0.3	—	V_{CC} 2.0	V
Current Into Feedback Terminal	I_{fb}	—	—	0.3	mA
Reference Output Current	I_{ref}	—	—	10	mA
Timing Resistor	R_T	1.8	30	500	kΩ
Timing Capacitor	C_T	0.0047	0.001	10	μF
Oscillator Frequency	f_{osc}	1.0	40	200	kHz
PWM Input Voltage (Pins 3, 4 & 13)	—	0.3	—	5.3	V

ELECTRICAL CHARACTERISTICS (V_{CC} 15 V, C_T 0.01 μF, R_T 12 kΩ unless otherwise noted.)
For typical values T_A 25 C, for min max values T_A is the operating ambient temperature range that applies unless otherwise noted.

Characteristic	Symbol	TL594C,I			TL594M			Unit
		Min	Typ	Max	Min	Typ	Max	
REFERENCE SECTION								
Reference Voltage (I_O 1.0 mA, T_A 25 C) (I_O 1.0 mA)	V_{ref}	 4.925 4.9	5.0 —	5.075 5.1	 4.925 4.9	5.0 —	5.075 5.1	V
Line Regulation (V_{CC} 7.0 V to 40 V)	Reg_{line}	—	2.0	25	—	2.0	25	mV
Load Regulation (I_O 1.0 mA to 10 mA)	Reg_{load}	—	2.0	15	—	2.0	15	mV
Short-Circuit Output Current (V_{ref} 0 V)	I_{SC}	15	40	75	15	40	75	mA

ELECTRICAL CHARACTERISTICS (V_{CC} = 15 V, C_T = 0.01 μF, R_T = 12 kΩ unless otherwise noted.)
For typical values T_A = 25 C, for min max values T_A is the operating ambient temperature range that applies unless otherwise noted.

Characteristic	Symbol	TL594C,I			TL594M			Unit
		Min	Typ	Max	Min	Typ	Max	
OUTPUT SECTION								
Collector Off-State Current (V_{CC} = 40 V, V_{CE} = 40 V)	$I_{C(off)}$	—	2.0	100	—	2.0	100	μA
Emitter Off-State Current (V_{CC} = 40 V, V_C = 40 V, V_E = 0 V)	$I_{E(off)}$	—	—	100	—	—	100	μA
Collector-Emitter Saturation Voltage (Note 2) Common-Emitter (V_E = 0 V, I_C = 200 mA) Emitter-Follower (V_C = 15 V, I_E = −200 mA)	$V_{SAT(C)}$	—	1.1	1.3	—	1.1	1.5	V
	$V_{SAT(E)}$	—	1.5	2.5	—	1.5	2.5	V
Output Control Pin Current Low State (V_{OC} = 0.4 V)	I_{OCL}	—	0.1	—	—	0.1	—	μA
High State (V_{OC} = V_{ref})	I_{OCH}	—	2.0	20	—	2.0	20	μA
Output Voltage Rise Time Common-Emitter (See Figure 13)	t_r	—	100	200	—	100	200	ns
Emitter-Follower (See Figure 14)		—	100	200	—	100	200	ns
Output Voltage Fall Time Common-Emitter (See Figure 13)	t_f	—	40	100	—	40	100	ns
Emitter-Follower (See Figure 14)		—	40	100	—	40	100	ns

Characteristic	Symbol	TL594			Unit
		Min	Typ	Max	
ERROR AMPLIFIER SECTIONS					
Input Offset Voltage (V_O (Pin 3) = 2.5 V)	V_{IO}	—	2.0	10	mV
Input Offset Current (V_O (Pin 3) = 2.5 V)	I_{IO}	—	5.0	250	nA
Input Bias Current (V_O (Pin 3) = 2.5 V)	I_{IB}	—	−0.1	−1.0	μA
Input Common-Mode Voltage Range (V_{CC} = 40 V, T_A = 25 C)	V_{ICR}	0 to V_{CC} − 2.0	—	—	V
Inverting Input Voltage Range	$V_{IR(INV)}$	−0.3 to V_{CC} − 2.0	—	—	V
Open-Loop Voltage Gain (ΔV_O = 3.0 V, V_O = 0.5 to 3.5 V, R_L = 2.0 kΩ)	A_{VOL}	70	95	—	dB
Unity-Gain Crossover Frequency (V_O = 0.5 to 3.5 V, R_L = 2.0 kΩ)	f_C	—	700	—	kHz
Phase Margin at Unity-Gain (V_O = 0.5 to 3.5 V, R_L = 2.0 kΩ)	ϕ_m	—	65	—	deg.
Common-Mode Rejection Ratio (V_{CC} = 40 V)	CMRR	65	90	—	dB
Power Supply Rejection Ratio (ΔV_{CC} = 33 V, V_O = 2.5 V, R_L = 2.0 kΩ)	PSRR	—	100	—	dB
Output Sink Current (V_O (Pin 3) = 0.7 V)	I_O^-	0.3	0.7	—	mA
Output Source Current (V_O (Pin 3) = 3.5 V)	I_O^+	−2.0	−4.0	—	mA

NOTE 2: Low duty cycle pulse techniques are used during test to maintain junction temperature as close to ambient temperature as possible.

ELECTRICAL CHARACTERISTICS (V_{CC} = 15 V, C_T = 0.01 μF, R_T = 12 kΩ unless otherwise noted.)
For typical values T_A = 25°C, for min max values T_A is the operating ambient temperature range that applies unless otherwise noted.

Characteristic	Symbol	TL594 Min	TL594 Typ	TL594 Max	Unit
PWM COMPARATOR SECTION (Test Circuit Figure 12)					
Input Threshold Voltage (Zero Duty Cycle)	V_{TH}	—	3.6	4.5	V
Input Sink Current ($V_{Pin\ 3}$ = 0.7 V)	I_I	0.3	0.7	—	mA
DEAD-TIME CONTROL SECTION (Test Circuit Figure 12)					
Input Bias Current (Pin 4) ($V_{Pin\ 4}$ = 0 to 5.25 V)	I_{IB} (DT)	—	2.0	10	μA
Maximum Duty Cycle, Each Output, Push-Pull Mode ($V_{Pin\ 4}$ = 0 V, C_T = 0.01 μF, R_T = 12 kΩ)	DC_{max}	45	48	50	%
($V_{Pin\ 4}$ = 0 V, C_T = 0.001 μF, R_T = 30 kΩ)		—	45	—	
Input Threshold Voltage (Pin 4) (Zero Duty Cycle)	V_{TH}	—	2.8	3.3	V
(Maximum Duty Cycle)		0	—	—	
OSCILLATOR SECTION					
Frequency (C_T = 0.001 μF, R_T = 30 kΩ)	f_{osc}	—	40	—	kHz
(C_T = 0.01 μF, R_T = 12 kΩ, T_A = 25°C)		9.2	10	10.8	
(C_T = 0.01 μF, R_T = 12 kΩ, T_A = T_{low} to T_{high})		9.0	—	12	
Standard Deviation of Frequency* (C_T = 0.001 μF, R_T = 30 kΩ)	σf_{osc}	—	1.5	—	%
Frequency Change with Voltage (V_{CC} = 7.0 V to 40 V, T_A = 25°C)	Δf_{osc} (ΔV)	—	0.2	1.0	%
Frequency Change with Temperature (ΔT_A = T_{low} to T_{high}, C_T = 0.01 μF, R_T = 12 kΩ)	Δf_{osc} (ΔT)	—	4.0	—	%
UNDERVOLTAGE LOCKOUT SECTION					
Turn-On Threshold (V_{CC} Increasing, I_{ref} = 1.0 mA) T_A = 25°C	V_{th}	4.0	5.2	6.0	V
T_A = T_{low} to T_{high}		3.5	—	6.5	
Hysteresis TL594C,I	V_H	100	150	300	mV
TL594M		50	150	300	
TOTAL DEVICE					
Standby Supply Current (Pin 6 at V_{ref}, All Other Inputs and Outputs Open) (V_{CC} = 15 V)	I_{CC}	—	8.0	15	mA
(V_{CC} = 40 V)		—	8.5	18	
Average Supply Current ($V_{Pin\ 4}$ = 2.0 V, C_T = 0.01 μF, R_T = 12 kΩ, V_{CC} = 15 V, See Figure 12)	—	—	11	—	mA

*Standard deviation is a measure of the statistical distribution about the mean as derived from the formula, $\sigma = \sqrt{\frac{\sum_{n=1}^{N} (X_n - \bar{X})^2}{N-1}}$

FIGURE 4 — OSCILLATOR FREQUENCY versus TIMING RESISTANCE

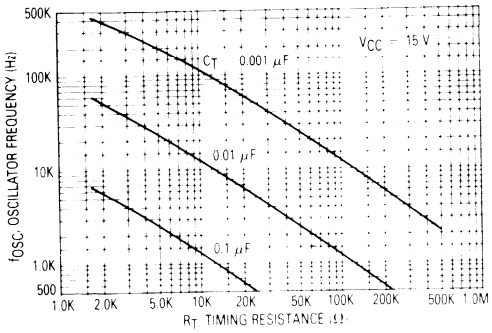


FIGURE 5 — OPEN-LOOP VOLTAGE GAIN AND PHASE versus FREQUENCY

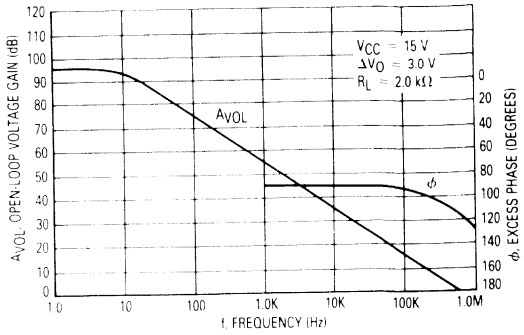


FIGURE 6 — PERCENT DEAD-TIME versus OSCILLATOR FREQUENCY

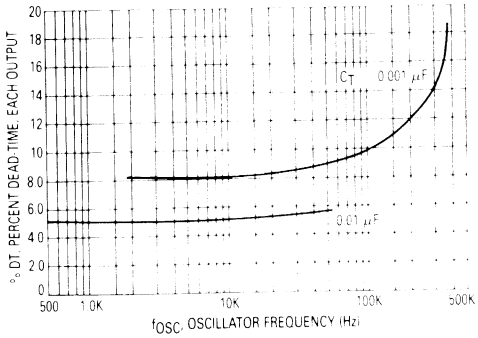


FIGURE 7 — PERCENT DUTY CYCLE versus DEAD-TIME CONTROL VOLTAGE

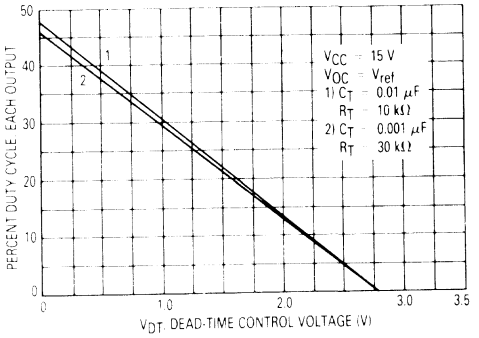


FIGURE 8 — EMITTER FOLLOWER CONFIGURATION OUTPUT SATURATION VOLTAGE versus EMITTER CURRENT

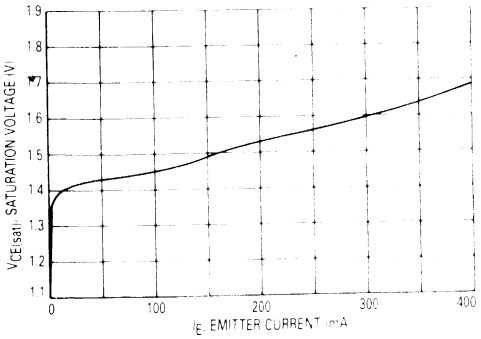


FIGURE 9 — COMMON EMITTER CONFIGURATION OUTPUT SATURATION VOLTAGE versus COLLECTOR CURRENT

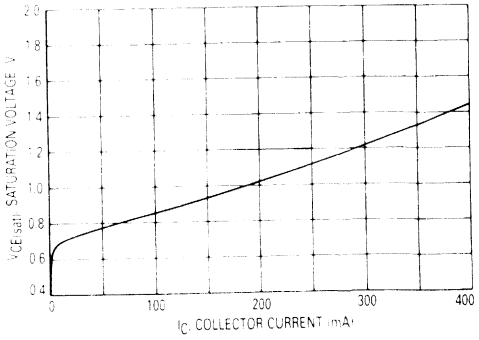


FIGURE 10 — STANDBY SUPPLY CURRENT versus SUPPLY VOLTAGE

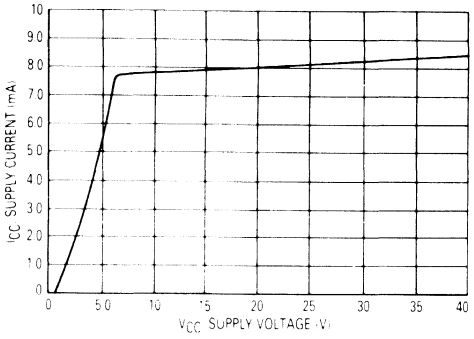


FIGURE 11 — UNDERVOLTAGE LOCKOUT THRESHOLDS versus REFERENCE LOAD CURRENT

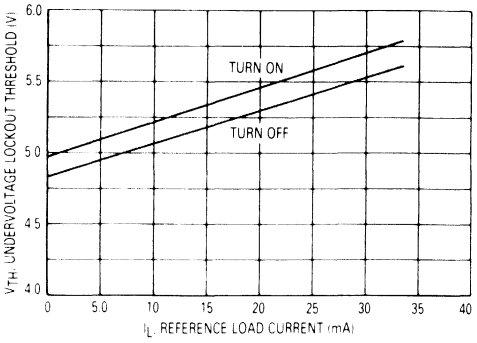


FIGURE 12 — ERROR AMPLIFIER CHARACTERISTICS

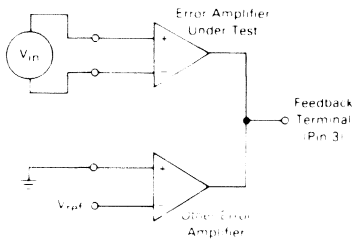


FIGURE 13 — DEAD-TIME AND FEEDBACK CONTROL TEST CIRCUIT

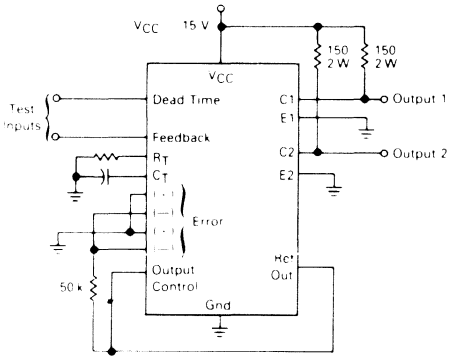


FIGURE 14 — COMMON-EMITTER CONFIGURATION TEST CIRCUIT AND WAVEFORM

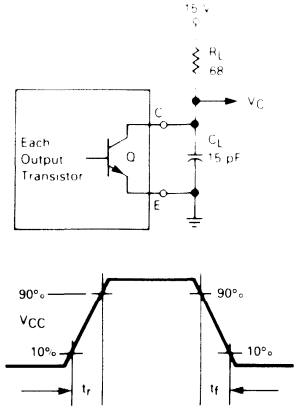


FIGURE 15 — EMITTER-FOLLOWER CONFIGURATION TEST CIRCUIT AND WAVEFORM

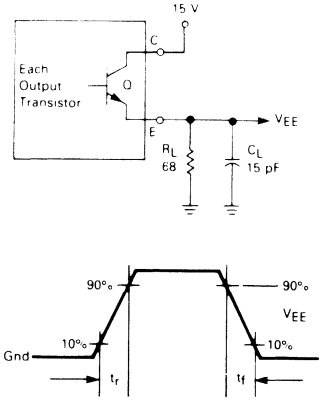


FIGURE 16 — ERROR-AMPLIFIER SENSING TECHNIQUES

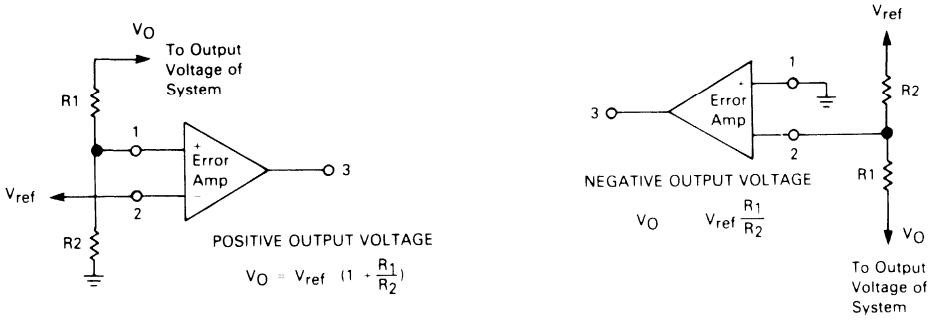


FIGURE 17 — DEAD-TIME CONTROL CIRCUIT

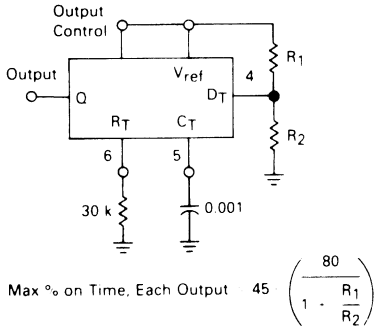


FIGURE 18 — SOFT-START CIRCUIT

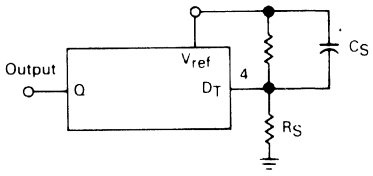


FIGURE 19 — OUTPUT CONNECTIONS FOR SINGLE-ENDED AND PUSH-PULL CONFIGURATIONS

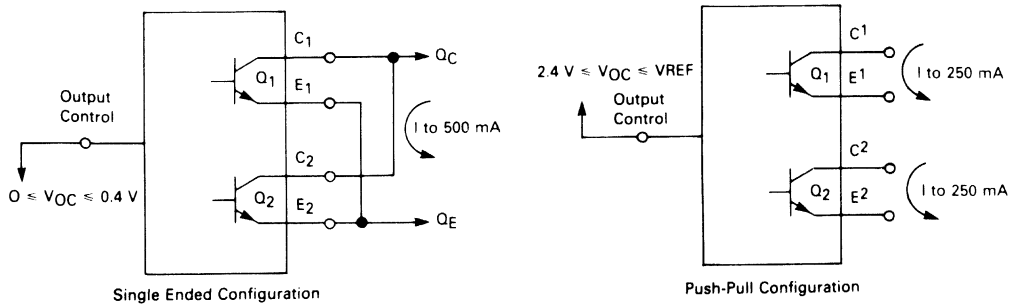


FIGURE 20 — SLAVING TWO OR MORE CONTROL CIRCUITS

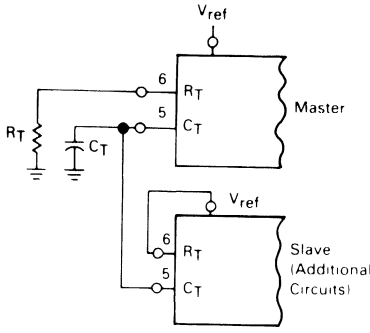


FIGURE 21 — OPERATION WITH V_{IN} > 40 V USING EXTERNAL ZENER

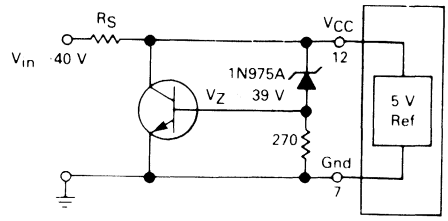
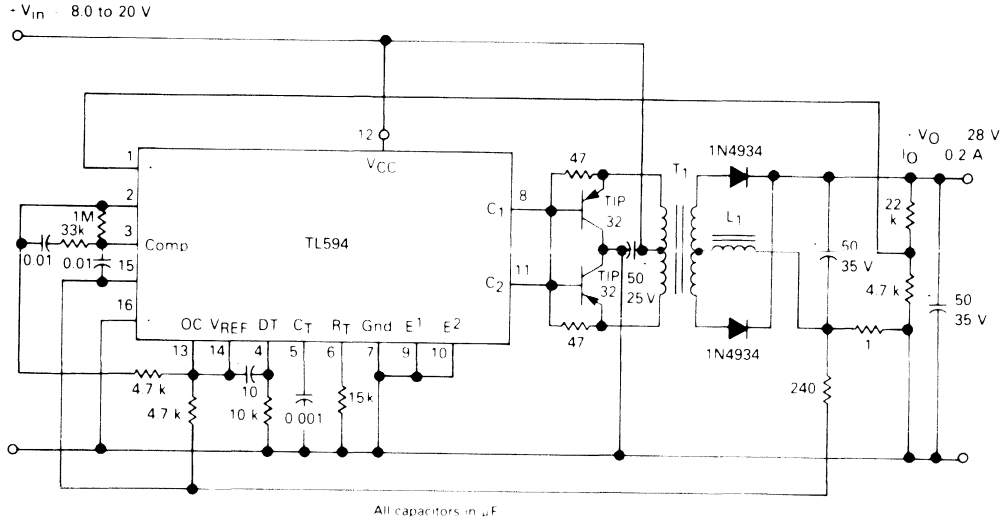


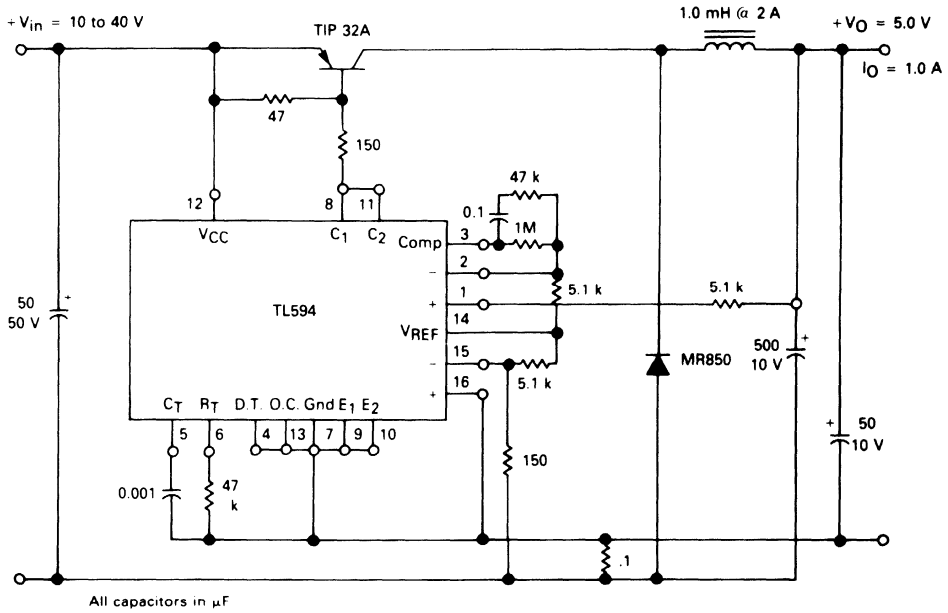
FIGURE 22 — PULSE-WIDTH MODULATED PUSH-PULL CONVERTER



L1 — 3.5 mH @ 0.3 A
T1 — Primary: 20T C.T. #28 AWG
Secondary: 120T C.T. #36 AWG
Core: Ferroxcube 1408P-L00-3C8

TEST	CONDITIONS	RESULTS
Line Regulation	V_{in} = 10 V to 40 V	14 mV 0.28%
Load Regulation	V_{in} = 28 V, I_O = 1 mA to 1 A	3.0 mV 0.06%
Output Ripple	V_{in} = 28 V, I_O = 1.0 A	65 mV P-P P.A.R.D.
Short Circuit Current	V_{in} = 28 V, R_L = 0.1 Ω	1.6 amps
Efficiency	V_{in} = 28 V, I_O = 1 A	71%

FIGURE 23 — PULSE-WIDTH MODULATED STEP-DOWN CONVERTER



TEST	CONDITIONS	RESULTS
Line Regulation	V_{in} = 8.0 to 40 V	3.0 mV 0.01%
Load Regulation	V_{in} = 12.6 V, I_O = 0.2 to 200 mA	5.0 mV 0.02%
Output Ripple	V_{in} = 12.6 V, I_O = 200 mA	40 mV p-P P.A.R.D.
Short Circuit Current	V_{in} = 12.6 V, R_L = 0.1 Ω	250 mA
Efficiency	V_{in} = 12.6 V, I_O = 200 mA	72%

MOTOROLA

TL780 Series

THREE-TERMINAL POSITIVE VOLTAGE REGULATORS

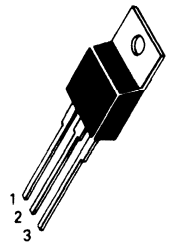
This family of precision fixed voltage regulators are monolithic integrated circuits capable of driving loads in excess of 1.5 amperes. Innovative design concepts, coupled with advanced thermal layout techniques has resulted in improved accuracy and excellent load, line and thermal regulation characteristics. Internal current limiting, thermal shutdown and safe-area compensation are employed, making these devices extremely rugged and virtually immune to overload.

- ±1% Output Voltage Tolerance @ 25°C
- ±2% Output Voltage Tolerance Over Full Operating Temperature Range
- Internal Short-Circuit Current Limiting
- Internal Thermal Overload Protection
- Output Transistor Safe-Area Compensation
- No External Components Required
- Pinout Compatible with MC7800 Series

THREE-TERMINAL POSITIVE FIXED VOLTAGE REGULATORS

SILICON MONOLITHIC INTEGRATED CIRCUITS

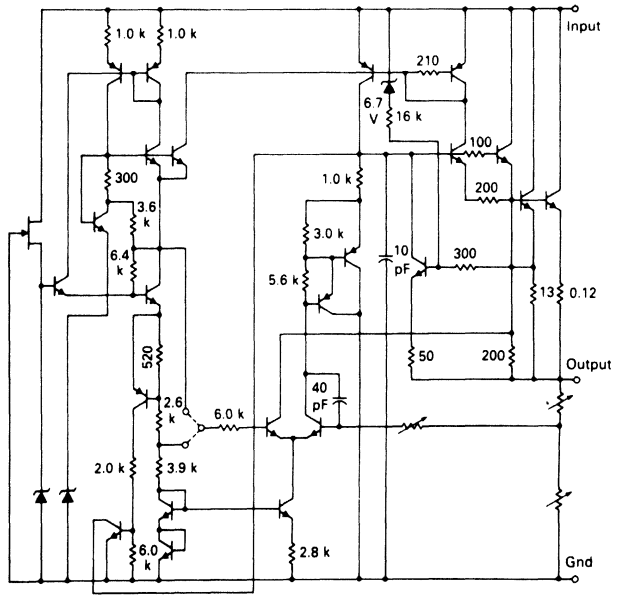
KC SUFFIX
PLASTIC PACKAGE
CASE 221A-04



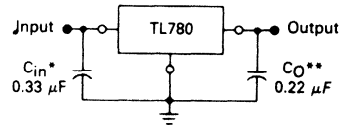
Pin 1. Input
2. Ground
3. Output

(Heatsink surface connected to Pin 2.)

EQUIVALENT SCHEMATIC DIAGRAM



STANDARD APPLICATION



A common ground is required between the input and the output voltages. The input voltage must remain typically 2.0 V above the output voltage even during the low point on the input ripple voltage.

XX = these two digits of the type number indicate voltage.

* = C_{in} is required if regulator is located an appreciable distance from power supply filter.

** = C_O is not needed for stability; however, it does improve transient response.

ORDERING INFORMATION

Nominal Output Voltage	Device
5.0 V	TL780-05CKC
12 V	TL780-12CKC
15 V	TL780-15CKC

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Input Voltage	V_{in}	35	Vdc
Power Dissipation and Thermal Characteristics			
T_A = +25°C	P_D	2.0	Watts
Derate above T_A = +25°C	1 θ_{JA}	16	mW/°C
Thermal Resistance, Junction to Air	θ_{JA}	62.5	°C/W
T_C = +25°C	P_D	15	Watts
Derate above T_C = +75°C (See Figure 1)	1 θ_{JC}	200	mW/°C
Thermal Resistance, Junction to Case	θ_{JC}	5.0	°C/W
Operating Junction Temperature Range	T_J	0 to +150	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C

TL780-05C

ELECTRICAL CHARACTERISTICS (V_{in} = 10 V, I_O = 500 mA, 0°C ≤ T_J ≤ +125°C unless otherwise noted [Note 1])

Characteristic	Symbol	TL780-05C Min	TL780-05C Typ	TL780-05C Max	Unit
Output Voltage	V_O				V
5.0 mA ≤ I_O ≤ 1.0 A, P ≤ 15 W					
7.0 V ≤ V_{in} ≤ 20 V					
T_J = +25°C		4.95	5.0	5.05	
0°C ≤ T_J ≤ +125°C		4.90	—	5.10	
Line Regulation (T_J = +25°C)	Reg_{line}				mV
7.0 V ≤ V_{in} ≤ 25 V		—	0.5	5.0	
8.0 V ≤ V_{in} ≤ 12 V		—	0.5	5.0	
Load Regulation (T_J = +25°C)	Reg_{load}				mV
5.0 mA ≤ I_O ≤ 1.5 A		—	4.0	25	
250 mA ≤ I_O ≤ 750 mA		—	1.5	15	
Ripple Rejection	RR	70	80	—	dB
8.0 V ≤ V_{in} ≤ 18 V, f = 120 Hz					
Output Resistance (f = 1.0 kHz)	r_O	—	0.0035	—	Ω
Average Temperature Coefficient of Output Voltage	TCV_O	—	0.06	—	mV/°C
I_O = 5.0 mA					
Output Noise Voltage (T_J = +25°C)	V_n	—	75	—	μV
10 Hz ≤ f ≤ 100 kHz					
Dropout Voltage (T_J = +25°C)	V_{in}-V_O	—	2.0	—	V
I_O = 1.0 A					
Bias Current (T_J = +25°C)	I_B	—	3.5	8.0	mA
Bias Current Change	ΔI_B				mA
7.0 V ≤ V_{in} ≤ 25 V, I_O = 500 mA		—	0.7	1.3	
5.0 mA ≤ I_O ≤ 1.0 A, V_{in} = 10 V		—	0.03	0.5	
Short-Circuit Output Current (T_J = +25°C)	I_{sc}	—	200	—	mA
V_{in} = 35 V					
Peak Output Current (T_J = +25°C)	I_P	—	2.2	—	A

Note 1: Line and load regulation are specified at constant junction temperature. Changes in V_O due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

TL780-12C

ELECTRICAL CHARACTERISTICS (V_{in} = 19 V, I_O = 500 mA, 0°C ≤ T_J ≤ +125°C unless otherwise noted [Note 1])

Characteristic	Symbol	TL780-12C Min	TL780-12C Typ	TL780-12C Max	Unit
Output Voltage	V_O				V
5.0 mA ≤ I_O ≤ 1.0 A, P ≤ 15 W					
14.5 V ≤ V_{in} ≤ 27 V					
T_J = +25°C		11.88	12	12.12	
0°C ≤ T_J ≤ +125°C		11.76	—	12.24	
Line Regulation (T_J = +25°C)	Reg_{line}				mV
14.5 V ≤ V_{in} ≤ 30		—	1.2	12	
16 V ≤ V_{in} ≤ 22		—	1.2	12	

TL780-12C (continued)

ELECTRICAL CHARACTERISTICS (V_{in} = 19 V, I_O = 500 mA, 0°C ≤ T_J ≤ +125°C unless otherwise noted [Note 1])

Characteristic	Symbol	TL780-12C Min	TL780-12C Typ	TL780-12C Max	Unit
Load Regulation (T_J = +25°C) 5.0 mA ≤ I_O ≤ 1.5 A 250 mA ≤ I_O ≤ 750 mA	Reg_{load}	 — —	 6.5 2.5	 60 36	mV
Ripple Rejection 15 V ≤ V_{in} ≤ 25 V, f = 120 Hz	RR	65	77	—	dB
Output Resistance (f = 1.0 kHz)	r_O	—	0.0035	—	Ω
Average Temperature Coefficient of Output Voltage I_O = 5.0 mA	TCV_O	—	0.15	—	mV/°C
Output Noise Voltage (T_J = +25°C) 10 Hz ≤ f ≤ 100 kHz	V_n	—	180	—	μV
Dropout Voltage (T_J = +25°C) I_O = 1.0 A	V_{in}-V_O	—	2.0	—	V
Bias Current (T_J = +25°C)	I_B	—	3.5	8.0	mA
Bias Current Change 14.5 V ≤ V_{in} ≤ 30 V, I_O = 500 mA 5.0 mA ≤ I_O ≤ 1.0 A, V_{in} = 19 V	ΔI_B	 — —	 0.4 0.03	 1.3 0.5	mA
Short-Circuit Output Current (T_J = +25°C) V_{in} = 35 V	I_{sc}	—	200	—	mA
Peak Output Current (T_J = +25°C)	I_P	—	2.2	—	A

Note 1: Line and load regulation are specified at constant junction temperature. Changes in V_O due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

TL780-15C

ELECTRICAL CHARACTERISTICS (V_{in} = 23 V, I_O = 500 mA, 0°C ≤ T_J ≤ +125°C unless otherwise noted [Note 1])

Characteristic	Symbol	TL780-15C Min	TL780-15C Typ	TL780-15C Max	Unit
Output Voltage 5.0 mA ≤ I_O ≤ 1.0 A, P ≤ 15 W 17.5 V ≤ V_{in} ≤ 30 V T_J = +25°C 0°C ≤ T_J ≤ +125°C	V_O	 14.85 14.70	 15 —	 15.15 15.30	V
Line Regulation (T_J = +25°C) 17.5 V ≤ V_{in} ≤ 30 V 20 V ≤ V_{in} ≤ 26 V	Reg_{line}	 — —	 1.5 1.5	 15 15	mV
Load Regulation (T_J = +25°C) 5.0 mA ≤ I_O ≤ 1.5 A 250 mA ≤ I_O ≤ 750 mA	Reg_{load}	 — —	 7.0 2.5	 75 45	mV
Ripple Rejection 18.5 V ≤ V_{in} ≤ 28.5 V, f = 120 Hz	RR	60	75	—	dB
Output Resistance (f = 1.0 kHz)	r_O	—	0.0035	—	Ω
Average Temperature Coefficient of Output Voltage I_O = 5.0 mA	TCV_O	—	0.18	—	mV/°C
Output Noise Voltage (T_J = +25°C) 10 Hz ≤ f ≤ 100 kHz	V_n	—	225	—	μV
Dropout Voltage (T_J = +25°C) I_O = 1.0 A	V_{in}-V_O	—	2.0	—	V
Bias Current (T_J = +25°C)	I_B	—	3.6	8.0	mA
Bias Current Change 17.5 V ≤ V_{in} ≤ 30 V, I_O = 500 mA 5.0 mA ≤ I_O ≤ 1.0 A, V_{in} = 23 V	ΔI_B	 — —	 0.4 0.02	 1.3 0.5	mA
Short-Circuit Output Current (T_J = +25°C) V_{in} = 35 V	I_{sc}	—	200	—	mA
Peak Output Current (T_J = +25°C)	I_P	—	2.2	—	A

Note 1: Line and load regulation are specified at constant junction temperature. Changes in V_O due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

TYPICAL PERFORMANCE CHARACTERISTICS

VOLTAGE REGULATOR PERFORMANCE

The performance of a voltage regulator is specified by its immunity to changes in load, input voltage, power dissipation, and temperature. Line and load regulation are tested with a pulse of short duration (< 100 μs) and are strictly a function of electrical gain. However, pulse widths of longer duration (> 1.0 ms) are sufficient to affect temperature gradients across the die. These temperature gradients can cause a change in the output voltage, in addition to changes caused by line and load regulation. Longer pulse widths and thermal gradients make it desirable to specify thermal regulation.

Thermal regulation is defined as the change in output voltage caused by a change in dissipated power for a specified time, and is expressed as a percentage output voltage change per watt. The change in dissipated power can be caused by a change in either the input voltage or the load current. Thermal regulation is a function of I.C. layout and die attach techniques, and usually occurs within 10 ms of a change in power dissipation. After 10 ms, additional changes in the output voltage are due to the temperature coefficient of the device.

Figure 1 shows the line and thermal regulation response of a typical TL780-05C to a 10 watt input pulse. The variation of the output voltage due to line regulation is labeled ① and the thermal regulation component is labeled ②. Figure 2 shows the load and thermal regulation response of a typical TL780-05C to a 15 watt load pulse. The output voltage variation due to load regulation is labeled ① and the thermal regulation component is labeled ②.

FIGURE 1 — LINE AND THERMAL REGULATION

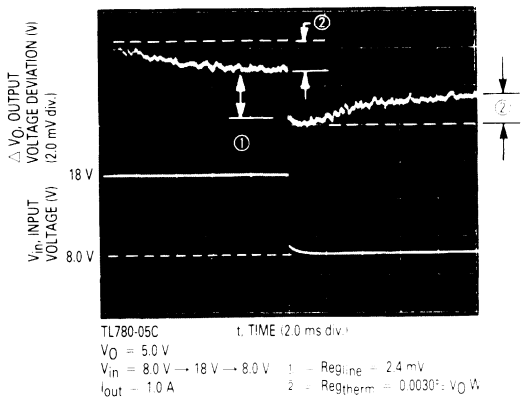


FIGURE 2 — LOAD AND THERMAL REGULATION

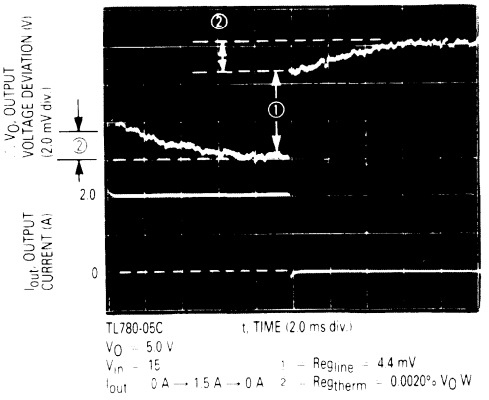


FIGURE 3 — TEMPERATURE STABILITY

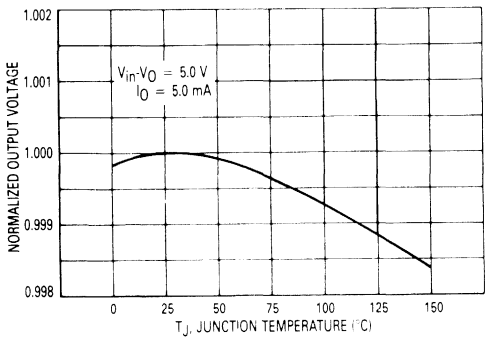


FIGURE 4 — OUTPUT IMPEDANCE

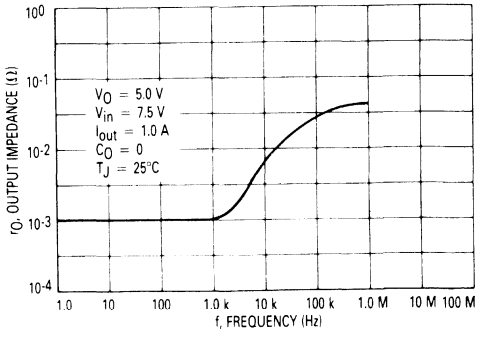


FIGURE 5 — RIPPLE REJECTION versus FREQUENCY

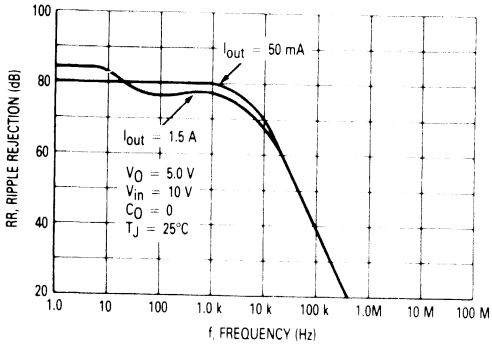


FIGURE 6 — RIPPLE REJECTION versus OUTPUT CURRENT

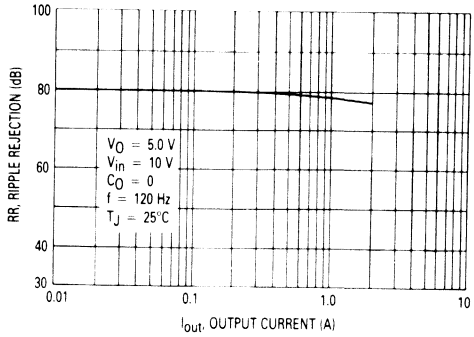


FIGURE 7 — BIAS CURRENT versus INPUT VOLTAGE

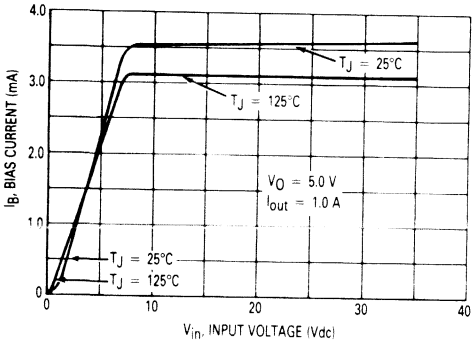


FIGURE 8 — BIAS CURRENT versus OUTPUT CURRENT

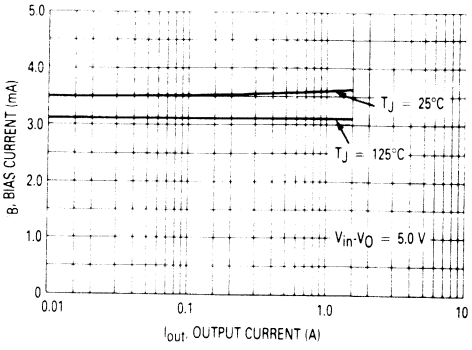


FIGURE 9 — DROPOUT VOLTAGE

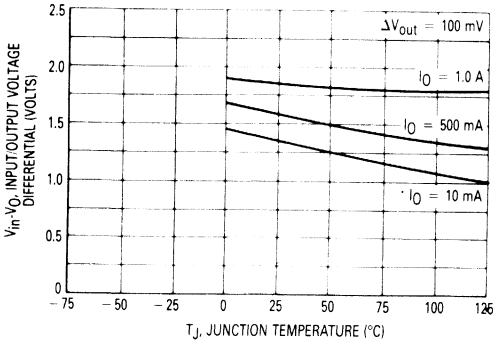


FIGURE 10 — PEAK OUTPUT CURRENT

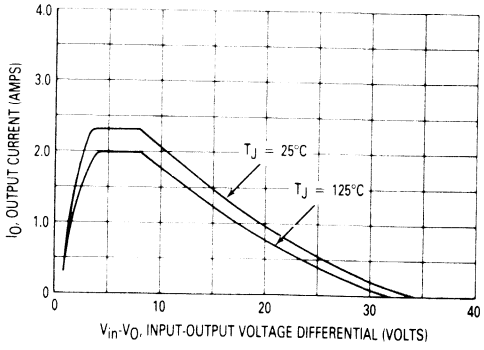


FIGURE 11 — LINE TRANSIENT RESPONSE

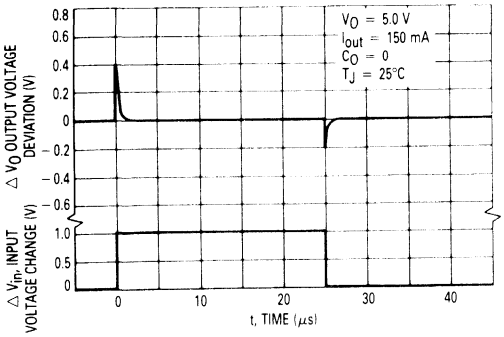


FIGURE 12 — LOAD TRANSIENT RESPONSE

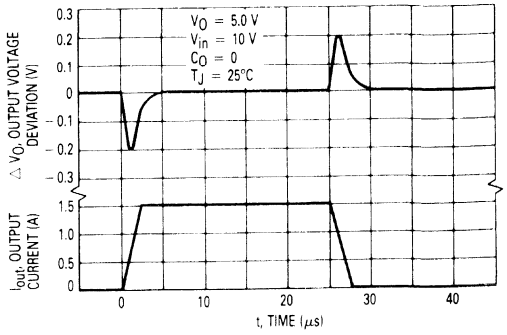
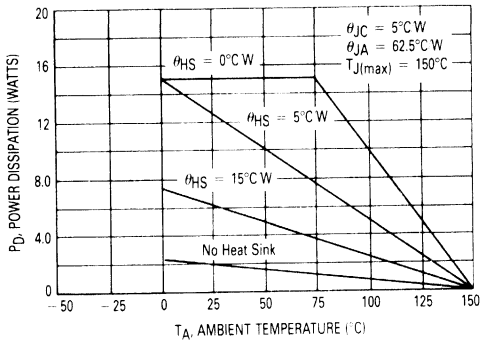


FIGURE 13 — WORST CASE POWER DISSIPATION versus AMBIENT TEMPERATURE



MOTOROLA

UC3842A, 43A
UC2842A, 43A

Advance Information

HIGH PERFORMANCE CURRENT MODE CONTROLLER

The UC3842A, UC3843A series are high performance fixed frequency current mode controllers. They are specifically designed for Off-Line and DC-to-DC converter applications offering the designer a cost effective solution with minimal external components. These integrated circuits feature a trimmed oscillator for precise duty cycle control, a temperature compensated reference, high gain error amplifier, current sensing comparator, and a high current totem pole output ideally suited for driving a power MOSFET.

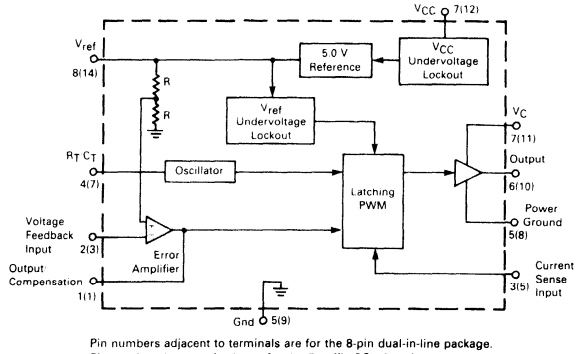
Also included are protective features consisting of input and reference undervoltage lockouts each with hysteresis, cycle-by-cycle current limiting, programmable output deadtime, and a latch for single pulse metering.

These devices are available in 8-pin dual-in-line ceramic and plastic packages as well as the 14-pin plastic surface mount (SO-14). The SO-14 package has separate power and ground pins for the totem pole output stage.

The UCX842A has UVLO thresholds of 16 V (on) and 10 V (off), ideally suited for off-line converters. The UCX843A is tailored for lower voltage applications having UVLO thresholds of 8.5 V (on) and 7.6 V (off).

- Trimmed Oscillator Discharge Current for Precise Duty Cycle Control
- Current Mode Operation to 500 kHz
- Automatic Feed Forward Compensation
- Latching PWM for Cycle-By-Cycle Current Limiting
- Internally Trimmed Reference with Undervoltage Lockout
- High Current Totem Pole Output
- Undervoltage Lockout with Hysteresis
- Low Start-Up and Operating Current
- Direct Interface with Motorola SENSEFET Products

SIMPLIFIED BLOCK DIAGRAM



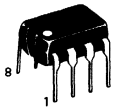
Pin numbers adjacent to terminals are for the 8-pin dual-in-line package.
Pin numbers in parenthesis are for the D suffix SO-14 package.

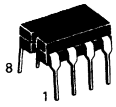
This document contains information on a new product. Specifications and information herein are subject to change without notice.

HIGH PERFORMANCE CURRENT MODE CONTROLLER

SILICON MONOLITHIC INTEGRATED CIRCUIT

N SUFFIX
PLASTIC PACKAGE
CASE 626-05

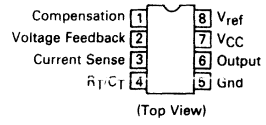




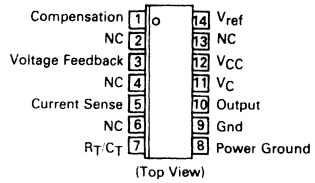
J SUFFIX
CERAMIC PACKAGE
CASE 693-02

D SUFFIX
PLASTIC PACKAGE
CASE 751A-02
SO-14

PIN CONNECTIONS



(Top View)



(Top View)

ORDERING INFORMATION

Device	Temperature Range	Package
UC3842AD	0 to +70°C	SO-14 Plastic DIP
UC3843AD		SO-14 Plastic DIP
UC3842AN		Plastic DIP
UC3843AN		Plastic DIP
UC2842AD	−25 to +85°C	SO-14 Plastic DIP
UC2843AD		SO-14 Plastic DIP
UC2842AJ		Ceramic DIP
UC2843AJ		Ceramic DIP
UC2842AN		Plastic DIP
UC2843AN		Plastic DIP

MAXIMUM RATING

Rating	Symbol	Value	Unit
Total Power Supply and Zener Current	$(I_{CC}+I_Z)$	30	mA
Output Current, Source or Sink (Note 1)	I_O	1.0	A
Output Energy (Capacitive Load per Cycle)	W	5.0	μJ
Current Sense and Voltage Feedback Inputs	V_{in}	−0.3 to +5.5	V
Error Amp Output Sink Current	I_O	10	mA
Power Dissipation and Thermal Characteristics D Suffix, Plastic Package Maximum Power Dissipation @ T_A = 25°C Thermal Resistance Junction to Air N Suffix, Plastic Package and J Suffix, Ceramic Package Maximum Power Dissipation @ T_A = 25°C Thermal Resistance Junction to Air	 P_D $R_{\theta JA}$ P_D $R_{\theta JA}$	 862 145 1.25 100	 mW °C/W W °C/W
Operating Junction Temperature	T_J	+150	°C
Operating Ambient Temperature UC3842A, UC3843A UC2842A, UC2843A	T_A	 0 to +70 −25 to +85	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = 15 V [Note 2], R_T = 10 k, C_T = 3.3 nF, T_A = T_{low} to T_{high} [Note 3] unless otherwise noted)

Characteristic	Symbol	UC284XA			UC384XA			Unit
		Min	Typ	Max	Min	Typ	Max	
REFERENCE SECTION								
Reference Output Voltage (I_O = 1.0 mA, T_J = 25°C)	V_{ref}	4.95	5.0	5.05	4.9	5.0	5.1	V
Line Regulation (V_{CC} = 12 V to 25 V)	Reg_{line}	—	2.0	20	—	2.0	20	mV
Load Regulation (I_O = 1.0 mA to 20 mA)	Reg_{load}	—	3.0	25	—	3.0	25	mV
Temperature Stability	T_S	—	0.2	—	—	0.2	—	mV/°C
Total Output Variation over Line, Load, and Temperature	V_{ref}	4.9	—	5.1	4.82	—	5.18	V
Output Noise Voltage (f = 10 Hz to 10 kHz, T_J = 25°C)	V_n	—	50	—	—	50	—	μV
Long Term Stability (T_A = 125°C for 1000 Hours)	S	—	5.0	—	—	5.0	—	mV
Output Short Circuit Current	I_{SC}	−30	−85	−180	−30	−85	−180	mA
OSCILLATOR SECTION								
Frequency T_J = 25°C T_A = T_{low} to T_{high}	f_{OSC}	 47 46	 52 —	 57 60	 47 46	 52 —	 57 60	kHz
Frequency Change with Voltage (V_{CC} = 12 V to 25 V)	$\Delta f_{OSC}/\Delta V$	—	0.2	1.0	—	0.2	1.0	%
Frequency Change with Temperature T_A = T_{low} to T_{high}	$\Delta f_{OSC}/\Delta T$	—	5.0	—	—	5.0	—	%
Oscillator Voltage Swing (Peak-to-Peak)	V_{OSC}	—	1.6	—	—	1.6	—	V
Discharge Current (V_{OSC} = 2.0 V) T_J = 25°C T_A = T_{low} to T_{high}	I_{dischg}	 7.5 7.2	 8.4 —	 9.3 9.5	 7.5 7.2	 8.4 —	 9.3 9.5	mA

Notes: 1. Maximum Package power dissipation limits must be observed.
2. Adjust V_{CC} above the Start-Up threshold before setting to 15 V.
3. Low duty cycle pulse techniques are used during test to maintain junction temperature as close to ambient as possible.
T_{low} = 0°C for UC3842A, UC3843A; = −25°C for UC2842A, UC2843A
T_{high} = +70°C for UC3842A, UC3843A; = +85°C for UC2842A, UC2843A
4. This parameter is measured at the latch trip point with V_{FB} = 0 V.
5. Comparator gain is defined as: $A_V = \frac{\Delta V \text{ Output Compensation}}{\Delta V \text{ Current Sense Input}}$

ELECTRICAL CHARACTERISTICS (V_{CC} = 15 V [Note 2], R_T = 10 k, C_T = 3.3 nF, T_A = T_{low} to T_{high} [Note 3] unless otherwise noted)

Characteristic	Symbol	UC284XA Min	UC284XA Typ	UC284XA Max	UC384XA Min	UC384XA Typ	UC384XA Max	Unit
ERROR AMPLIFIER SECTION								
Voltage Feedback Input (V_O = 2.5 V)	V_{FB}	2.45	2.5	2.55	2.42	2.5	2.58	V
Input Bias Current (V_{FB} = 5.0 V)	I_{IB}	—	−0.1	−1.0	—	−0.1	−2.0	μA
Open-Loop Voltage Gain (V_O = 2.0 V to 4.0 V)	A_{VOL}	65	90	—	65	90	—	dB
Unity Gain Bandwidth (T_J = 25°C)	BW	0.7	1.0	—	0.7	1.0	—	MHz
Power Supply Rejection Ratio (V_{CC} = 12 V to 25 V)	PSRR	60	70	—	60	70	—	dB
Output Current								mA
Sink (V_O = 1.1 V, V_{FB} = 2.7 V)	I_{Sink}	2.0	12	—	2.0	12	—	
Source (V_O = 5.0 V, V_{FB} = 2.3 V)	I_{Source}	−0.5	−1.0	—	−0.5	−1.0	—	
Output Voltage Swing								V
High State (R_L = 15 k to ground, V_{FB} = 2.3 V)	V_{OH}	5.0	6.2	—	5.0	6.2	—	
Low State (R_L = 15 k to V_{ref}, V_{FB} = 2.7 V)	V_{OL}	—	0.8	1.1	—	0.8	1.1	
CURRENT SENSE SECTION								
Current Sense Input Voltage Gain (Notes 4 & 5)	A_V	2.85	3.0	3.15	2.85	3.0	3.15	V/V
Maximum Current Sense Input Threshold (Note 4)	V_{th}	0.9	1.0	1.1	0.9	1.0	1.1	V
Power Supply Rejection Ratio V_{CC} = 12 V to 25 V, Note 4	PSRR	—	70	—	—	70	—	dB
Input Bias Current	I_{IB}	—	−2.0	−10	—	−2.0	−10	μA
Propagation Delay (Current Sense Input to Output)	$t_{PLH(IN/OUT)}$	—	150	300	—	150	300	ns
OUTPUT SECTION								
Output Voltage								V
Low State (I_{Sink} = 20 mA)	V_{OL}	—	0.1	0.4	—	0.1	0.4	
(I_{Sink} = 200 mA)		—	1.6	2.2	—	1.6	2.2	
High State (I_{Source} = 20 mA)	V_{OH}	13	13.5	—	13	13.5	—	
(I_{Source} = 200 mA)		12	13.4	—	12	13.4	—	
Output Voltage with UVLO Activated V_{CC} = 6.0 V, I_{Sink} = 1.0 mA	$V_{OL(UVLO)}$	—	0.1	1.1	—	0.1	1.1	V
Output Voltage Rise Time (C_L = 1.0 nF, T_J = 25°C)	t_r	—	50	150	—	50	150	ns
Output Voltage Fall Time (C_L = 1.0 nF, T_J = 25°C)	t_f	—	50	150	—	50	150	ns
UNDERVOLTAGE LOCKOUT SECTION								
Start-Up Threshold	V_{th}							V
UCX842A		15	16	17	14.5	16	17.5	
UCX843A		7.8	8.4	9.0	7.8	8.4	9.0	
Minimum Operating Voltage After Turn-On	$V_{CC(min)}$							V
UCX842A		9.0	10	11	8.5	10	11.5	
UCX843A		7.0	7.6	8.2	7.0	7.6	8.2	
PWM SECTION								
Duty Cycle								%
Maximum	DC_{max}	94	96	—	94	96	—	
Minimum	DC_{min}	—	—	0	—	—	0	
TOTAL DEVICE								
Power Supply Current	I_{CC}							mA
Start-Up		—	0.5	1.0	—	0.5	1.0	
(V_{CC} = 6.5 V for UCX843A, 14 V for UCX842A)								
Operating (Note 2)		—	12	17	—	12	17	
Power Supply Zener Voltage (I_{CC} = 25 mA)	V_Z	30	36	—	30	36	—	V

FIGURE 1 — TIMING RESISTOR versus OSCILLATOR FREQUENCY

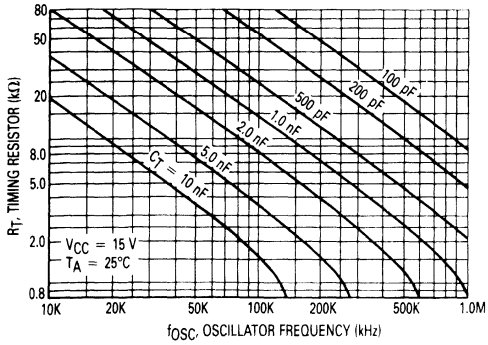


FIGURE 2 — OUTPUT DEAD TIME versus OSCILLATOR FREQUENCY

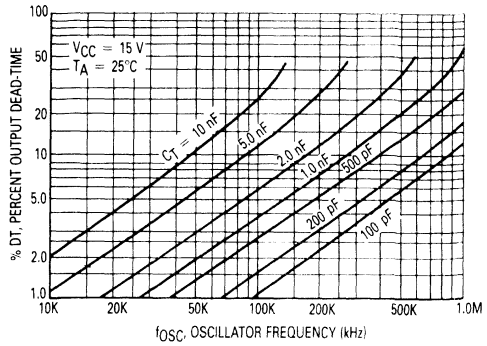


FIGURE 3 — OSCILLATOR DISCHARGE CURRENT versus TEMPERATURE

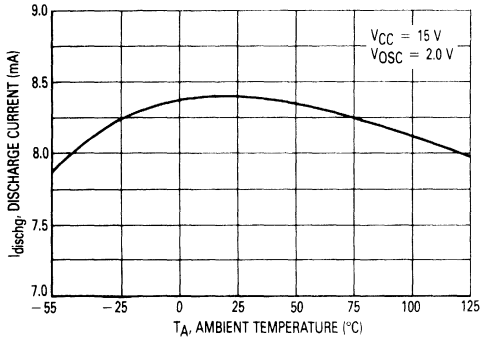


FIGURE 4 — MAXIMUM OUTPUT DUTY CYCLE versus TIMING RESISTOR

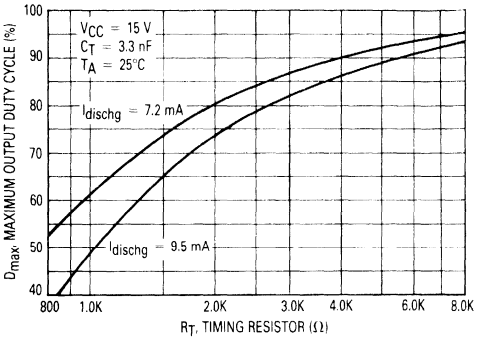


FIGURE 5 — ERROR AMP SMALL SIGNAL TRANSIENT RESPONSE

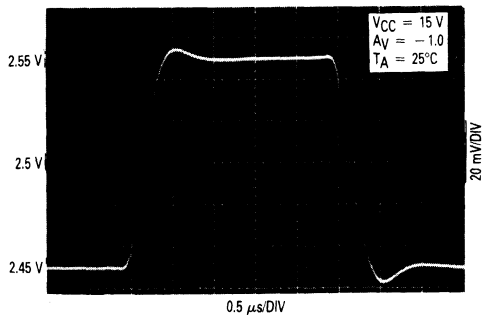


FIGURE 6 — ERROR AMP LARGE SIGNAL TRANSIENT RESPONSE

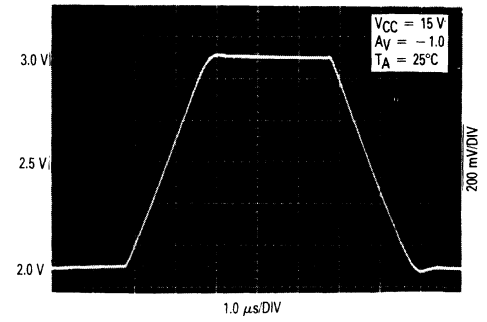


FIGURE 7 — ERROR AMP OPEN-LOOP GAIN AND PHASE versus FREQUENCY

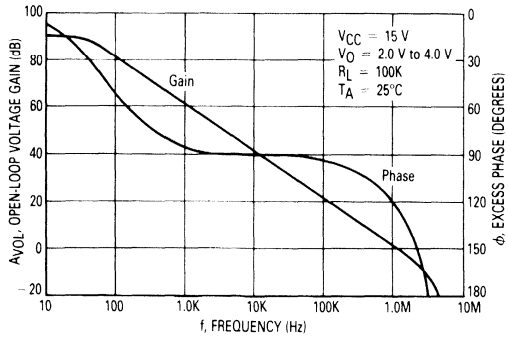


FIGURE 8 — CURRENT SENSE INPUT THRESHOLD versus ERROR AMP OUTPUT VOLTAGE

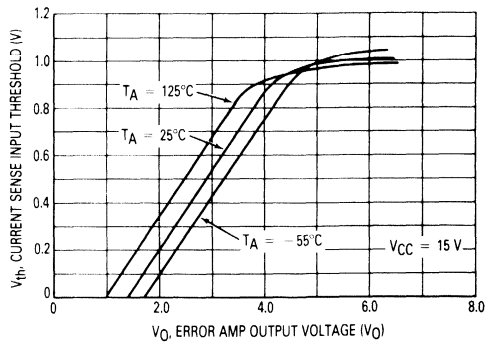


FIGURE 9 — REFERENCE VOLTAGE CHANGE versus SOURCE CURRENT

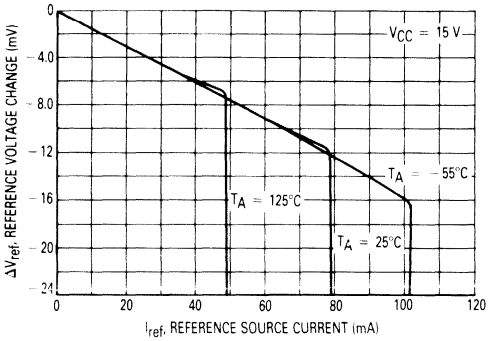


FIGURE 10 — REFERENCE SHORT CIRCUIT CURRENT versus TEMPERATURE

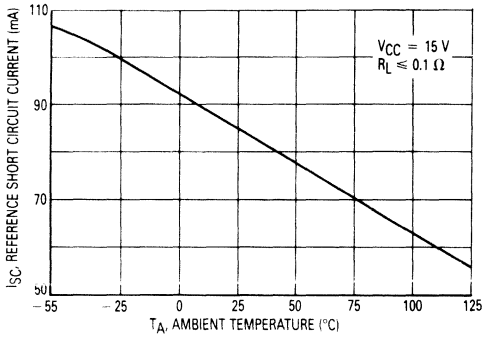


FIGURE 11 — REFERENCE LOAD REGULATION

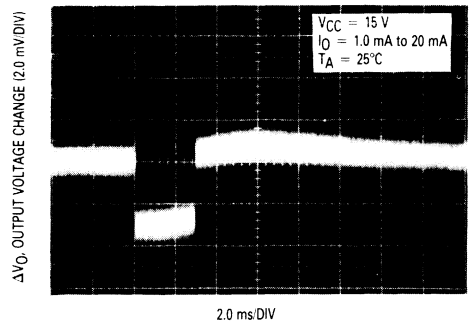


FIGURE 12 — REFERENCE LINE REGULATION

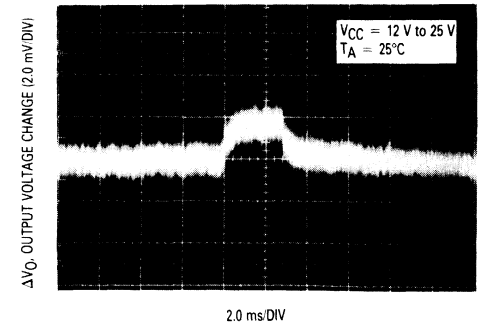


FIGURE 13 — OUTPUT SATURATION VOLTAGE versus LOAD CURRENT

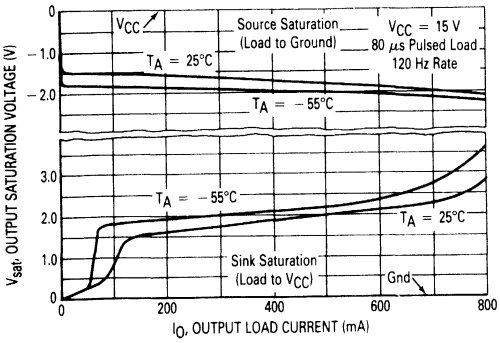


FIGURE 14 — OUTPUT WAVEFORM

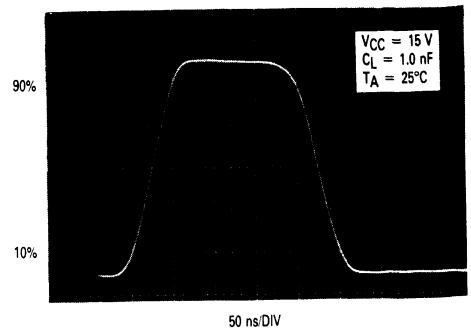


FIGURE 15 — OUTPUT CROSS CONDUCTION

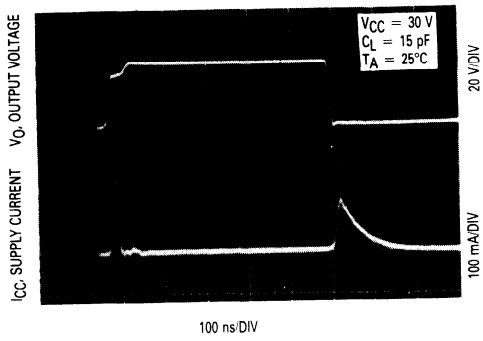


FIGURE 16 — SUPPLY CURRENT versus SUPPLY VOLTAGE

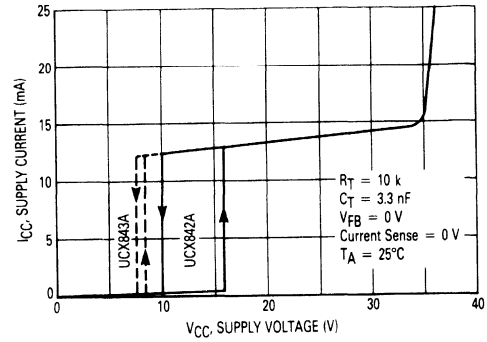
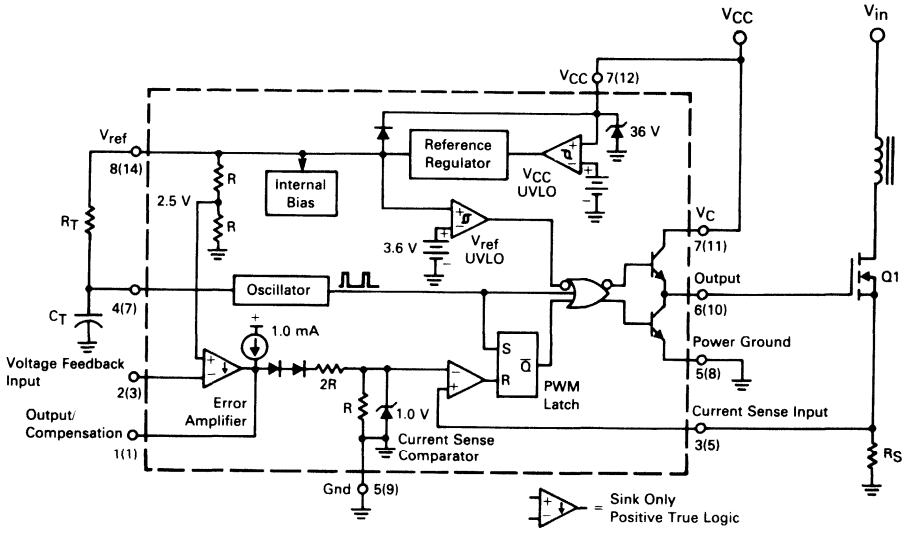
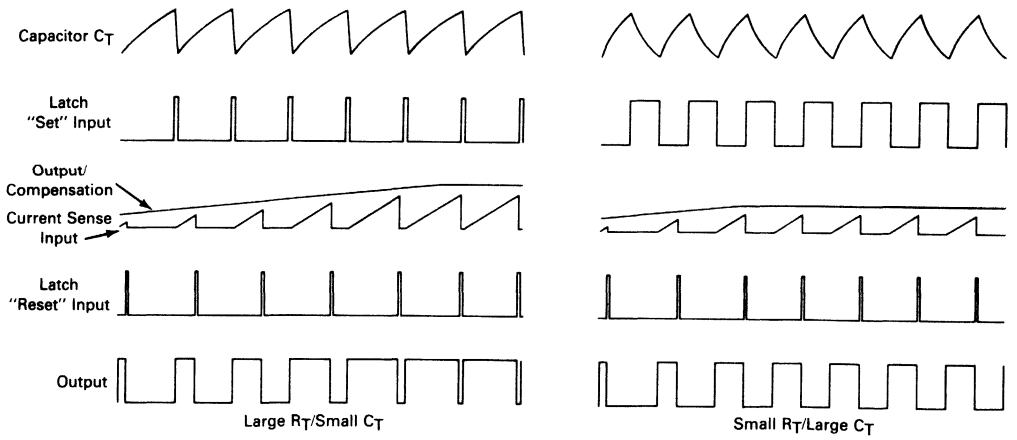


FIGURE 17 — REPRESENTATIVE BLOCK DIAGRAM



Pin numbers adjacent to terminals are for the 8 pin dual-in-line package.
Pin numbers in parenthesis are for the D suffix SO-14 package.

FIGURE 18 — TIMING DIAGRAM



Undervoltage Lockout

Two undervoltage lockout comparators have been incorporated to guarantee that the IC is fully functional before the output stage is enabled. The positive power supply terminal (V_{CC}) and the reference output (V_{ref}) are each monitored by separate comparators. Each has built-in hysteresis to prevent erratic output behavior as their respective thresholds are crossed. The V_{CC} comparator upper and lower thresholds are 16 V/10 V for the UCX842A, and 8.4 V/7.6 V for the UCX843A. The V_{ref} comparator upper and lower thresholds are 3.6 V/3.4 V. The large hysteresis and low start-up current of the UCX842A makes it ideally suited in off-line converter applications where efficient bootstrap start-up tech-

niques are required (Figure 33). The UCX843A is intended for lower voltage DC to DC converter applications. A 36 V zener is connected as a shunt regulator from V_{CC} to ground. Its purpose is to protect the IC from excessive voltage that can occur during system start-up. The minimum operating voltage for the UCX842A is 11 V and 8.2 V for the UCX843A.

Output

These devices contain a single totem pole output stage that was specifically designed for direct drive of power MOSFET's. It is capable of up to ±1.0 A peak drive current and has a typical rise and fall time of 50 ns with a 1.0 nF load. Additional internal circuitry has been added to keep the Output in a sinking mode whenever an undervoltage lockout is active. This characteristic eliminates the need for an external pull-down resistor.

The SO-14 surface mount package provides separate pins for V_C (output supply) and Power Ground. Proper implementation will significantly reduce the level of switching transient noise imposed on the control circuitry. This becomes particularly useful when reducing the $I_{pk(max)}$ clamp level. The separate V_C supply input allows the designer added flexibility in tailoring the drive voltage independent of V_{CC}. A zener clamp is typically connected to this input when driving power MOSFETs in systems where V_{CC} is greater than 20 V. Figure 25 shows proper power and control ground connections in a current sensing power MOSFET application.

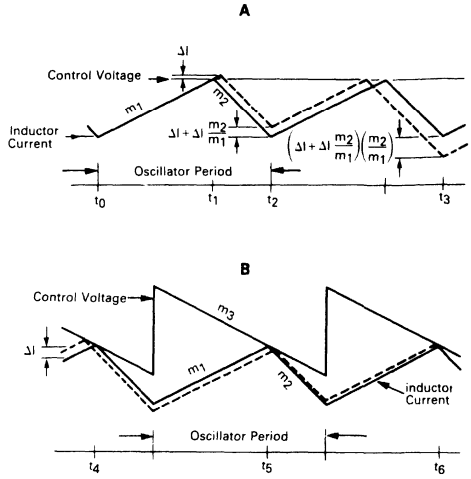
Reference

The 5.0 V bandgap reference is trimmed to ±1.0% tolerance at T_J = 25°C on the UC284XA, and ±2.0% on the UC384XA. Its primary purpose is to supply charging current to the oscillator timing capacitor. The reference has short circuit protection and is capable of providing in excess of 20 mA for powering additional control system circuitry.

Design Considerations

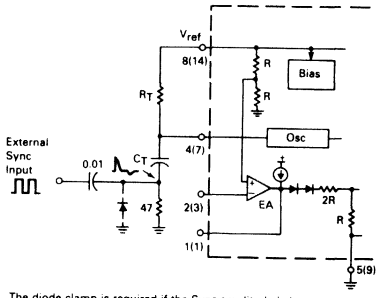
Do not attempt to construct the converter on wire-wrap or plug-in prototype boards. High frequency circuit layout techniques are imperative to prevent pulse-width jitter. This is usually caused by excessive noise pick-up imposed on the Current Sense or Voltage Feedback inputs. Noise immunity can be improved by lowering circuit impedances at these points. The printed circuit layout should contain a ground plane with low-current signal and high-current switch and output grounds returning on separate paths back to the input filter capacitor. Ceramic bypass capacitors (0.1 μF) connected directly to V_{CC}, V_C, and V_{ref} may be required depending upon circuit layout. This provides a low impedance path for filtering the high frequency noise. All high current loops should be kept as short as possible using heavy copper runs to minimize radiated EMI. The Error Amp compensation circuitry and the converter output voltage divider should be located close to the IC and as far as possible from the power switch and other noise generating components.

FIGURE 19 — CONTINUOUS CURRENT WAVEFORMS



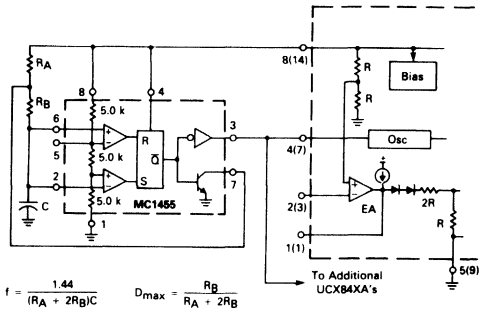
Current mode converters can exhibit subharmonic oscillations when operating at a duty cycle greater than 50% with continuous inductor current. This instability is independent of the regulators closed loop characteristics and is caused by the simultaneous operating conditions of fixed frequency and peak current detecting. Figure 19A shows the phenomenon graphically. At t_0, switch conduction begins, causing the inductor current to rise at a slope of m_1. This slope is a function of the input voltage divided by the inductance. At t_1, the Current Sense Input reaches the threshold established by the control voltage. This causes the switch to turn off and the current to decay at a slope of m_2, until the next oscillator cycle. The unstable condition can be shown if a pertubation is added to the control voltage, resulting in a small ΔI (dashed line). With a fixed oscillator period, the current decay time is reduced, and the minimum current at switch turn-on (t_2) is increased by ΔI + ΔI m_2/m_1. The minimum current at the next cycle (t_3) decreases to (ΔI + ΔI m_2/m_1) (m_2/m_1). This pertubation is multiplied by m_2/m_1 on each succeeding cycle, alternately increasing and decreasing the inductor current at switch turn-on. Several oscillator cycles may be required before the inductor current reaches zero causing the process to commence again. If m_2/m_1 is greather than 1, the converter will be unstable. Figure 19B shows that by adding an artificial ramp that is synchronized with the PWM clock to the control voltage, the ΔI pertubation will decrease to zero on succeeding cycles. This compensating ramp (m_3) must have a slope equal to or slightly greater than $m_2/2$ for stability. With $m_2/2$ slope compensation, the average inductor current follows the control voltage yielding true current mode operation. The compensating ramp can be derived from the oscillator and added to either the Voltage Feedback or Current Sense inputs (Figure 32).

FIGURE 20 — EXTERNAL CLOCK SYNCHRONIZATION



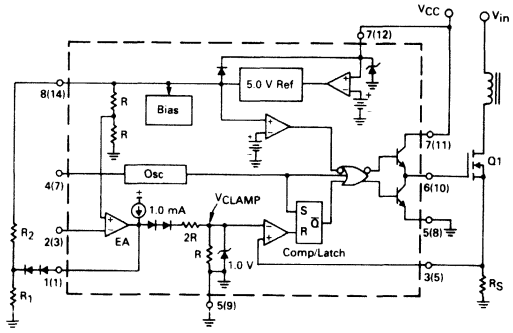
The diode clamp is required if the Sync amplitude is large enough to cause the bottom side of C_T to go more than 300 mV below ground.

FIGURE 21 — EXTERNAL DUTY CYCLE CLAMP AND MULTI UNIT SYNCHRONIZATION



$$f = \frac{1.44}{(R_A + 2R_B)C} \qquad D_{max} = \frac{R_B}{R_A + 2R_B}$$

FIGURE 22 — ADUSTABLE REDUCTION OF CLAMP LEVEL



$$V_{Clamp} \approx \frac{1.67}{\left(\frac{R_2}{R_1} + 1\right)} + 0.33 \times 10^{-3}\left(\frac{R_1 R_2}{R_1 + R_2}\right) \qquad I_{pk(max)} \approx \frac{V_{Clamp}}{R_S}$$

Where: $0 \leq V_{Clamp} \leq 1.0\ V$

FIGURE 23 — SOFT-START CIRCUIT

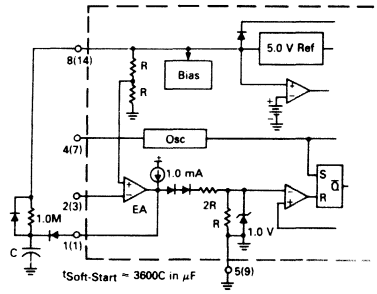
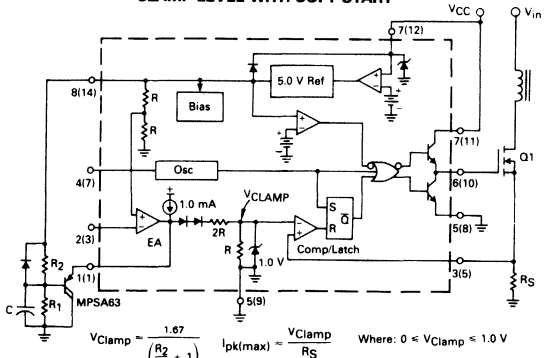


FIGURE 24 — ADJUSTABLE BUFFERED REDUCTION OF CLAMP LEVEL WITH SOFT-START

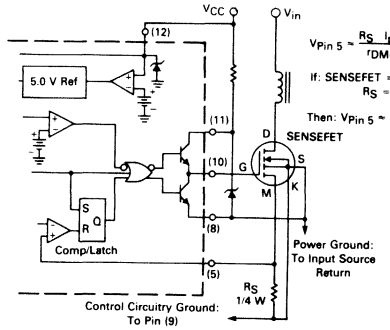


$$V_{Clamp} \approx \frac{1.67}{\left(\frac{R_2}{R_1} + 1\right)} \qquad I_{pk(max)} \approx \frac{V_{Clamp}}{R_S}$$

Where: $0 \leq V_{Clamp} \leq 1.0\ V$

$$t_{SOFTSTART} = -\ln\left[1 - \frac{V_C}{3\,V_{CLAMP}}\right] C\,\frac{R_1 R_2}{R_1 + R_2}$$

FIGURE 25 — CURRENT SENSING POWER MOSFET



$$V_{Pin\ 5} \approx \frac{R_S\ I_{pk}\ r_{DS(on)}}{r_{DM(on)} + R_S}$$

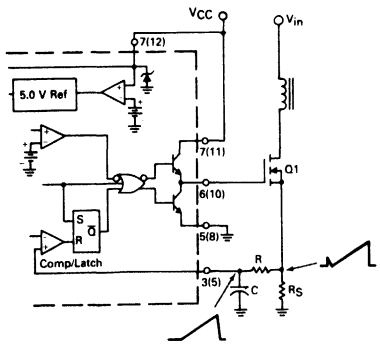
If: SENSEFET = MTP10N10M

$R_S = 200$

Then: $V_{Pin\ 5} \approx 0.075\ I_{pk}$

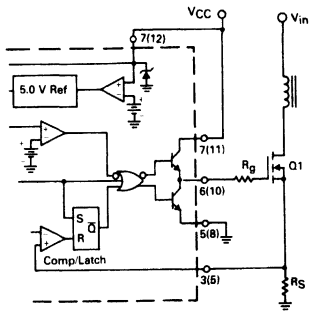
Virtually lossless current sensing can be achieved with the implementation of a SENSEFET power switch. For proper operation during over current conditions, a reduction of the $I_{pk(max)}$ clamp level must be implemented. Refer to Figures 22 and 24.

FIGURE 26 — CURRENT WAVEFORM SPIKE SUPPRESSION



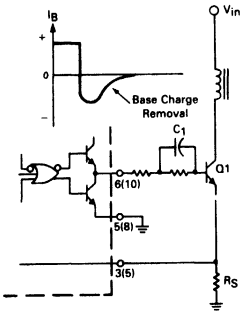
The addition of the RC filter will eliminate instability caused by the leading edge spike on the current waveform.

FIGURE 27 — MOSFET PARASITIC OSCILLATIONS



Series gate resistor R_g will damp any high frequency parasitic oscillations caused by the MOSFET input capacitance and any series wiring inductance in the gate-source circuit.

FIGURE 28 — BIPOLAR TRANSISTOR DRIVE



The totem-pole output can furnish negative base current for enhanced transistor turn-off, with the addition of capacitor C_1.

FIGURE 29 — ISOLATED MOSFET DRIVE

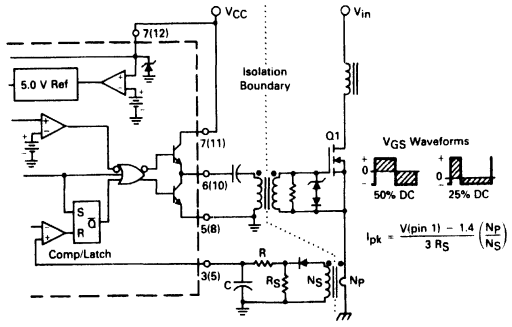
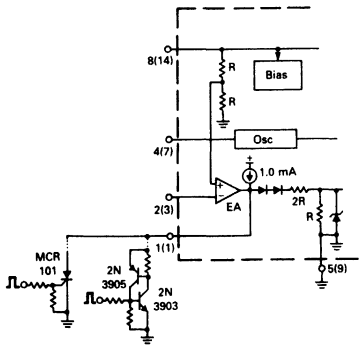
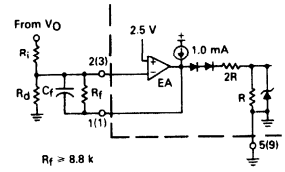


FIGURE 30 — LATCHED SHUTDOWN



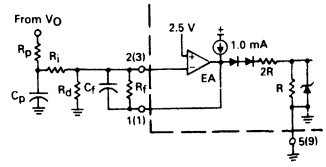
The MCR101 SCR must be selected for a holding of less than 0.5 mA at $T_{A(min)}$. The simple two transistor circuit can be used in place of the SCR as shown. All resistors are 10 k.

FIGURE 31 — ERROR AMPLIFIER COMPENSATION



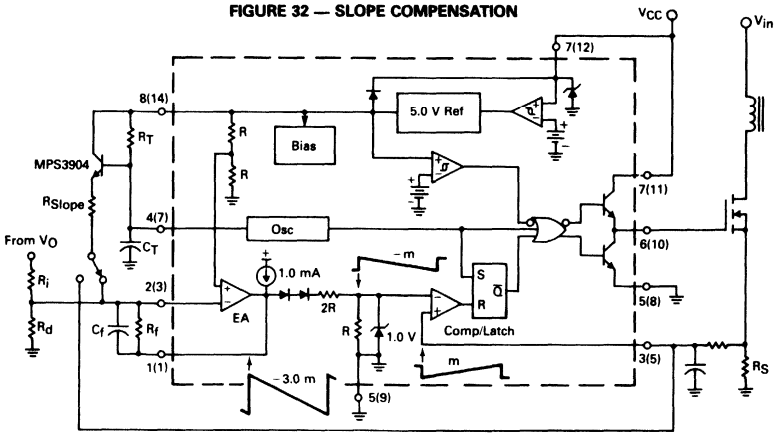
$R_f \geq 8.8$ k

Error Amp compensation circuit for stabilizing any current-mode topology except for boost and flyback converters operating with continuous inductor current.



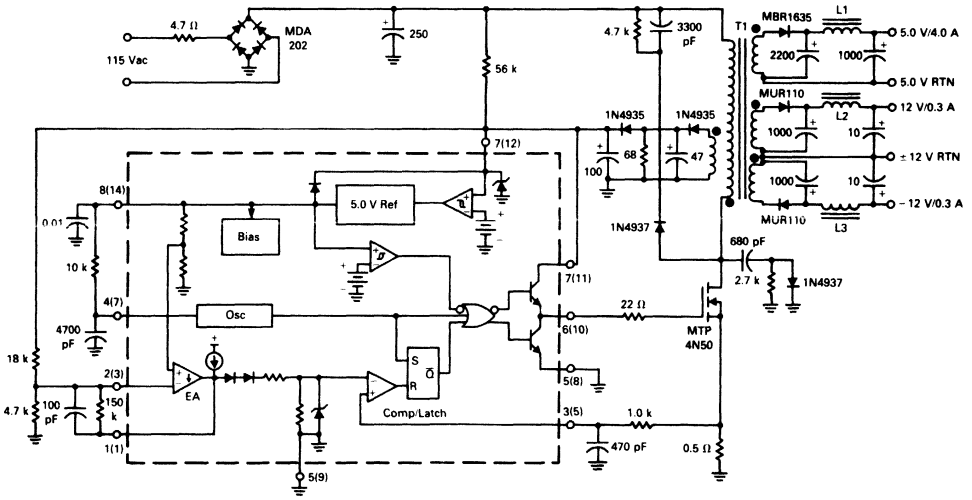
Error Amp compensation circuit for stabilizing current-mode boost and flyback topologies operating with continuous inductor current.

FIGURE 32 — SLOPE COMPENSATION



The buffered oscillator ramp can be resistively summed with either the voltage feedback or current sense inputs to provide slope compensation.

FIGURE 33 — 27 WATT OFF-LINE FLYBACK REGULATOR



T1 — Primary: 45 Turns #26 AWG
Secondary ± 12 V: 9 Turns #30 AWG (2 strands) Bifiliar Wound
Secondary 5.0 V: 4 Turns (six strands) #26 Hexfiliar Wound
Secondary Feedback: 10 Turns #30 AWG (2 strands) Bifiliar Wound
Core: Ferroxcube EC35-3C8
Bobbin: Ferroxcube EC35PCB1
Gap: ≈ 0.10" for a primary inductance of 1.0 mH

L1 — 15 μH at 5.0 A, Coilcraft Z7156.
L2, L3 — 25 μH at 1.0 A, Coilcraft Z7157.

Line Regulation: 5.0 V ±12 V	V_{in} = 95 to 130 Vac	Δ = 50 mV or ±0.5% Δ = 24 mV or ±0.1%
Load Regulation: 5.0 V ±12 V	V_{in} = 115 Vac, I_{out} = 1.0 A to 4.0 A V_{in} = 115 Vac, I_{out} = 100 mA to 300 mA	Δ = 300 mV or ±3.0% Δ = 60 mV or ±0.25%
Output Ripple: 5.0 V ±12 V	V_{in} = 115 Vac	40 mV_{p-p} 80 mV_{p-p}
Efficiency	V_{in} = 115 Vac	70%

All outputs are at nominal load currents unless otherwise noted.

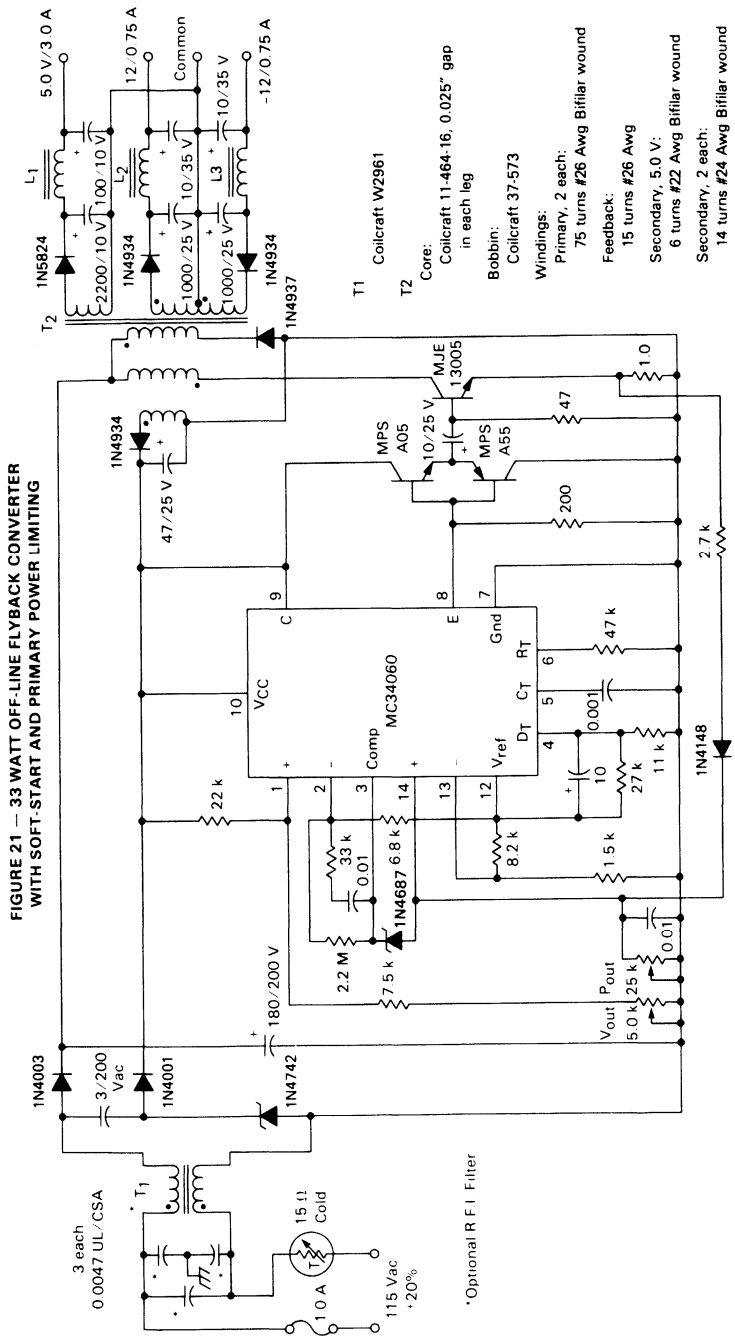


FIGURE 21 — 33 WATT OFF-LINE FLYBACK CONVERTER WITH SOFT-START AND PRIMARY POWER LIMITING

TEST	CONDITIONS	RESULTS
Line Regulation 5.0 V	V_{in} = 95 to 135 Vac, I_O = 3.0 A	20 mV 0.40%
Line Regulation ±12 V	V_{in} = 95 to 135 Vac, I_O = ±0.75 A	52 mV 0.26%
Load Regulation 5.0 V	V_{in} = 115 Vac, I_O = 1.0 to 4.0 A	476 mV 9.5%
Load Regulation ±12 V	V_{in} = 115 Vac, I_O = ±0.4 to ±0.9 A	300 mV 2.5%
Output Ripple 5.0 V	V_{in} = 115 Vac, I_O = 3.0 A	45 mV p-p P.A.R.D
Output Ripple ±12 V	V_{in} = 115 Vac, I_O = ±0.75 A	75 mV p-p P.A.R.D
Efficiency	V_{in} = 115 Vac, I_O 5.0 V = 3.0 A I_O ±12 = ±0.75 A	74%

PIN FUNCTION DESCRIPTION

Pin No.		Function	Description
8-Pin	14-Pin		
1	1	Compensation	This pin is the Error Amplifier output and is made available for loop compensation.
2	3	Voltage Feedback	This is the inverting input of the Error Amplifier. It is normally connected to the switching power supply output through a resistor divider.
3	5	Current Sense	A voltage proportional to inductor current is connected to this input. The PWM uses this information to terminate the output switch conduction.
4	7	R_T/C_T	The Oscillator frequency and maximum Output duty cycle are programmed by connecting resistor R_T to V_{ref} and capacitor C_T to ground. Operation to 500 kHz is possible.
5	—	Gnd	This pin is the combined control circuitry and power ground (8-pin package only).
6	10	Output	This output directly drives the gate of a power MOSFET. Peak currents up to 1.0 A are sourced and sunk by this pin.
7	12	V_{CC}	This pin is the positive supply of the control IC.
8	14	V_{ref}	This is the reference output. It provides charging current for capacitor C_T through resistor R_T.
—	8	Power Ground	This pin is a separate power ground return (14-pin package only) that is connected back to the power source. It is used to reduce the effects of switching transient noise on the control circuitry.
—	11	V_C	The Output high state (V_{OH}) is set by the voltage applied to this pin (14-pin package only). With a separate power source connection, it can reduce the effects of switching transient noise on the control circuitry.
—	9	Gnd	This pin is the control circuitry ground return (14-pin package only) and is connected back to the power source ground.
—	2,4,6,13	NC	No connection (14-pin package only). These pins are not internally connected.

OPERATING DESCRIPTION

The UC3842A, UC3843A series are high performance, fixed frequency, current mode controllers. They are specifically designed for Off-Line and DC-to-DC converter applications offering the designer a cost effective solution with minimal external components. A representative block diagram is shown in Figure 17.

Oscillator

The oscillator frequency is programmed by the values selected for the timing components R_T and C_T. Capacitor C_T is charged from the 5.0 V reference through resistor R_T to approximately 2.8 V and discharged to 1.2 V by an internal current sink. During the discharge of C_T, the oscillator generates an internal blanking pulse that holds the center input of the NOR gate high. This causes the Output to be in a low state, thus producing a controlled amount of output deadtime. Figure 1 shows R_T versus Oscillator Frequency and Figure 2, Output Deadtime versus Frequency, both for given values of C_T. Note that many values of R_T and C_T will give the same oscillator frequency but only one combination will yield a specific output deadtime at a given frequency. The oscillator thresholds are temperature compensated, and the discharge current is trimmed and guaranteed to within ±10% at T_J = 25°C. These internal circuit refinements minimize variations of oscillator frequency and maximum output duty cycle. The results are shown in Figures 3 and 4.

In many noise sensitive applications it may be desirable to frequency-lock the converter to an external system clock. This can be accomplished by applying a clock signal to the circuit shown in Figure 20. For reliable locking, the free-running oscillator frequency should be set about 10% less than the clock frequency. A method for multi unit synchronization is shown in Figure 21. By tailoring the clock waveform, accurate Output duty cycle clamping can be achieved.

Error Amplifier

A fully compensated Error Amplifier with access to the inverting input and output is provided. It features a typical DC voltage gain of 90 dB, and a unity gain bandwidth of 1.0 MHz with 57 degrees of phase margin (Figure 7). The non-inverting input is internally biased at 2.5 V and is not pinned out. The converter output voltage is typically divided down and monitored by the inverting input. The maximum input bias current is −2.0 μA which can cause an output voltage error that is equal to the product of the input bias current and the equivalent input divider source resistance.

The Error Amp Output (Pin 1) is provided for external loop compensation (Figure 31). The output voltage is offset by two diode drops (≈1.4 V) and divided by three before it connects to the inverting input of the Current Sense Comparator. This guarantees that no drive pulses appear at the Output (Pin 6) when pin 1 is at its lowest state (V_{OL}). This occurs when the power supply is operating and the load is removed, or at the beginning of a soft-start interval (Figures 23, 24). The Error Amp minimum feedback resistance is limited by the amplifier's source current (0.5 mA) and the required output voltage (V_{OH}) to reach the comparator's 1.0 V clamp level:

$$R_{f(MIN)} \approx \frac{3.0\ (1.0\ V) + 1.4\ V}{0.5\ mA} = 8800\ \Omega$$

Current Sense Comparator and PWM Latch

The UC3842A, UC3843A operate as a current mode controller, whereby output switch conduction is initiated by the oscillator and terminated when the peak inductor current reaches the threshold level established by the Error Amplifier Output/Compensation (Pin 1). Thus the error signal controls the peak inductor current on a cycle-by-cycle basis. The Current Sense Comparator PWM Latch configuration used ensures that only a single pulse appears at the Output during any given oscillator cycle. The inductor current is converted to a voltage by inserting the ground referenced sense resistor R_S in series with the source of output switch Q1. This voltage is monitored by the Current Sense Input (Pin 3) and compared a level derived from the Error Amp Output. The peak inductor current under normal operating conditions is controlled by the voltage at pin 1 where:

$$I_{pk} = \frac{V_{(Pin\ 1)} - 1.4\ V}{3\ R_S}$$

Abnormal operating conditions occur when the power supply output is overloaded or if output voltage sensing is lost. Under these conditions, the Current Sense Comparator threshold will be internally clamped to 1.0 V. Therefore the maximum peak switch current is:

$$I_{pk(max)} = \frac{1.0\ V}{R_S}$$

When designing a high power switching regulator it becomes desirable to reduce the internal clamp voltage in order to keep the power dissipation of R_S to a reasonable level. A simple method to adjust this voltage is shown in Figure 22. The two external diodes are used to compensate the internal diodes yielding a constant clamp voltage over temperature. Erratic operation due to noise pickup can result if there is an excessive reduction of the $I_{pk(max)}$ clamp voltage.

A narrow spike on the leading edge of the current waveform can usually be observed and may cause the power supply to exhibit an instability when the output is lightly loaded. This spike is due to the power transformer interwinding capacitance and output rectifier recovery time. The addition of an RC filter on the Current Sense Input with a time constant that approximates the spike duration will usually eliminate the instability; refer to Figure 26.

MOTOROLA

UC3844, 45
UC2844, 45

Advance Information

HIGH PERFORMANCE CURRENT MODE CONTROLLER

The UC3844, UC3845 series are high performance fixed frequency current mode controllers. They are specifically designed for Off-Line and DC-to-DC converter applications offering the designer a cost effective solution with minimal external components. These integrated circuits feature an oscillator, a temperature compensated reference, high gain error amplifier, current sensing comparator, and a high current totem pole output ideally suited for driving a power MOSFET.

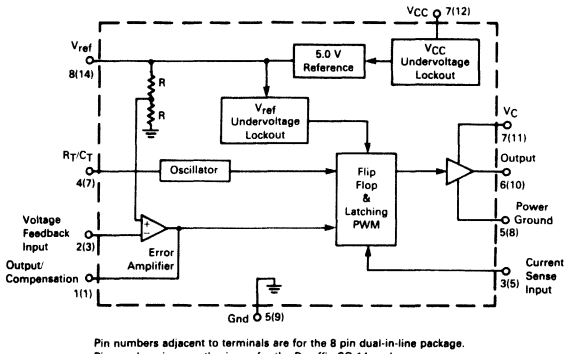
Also included are protective features consisting of input and reference undervoltage lockouts each with hysteresis, cycle-by-cycle current limiting, a latch for single pulse metering, and a flip-flop which blanks the output off every other oscillator cycle, allowing output deadtimes to be programmed from 50% to 70%.

These devices are available in 8-pin dual-in-line ceramic and plastic packages as well as the 14-pin plastic surface mount (SO-14). The SO-14 package has separate power and ground pins for the totem pole output stage.

The UCX844 has UVLO thresholds of 16 V (on) and 10 V (off), ideally suited for off-line converters. The UCX845 is tailored for lower voltage applications having UVLO thresholds of 8.5 V (on) and 7.6 V (off).

- Current Mode Operation to 500 kHz Output Switching Frequency
- Output Deadtime Adjustable from 50% to 70%
- Automatic Feed Forward Compensation
- Latching PWM for Cycle-By-Cycle Current Limiting
- Internally Trimmed Reference with Undervoltage Lockout
- High Current Totem Pole Output
- Input Undervoltage Lockout with Hysteresis
- Low Start-Up and Operating Current
- Direct Interface with Motorola SENSEFET Products

SIMPLIFIED BLOCK DIAGRAM



Pin numbers adjacent to terminals are for the 8 pin dual-in-line package.
Pin numbers in parenthesis are for the D suffix SO-14 package.

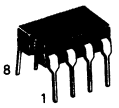
This document contains information on a new product. Specifications and information herein are subject to change without notice.

SENSEFET is a trademark of Motorola Inc.

HIGH PERFORMANCE CURRENT MODE CONTROLLER

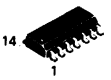
SILICON MONOLITHIC INTEGRATED CIRCUIT

N SUFFIX
PLASTIC PACKAGE
CASE 626-05

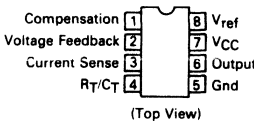


J SUFFIX
CERAMIC PACKAGE
CASE 693-02

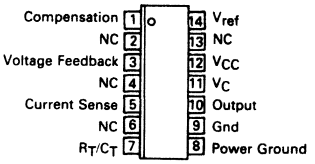
D SUFFIX
PLASTIC PACKAGE
CASE 751A-02
SO-14



PIN CONNECTIONS



(Top View)



(Top View)

ORDERING INFORMATION

Device	Temperature Range	Package
UC3844D	0 to +70°C	SO-14 Plastic DIP
UC3845D		SO-14 Plastic DIP
UC3844N		Plastic DIP
UC3845N		Plastic DIP
UC2844D	−25 to +85°C	SO-14 Plastic DIP
UC2845D		SO-14 Plastic DIP
UC2844J		Ceramic DIP
UC2845J		Ceramic DIP
UC2844N		Plastic DIP
UC2845N		Plastic DIP

MAXIMUM RATING

Rating	Symbol	Value	Unit
Total Power Supply and Zener Current	$(I_{CC}+I_Z)$	30	mA
Output Current, Source or Sink (Note 1)	I_O	1.0	A
Output Energy (Capacitive Load per Cycle)	W	5.0	μJ
Current Sense and Voltage Feedback Inputs	V_{in}	−0.3 to +5.5	V
Error Amp Output Sink Current	I_O	10	mA
Power Dissipation and Thermal Characteristics D Suffix, Plastic Package Maximum Power Dissipation @ T_A = 25°C Thermal Resistance Junction to Air N Suffix, Plastic Package and J Suffix, Ceramic Package Maximum Power Dissipation @ T_A = 25°C Thermal Resistance Junction to Air	 P_D $R_{\theta JA}$ P_D $R_{\theta JA}$	 862 145 1.25 100	 mW °C/W W °C/W
Operating Junction Temperature	T_J	+150	°C
Operating Ambient Temperature UC3844, UC3845 UC2844, UC2845	T_A	 0 to +70 −25 to +85	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = 15 V [Note 2], R_T = 10 k, C_T = 3.3 nF, T_A = T_{low} to T_{high} [Note 3] unless otherwise noted)

Characteristic	Symbol	UC284X			UC384X			Unit
		Min	Typ	Max	Min	Typ	Max	
REFERENCE SECTION								
Reference Output Voltage (I_O = 1.0 mA, T_J = 25°C)	V_{ref}	4.95	5.0	5.05	4.9	5.0	5.1	V
Line Regulation (V_{CC} = 12 V to 25 V)	Reg_{line}	—	2.0	20	—	2.0	20	mV
Load Regulation (I_O = 1.0 mA to 20 mA)	Reg_{load}	—	3.0	25	—	3.0	25	mV
Temperature Stability	T_S	—	0.2	—	—	0.2	—	mV/°C
Total Output Variation over Line, Load, and Temperature	V_{ref}	4.9	—	5.1	4.82	—	5.18	V
Output Noise Voltage (f = 10 Hz to 10 kHz, T_J = 25°C)	V_n	—	50	—	—	50	—	μV
Long Term Stability (T_A = 125°C for 1000 Hours)	S	—	5.0	—	—	5.0	—	mV
Output Short Circuit Current	I_{SC}	−30	−85	−180	−30	−85	−180	mA
OSCILLATOR SECTION								
Frequency T_J = 25°C T_A = T_{low} to T_{high}	f_{OSC}	 47 46	 52 —	 57 60	 47 46	 52 —	 57 60	kHz
Frequency Change with Voltage (V_{CC} = 12 V to 25 V)	$\Delta f_{OSC}/\Delta V$	—	0.2	1.0	—	0.2	1.0	%
Frequency Change with Temperature T_A = T_{low} to T_{high}	$\Delta f_{OSC}/\Delta T$	—	5.0	—	—	5.0	—	%
Oscillator Voltage Swing (Peak-to-Peak)	V_{OSC}	—	1.6	—	—	1.6	—	V
Discharge Current (V_{OSC} = 2.0 V, T_J = 25°C)	I_{dischg}	—	10.8	—	—	10.8	—	mA

Notes: 1. Maximum Package power dissipation limits must be observed.
2. Adjust V_{CC} above the Start-Up threshold before setting to 15 V.
3. Low duty cycle pulse techniques are used during test to maintain junction temperature as close to ambient as possible.
T_{low} = 0°C for UC3844, UC3845 = −25°C for UC2844, UC2845
T_{high} = +70°C for UC3844, UC3845 = +85°C for UC2844, UC2845

ELECTRICAL CHARACTERISTICS (V_{CC} = 15 V [Note 2], R_T = 10 k, C_T = 3.3 nF, T_A = T_{low} to T_{high} [Note 3] unless otherwise noted)

Characteristic	Symbol	UC284X			UC384X			Unit
		Min	Typ	Max	Min	Typ	Max	
ERROR AMPLIFIER SECTION								
Voltage Feedback Input (V_O = 2.5 V)	V_{FB}	2.45	2.5	2.55	2.42	2.5	2.58	V
Input Bias Current (V_{FB} = 5.0 V)	I_{IB}	—	−0.1	−1.0	—	−0.1	−2.0	μA
Open-Loop Voltage Gain (V_O = 2.0 V to 4.0 V)	A_{VOL}	65	90	—	65	90	—	dB
Unity Gain Bandwidth (T_J = 25°C)	BW	0.7	1.0	—	0.7	1.0	—	MHz
Power Supply Rejection Ratio (V_{CC} = 12 V to 25 V)	PSRR	60	70	—	60	70	—	dB
Output Current								mA
Sink (V_O = 1.1 V, V_{FB} = 2.7 V)	I_{Sink}	2.0	12	—	2.0	12	—	
Source (V_O = 5.0 V, V_{FB} = 2.3 V)	I_{Source}	−0.5	−1.0	—	−0.5	−1.0	—	
Output Voltage Swing								V
High State (R_L = 15 k to ground, V_{FB} = 2.3 V)	V_{OH}	5.0	6.2	—	5.0	6.2	—	
Low State (R_L = 15 k to V_{ref}, V_{FB} = 2.7 V)	V_{OL}	—	0.8	1.1	—	0.8	1.1	
CURRENT SENSE SECTION								
Current Sense Input Voltage Gain (Notes 4 & 5)	A_V	2.85	3.0	3.15	2.85	3.0	3.15	V/V
Maximum Current Sense Input Threshold (Note 4)	V_{th}	0.9	1.0	1.1	0.9	1.0	1.1	V
Power Supply Rejection Ratio V_{CC} = 12 V to 25 V (Note 4)	PSRR	—	70	—	—	70	—	dB
Input Bias Current	I_{IB}	—	−2.0	−10	—	−2.0	−10	μA
Propagation Delay (Current Sense Input to Output)	$t_{PLH(IN/OUT)}$	—	150	300	—	150	300	ns
OUTPUT SECTION								
Output Voltage								V
Low State (I_{Sink} = 20 mA)	V_{OL}	—	0.1	0.4	—	0.1	0.4	
(I_{Sink} = 200 mA)		—	1.6	2.2	—	1.6	2.2	
High State (I_{Source} = 20 mA)	V_{OH}	13	13.5	—	13	13.5	—	
(I_{Source} = 200 mA)		12	13.4	—	12	13.4	—	
Output Voltage with UVLO Activated V_{CC} = 6.0 V, I_{Sink} = 1.0 mA	$V_{OL(UVLO)}$	—	0.1	1.1	—	0.1	1.1	V
Output Voltage Rise Time (C_L = 1.0 nF, T_J = 25°C)	t_r	—	50	150	—	50	150	ns
Output Voltage Fall Time (C_L = 1.0 nF, T_J = 25°C)	t_f	—	50	150	—	50	150	ns
UNDERVOLTAGE LOCKOUT SECTION								
Start-Up Threshold	V_{th}							V
UCX844		15	16	17	14.5	16	17.5	
UCX845		7.8	8.4	9.0	7.8	8.4	9.0	
Minimum Operating Voltage After Turn-On	$V_{CC(min)}$							V
UCX844		9.0	10	11	8.5	10	11.5	
UCX845		7.0	7.6	8.2	7.0	7.6	8.2	
PWM SECTION								
Duty Cycle								%
Maximum	DC_{max}	46	48	50	47	48	50	
Minimum	DC_{min}	—	—	0	—	—	0	
TOTAL DEVICE								
Power Supply Current	I_{CC}							mA
Start-Up		—	0.5	1.0	—	0.5	1.0	
(V_{CC} = 6.5 V for UCX845, 14 V for UCX844)								
Operating (Note 2)		—	12	17	—	12	17	
Power Supply Zener Voltage (I_{CC} = 25 mA)	V_Z	30	36	—	30	36	—	V

Notes: 4. This parameter is measured at the latch trip point with V_{FB} = 0 V.

5. Comparator gain is defined as: $A_V = \frac{\Delta V \text{ Output/Compensation}}{\Delta V \text{ Current Sense Input}}$

FIGURE 1 — TIMING RESISTOR versus OSCILLATOR FREQUENCY

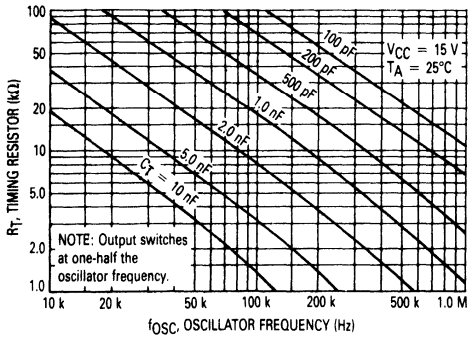


FIGURE 2 — OUTPUT DEAD TIME versus OSCILLATOR FREQUENCY

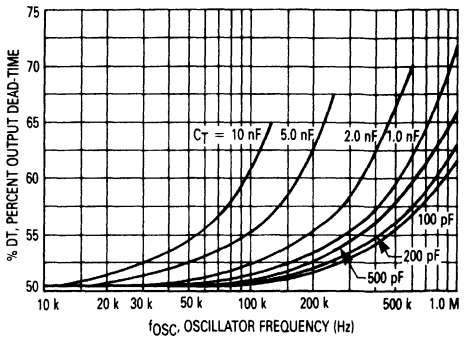


FIGURE 3 — ERROR AMP SMALL SIGNAL TRANSIENT RESPONSE

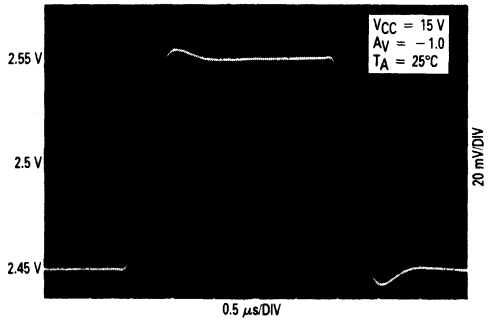


FIGURE 4 — ERROR AMP LARGE SIGNAL TRANSIENT RESPONSE

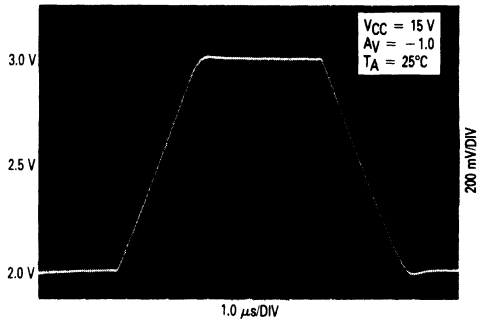


FIGURE 5 — ERROR AMP OPEN-LOOP GAIN AND PHASE versus FREQUENCY

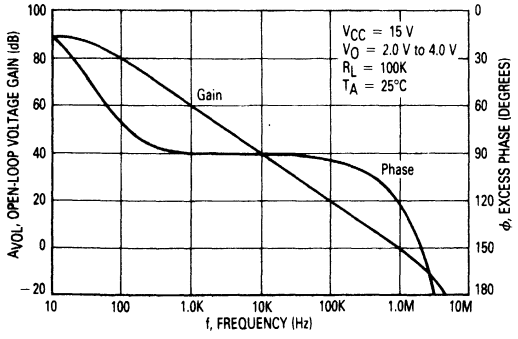


FIGURE 6 — CURRENT SENSE INPUT THRESHOLD versus ERROR AMP OUTPUT VOLTAGE

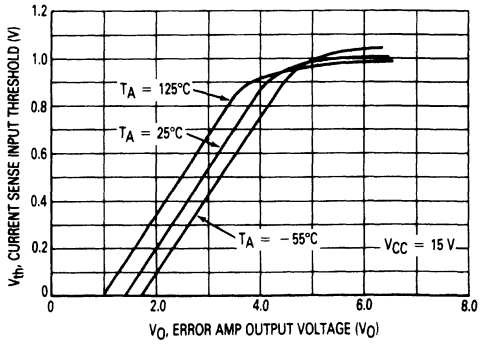


FIGURE 7 — REFERENCE VOLTAGE CHANGE versus SOURCE CURRENT

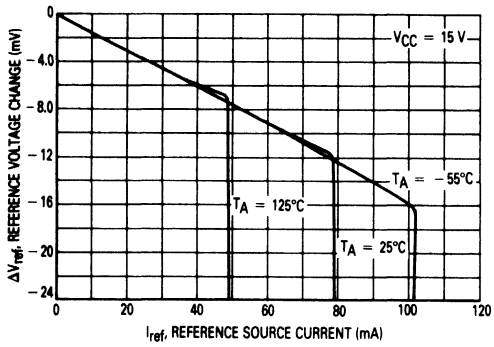


FIGURE 8 — REFERENCE SHORT CIRCUIT CURRENT versus TEMPERATURE

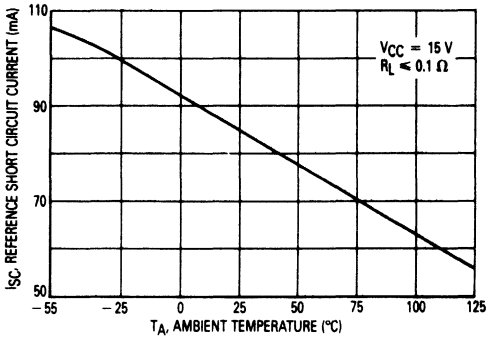


FIGURE 9 — REFERENCE LOAD REGULATION

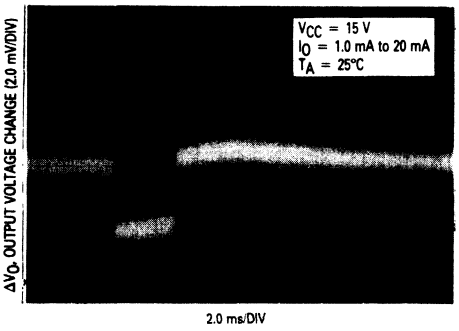


FIGURE 10 — REFERENCE LINE REGULATION

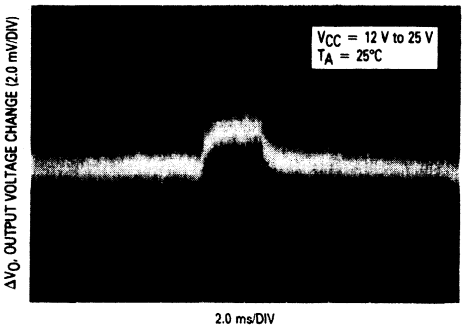


FIGURE 11 — OUTPUT SATURATION VOLTAGE versus LOAD CURRENT

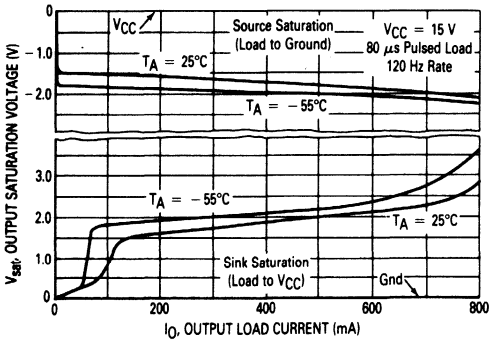


FIGURE 12 — OUTPUT WAVEFORM

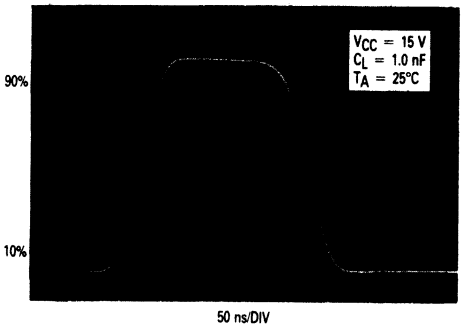


FIGURE 13 — OUTPUT CROSS CONDUCTION

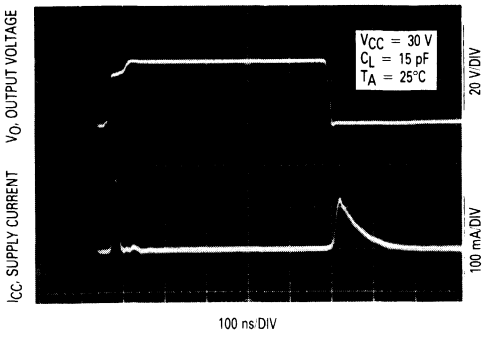
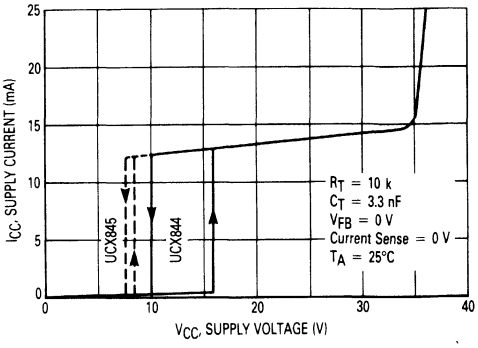


FIGURE 14 — SUPPLY CURRENT versus SUPPLY VOLTAGE



PIN FUNCTION DESCRIPTION

Pin No.		Function	Description
8-Pin	14-Pin		
1	1	Compensation	This pin is the Error Amplifier output and is made available for loop compensation.
2	3	Voltage Feedback	This is the inverting input of the Error Amplifier. It is normally connected to the switching power supply output through a resistor divider.
3	5	Current Sense	A voltage proportional to inductor current is connected to this input. The PWM uses this information to terminate the output switch conduction.
4	7	R_T/C_T	The Oscillator frequency and maximum Output duty cycle are programmed by connecting resistor R_T to V_{ref} and capacitor C_T to ground. Oscillator operation to 1.0 MHz is possible.
5	—	Gnd	This pin is the combined control circuitry and power ground (8-pin package only).
6	10	Output	This output directly drives the gate of a power MOSFET. Peak currents up to 1.0 A are sourced and sunk by this pin. The output switches at one-half the oscillator frequency.
7	12	V_{CC}	This pin is the positive supply of the control IC.
8	14	V_{ref}	This is the reference output. It provides charging current for capacitor C_T through resistor R_T.
—	8	Power Ground	This pin is a separate power ground return (14-pin package only) that is connected back to the power source. It is used to reduce the effects of switching transient noise on the control circuitry.
—	11	V_C	The Output high state (V_{OH}) is set by the voltage applied to this pin (14-pin package only). With a separate power source connection, it can reduce the effects of switching transient noise on the control circuitry.
—	9	Gnd	This pin is the control circuitry ground return (14-pin package only) and is connected back to the power source ground.
—	2,4,6,13	NC	No connection (14-pin package only). These pins are not internally connected.

OPERATING DESCRIPTION

The UC3844, UC3845 series are high performance, fixed frequency, current mode controllers. They are specifically designed for Off-Line and DC-to-DC converter applications offering the designer a cost effective solution with minimal external components. A representative block diagram is shown in Figure 15.

Oscillator

The oscillator frequency is programmed by the values selected for the timing components R_T and C_T. Capacitor C_T is charged from the 5.0 V reference through resistor R_T to approximately 2.8 V and discharged to 1.2 V by an internal current sink. During the discharge of C_T, the oscillator generates an internal blanking pulse that holds the center input of the NOR gate high. This causes the Output to be in a low state, thus producing a controlled amount of output deadtime. An internal flip-flop has been incorporated in the UCX844/5 which blanks the output off every other clock cycle by holding one of the inputs of the NOR gate high. This in combination with the C_T discharge period yields output deadtimes programmable from 50% to 70%. Figure 1 shows R_T versus Oscillator Frequency and Figure 2, Output Deadtime versus Frequency, both for given values of C_T. Note that many values of R_T and C_T will give the same oscillator frequency but only one combination will yield a specific output deadtime at a given frequency.

In many noise sensitive applications it may be desirable to frequency-lock the converter to an external system clock. This can be accomplished by applying a clock signal to the circuit shown in Figure 17. For reliable locking, the free-running oscillator frequency should be set about 10% less than the clock frequency. A method for multi unit synchronization is shown in Figure 18. By tailoring the clock waveform, accurate Output duty cycle clamping can be achieved to realize output deadtimes of greater than 70%.

Error Amplifier

A fully compensated Error Amplifier with access to the inverting input and output is provided. It features a typical DC voltage gain of 90 dB, and a unity gain bandwidth of 1.0 MHz with 57 degrees of phase margin (Figure 5). The non-inverting input is internally biased at 2.5 V and is not pinned out. The converter output voltage is typically divided down and monitored by the inverting input. The maximum input bias current is $-2.0\ \mu A$ which can cause an output voltage error that is equal to the product of the input bias current and the equivalent input divider source resistance.

The Error Amp Output (Pin 1) is provided for external loop compensation (Figure 28). The output voltage is offset by two diode drops ($\approx$1.4 V) and divided by three before it connects to the inverting input of the Current Sense Comparator. This guarantees that no drive pulses appear at the Output (Pin 6) when Pin 1 is at its lowest state (V_{OL}). This occurs when the power supply is operating and the load is removed, or at the beginning of a soft-start interval (Figures 20, 21). The Error Amp minimum feedback resistance is limited by the amplifier's source current (0.5 mA) and the required output voltage (V_{OH}) to reach the comparator's 1.0 V clamp level:

$$R_{f(MIN)} \approx \frac{3.0\ (1.0\ V) + 1.4\ V}{0.5\ mA} = 8800\ \Omega$$

Current Sense Comparator and PWM Latch

The UC3844, UC3845 operate as a current mode controller, whereby output switch conduction is initiated by the oscillator and terminated when the peak inductor current reaches the threshold level established by the Error Amplifier Output/Compensation (Pin 1). Thus the error signal controls the peak inductor current on a cycle-by-cycle basis. The Current Sense Comparator PWM Latch configuration used ensures that only a single pulse appears at the Output during any given oscillator cycle. The inductor current is converted to a voltage by inserting the ground referenced sense resistor R_S in series with the source of output switch Q1. This voltage is monitored by the Current Sense Input (Pin 3) and compared to a level derived from the Error Amp Output. The peak inductor current under normal operating conditions is controlled by the voltage at pin 1 where:

$$I_{pk} = \frac{V_{(Pin\ 1)} - 1.4\ V}{3\ R_S}$$

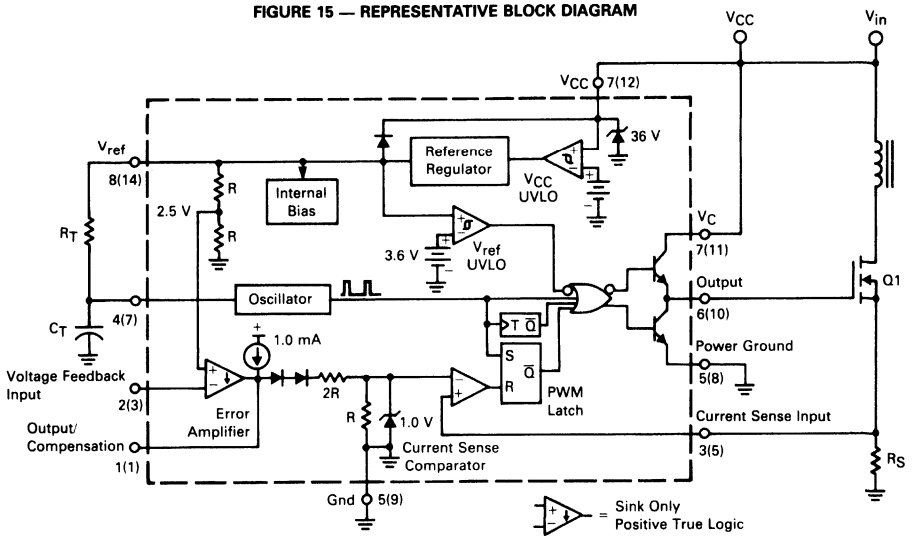
Abnormal operating conditions occur when the power supply output is overloaded or if output voltage sensing is lost. Under these conditions, the Current Sense Comparator threshold will be internally clamped to 1.0 V. Therefore the maximum peak switch current is:

$$I_{pk(max)} = \frac{1.0\ V}{R_S}$$

When designing a high power switching regulator it becomes desirable to reduce the internal clamp voltage in order to keep the power dissipation of R_S to a reasonable level. A simple method to adjust this voltage is shown in Figure 19. The two external diodes are used to compensate the internal diodes yielding a constant clamp voltage over temperature. Erratic operation due to noise pickup can result if there is an excessive reduction of the $I_{pk(max)}$ clamp voltage.

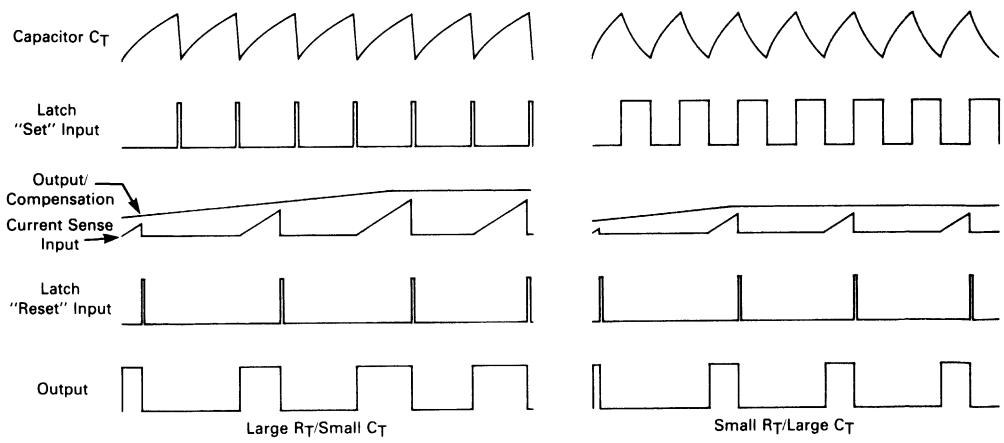
A narrow spike on the leading edge of the current waveform can usually be observed and may cause the power supply to exhibit an instability when the output is lightly loaded. This spike is due to the power transformer interwinding capacitance and output rectifier recovery time. The addition of an RC filter on the Current Sense Input with a time constant that approximates the spike duration will usually eliminate the instability; refer to Figure 23.

FIGURE 15 — REPRESENTATIVE BLOCK DIAGRAM



Pin numbers adjacent to terminals are for the 8 pin dual-in-line package.
Pin numbers in parenthesis are for the D suffix SO-14 package.

FIGURE 16 — TIMING DIAGRAM



Undervoltage Lockout

Two undervoltage lockout comparators have been incorporated to guarantee that the IC is fully functional before the output stage is enabled. The positive power supply terminal (V_{CC}) and the reference output (V_{ref}) are each monitored by separate comparators. Each has built-in hysteresis to prevent erratic output behavior as their respective thresholds are crossed. The V_{CC} comparator upper and lower thresholds are 16 V/10 V for the UCX844, and 8.4 V/7.6 V for the UCX845. The V_{ref} comparator upper and lower thresholds are 3.6 V/3.4 V. The large hysteresis and low start-up current of the UCX844 makes it ideally suited in off-line converter applications where efficient bootstrap start-up techniques are required (Figure 29). The UCX845 is intended for lower voltage DC-to-DC converter applications. A 36 V zener is connected as a shunt regulator from V_{CC} to ground. Its purpose is to protect the IC from excessive voltage that can occur during system start-up. The minimum operating voltage for the UCX844 is 11 V and 8.2 V for the UCX845.

Output

These devices contain a single totem pole output stage that was specifically designed for direct drive of power MOSFET's. It is capable of up to ±1.0 A peak drive current and has a typical rise and fall time of 50 ns with a 1.0 nF load. Additional internal circuitry has been added to keep the Output in a sinking mode whenever an undervoltage lockout is active. This characteristic eliminates the need for an external pull-down resistor.

The SO-14 surface mount package provides separate pins for V_C (output supply) and Power Ground. Proper implementation will significantly reduce the level of switching transient noise imposed on the control circuitry. This becomes particularly useful when reducing the $I_{pk(max)}$ clamp level. The separate V_C supply input allows the designer added flexibility in tailoring the drive voltage independent of V_{CC}. A zener clamp is typically connected to this input when driving power MOSFETs in systems where V_{CC} is greater than 20 V. Figure 22 shows proper power and control ground connections in a current sensing power MOSFET application.

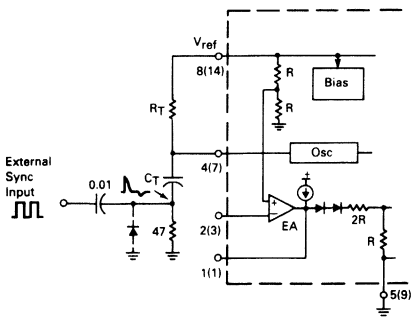
Reference

The 5.0 V bandgap reference is trimmed to ±1.0% tolerance at T_J = 25°C on the UC284X, and ±2.0% on the UC384X. Its primary purpose is to supply charging current to the oscillator timing capacitor. The reference has short circuit protection and is capable of providing in excess of 20 mA for powering additional control system circuitry.

Design Considerations

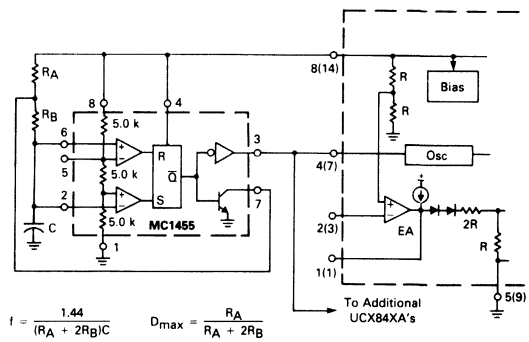
Do not attempt to construct the converter on wire-wrap or plug-in prototype boards. High frequency circuit layout techniques are imperative to prevent pulse-width jitter. This is usually caused by excessive noise pick-up imposed on the Current Sense or Voltage Feedback inputs. Noise immunity can be improved by lowering circuit impedances at these points. The printed circuit layout should contain a ground plane with low-current signal and high-current switch and output grounds returning on separate paths back to the input filter capacitor. Ceramic bypass capacitors (0.1 μF) connected directly to V_{CC}, V_C, and V_{ref} may be required depending upon circuit layout. This provides a low impedance path for filtering the high frequency noise. All high current loops should be kept as short as possible using heavy copper runs to minimize radiated EMI. The Error Amp compensation circuitry and the converter output voltage divider should be located close to the IC and as far as possible from the power switch and other noise generating components.

FIGURE 17 — EXTERNAL CLOCK SYNCHRONIZATION



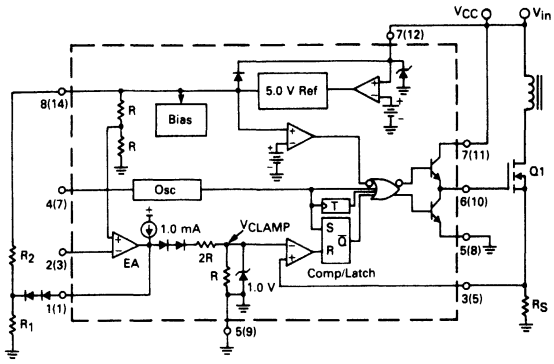
The diode clamp is required if the Sync amplitude is large enough to cause the bottom side of C_T to go more than 300 mV below ground.

FIGURE 18 — EXTERNAL DUTY CYCLE CLAMP AND MULTI UNIT SYNCHRONIZATION



$$f = \frac{1.44}{(R_A + 2R_B)C} \qquad D_{max} = \frac{R_A}{R_A + 2R_B}$$

FIGURE 19 — ADUSTABLE REDUCTION OF CLAMP LEVEL



$$V_{Clamp} \approx \frac{1.67}{\left(\frac{R_2}{R_1}+1\right)} + 0.33 \times 10^{-3}\left(\frac{R_1 R_2}{R_1 + R_2}\right) \qquad I_{pk(max)} \approx \frac{V_{Clamp}}{R_S}$$

Where: $0 \leq V_{Clamp} \leq 1.0\ V$

FIGURE 20 — SOFT-START CIRCUIT

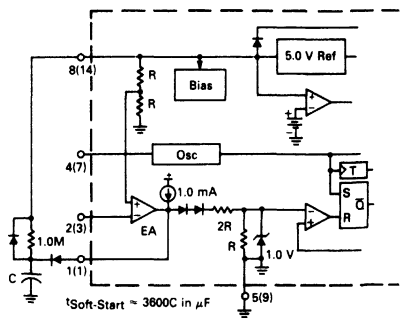
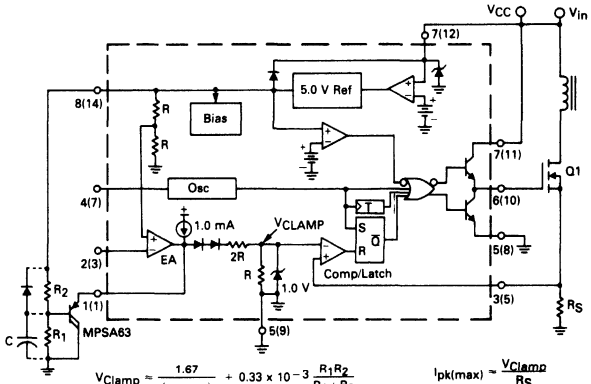


FIGURE 21 — ADJUSTABLE BUFFERED REDUCTION OF CLAMP LEVEL WITH SOFT-START

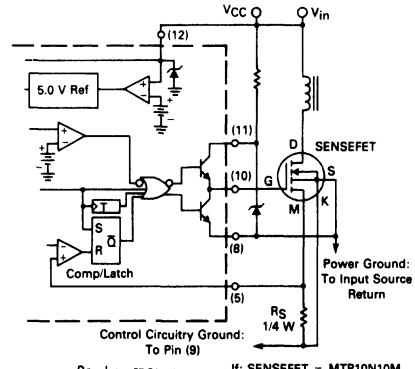


$$V_{Clamp} \approx \frac{1.67}{\left(\frac{R_2}{R_1}+1\right)} + 0.33 \times 10^{-3}\,\frac{R_1 R_2}{R_1 + R_2} \qquad I_{pk(max)} \approx \frac{V_{Clamp}}{R_S}$$

Where: $0 \leq V_{Clamp} \leq 1.0\ V$

$$t_{SOFT\text{-}START} = -\ln\left[1 - \frac{V_C}{3V_{CLAMP}}\right] C\,\frac{R_1 R_2}{R_1 + R_2}$$

FIGURE 22 — CURRENT SENSING POWER MOSFET



$$V_{Pin\ 5} \approx \frac{R_S\ I_{pk}\ r_{DS(on)}}{r_{DM(on)} + R_S}$$

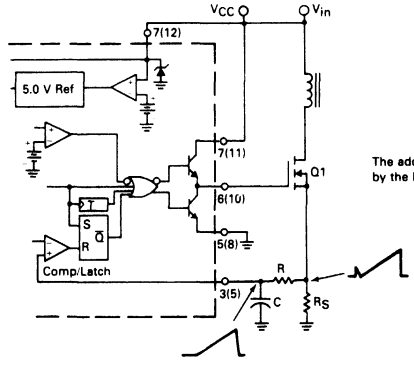
If: SENSEFET = MTP10N10M

$R_S = 200$

Then: $V_{Pin\ 5} \approx 0.075\ I_{pk}$

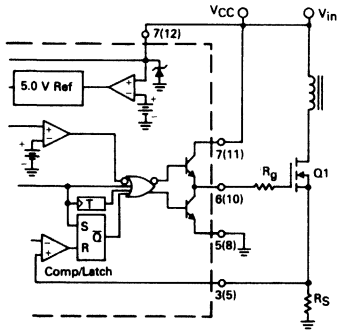
Virtually lossless current sensing can be achieved with the implementation of a SENSEFET power switch. For proper operation during over current conditions, a reduction of the $I_{pk(max)}$ clamp level must be implemented. Refer to Figures 19 and 21.

FIGURE 23 — CURRENT WAVEFORM SPIKE SUPPRESSION



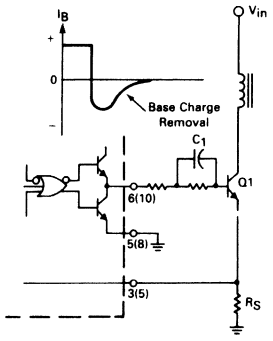
The addition of the RC filter will eliminate instability caused by the leading edge spike on the current waveform.

FIGURE 24 — MOSFET PARASITIC OSCILLATIONS



Series gate resistor R_g will damp any high frequency parasitic oscillations caused by the MOSFET input capacitance and any series wiring inductance in the gate-source circuit.

FIGURE 25 — BIPOLAR TRANSISTOR DRIVE



The totem-pole output can furnish negative base current for enhanced transistor turn-off, with the addition of capacitor C_1.

FIGURE 26 — ISOLATED MOSFET DRIVE

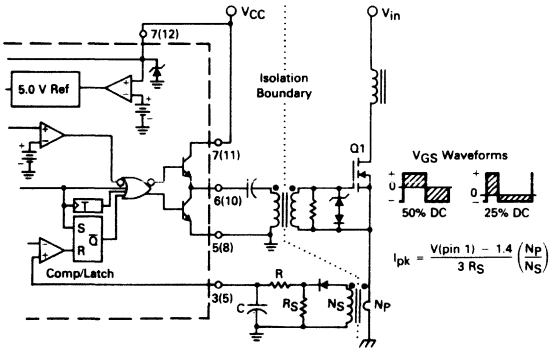
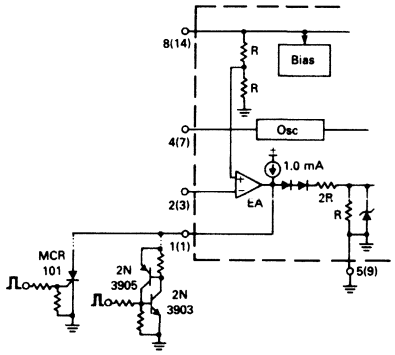
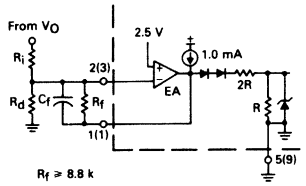


FIGURE 27 — LATCHED SHUTDOWN

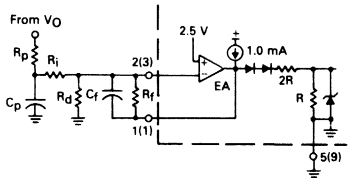


The MCR101 SCR must be selected for a holding of less than 0.5 mA at $T_{A(min)}$. The simple two transistor circuit can be used in place of the SCR as shown. All resistors are 10 k.

FIGURE 28 — ERROR AMPLIFIER COMPENSATION

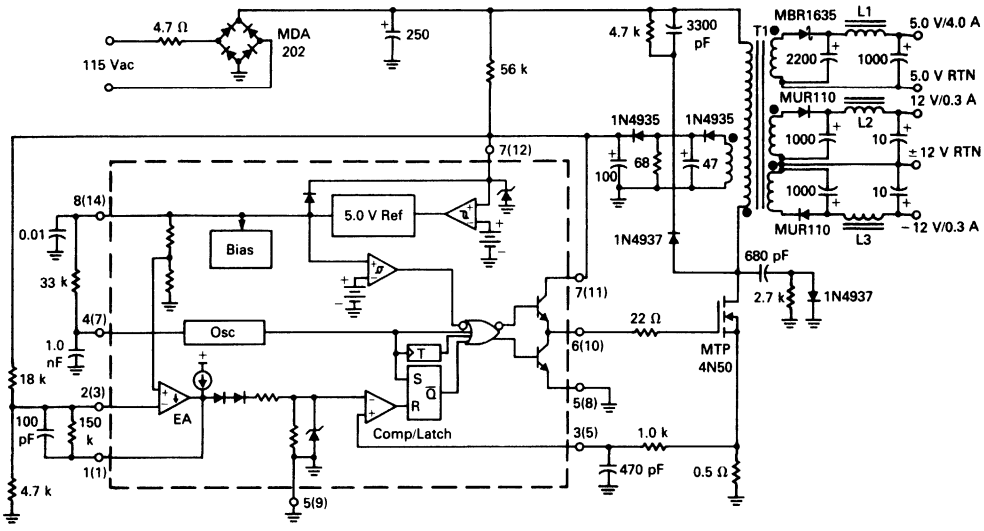


Error Amp compensation circuit for stabilizing any current-mode topology except for boost and flyback converters operating with continuous inductor current.



Error Amp compensation circuit for stabilizing current-mode boost and flyback topologies operating with continuous inductor current.

FIGURE 29 — 27 WATT OFF-LINE FLYBACK REGULATOR



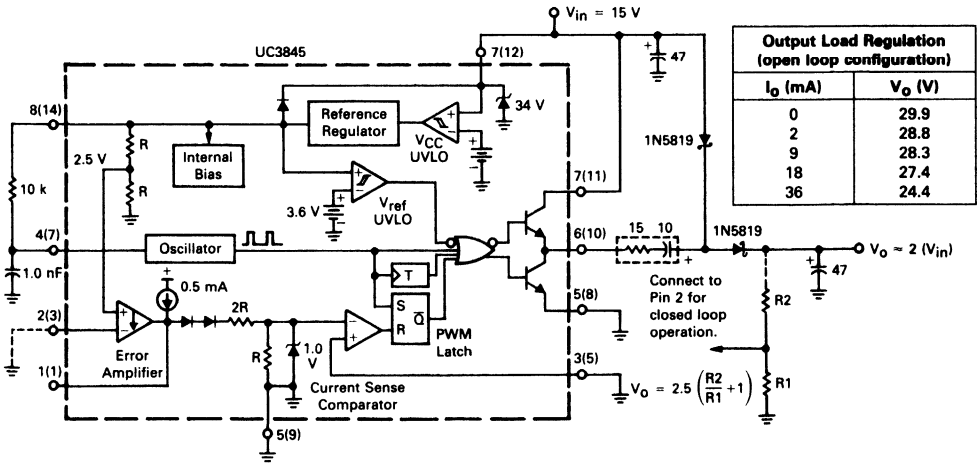
T1 — Primary: 45 Turns #26 AWG
Secondary ± 12 V: 9 Turns #30 AWG (2 strands) Bifiliar Wound
Secondary 5.0 V: 4 Turns (six strands) #26 Hexfiliar Wound
Secondary Feedback: 10 Turns #30 AWG (2 strands) Bifiliar Wound
Core: Ferroxcube EC35-3C8
Bobbin: Ferroxcube EC35PCB1
Gap: ≈ 0.10" for a primary inductance of 1.0 mH

L1 — 15 μH at 5.0 A, Coilcraft Z7156.
L2, L3 — 25 μH at 1.0 A, Coilcraft Z7157.

Line Regulation: 5.0 V ±12 V	V_{in} = 95 to 130 Vac	Δ = 50 mV or ±0.5% Δ = 24 mV or ±0.1%
Load Regulation: 5.0 V ±12 V	V_{in} = 115 Vac, I_{out} = 1.0 A to 4.0 A V_{in} = 115 Vac, I_{out} = 100 mA to 300 mA	Δ = 300 mV or ±3.0% Δ = 60 mV or ±0.25%
Output Ripple: 5.0 V ±12 V	V_{in} = 115 Vac	40 mV_{p-p} 80 mV_{p-p}
Efficiency	V_{in} = 115 Vac	70%

All outputs are at nominal load currents unless otherwise noted.

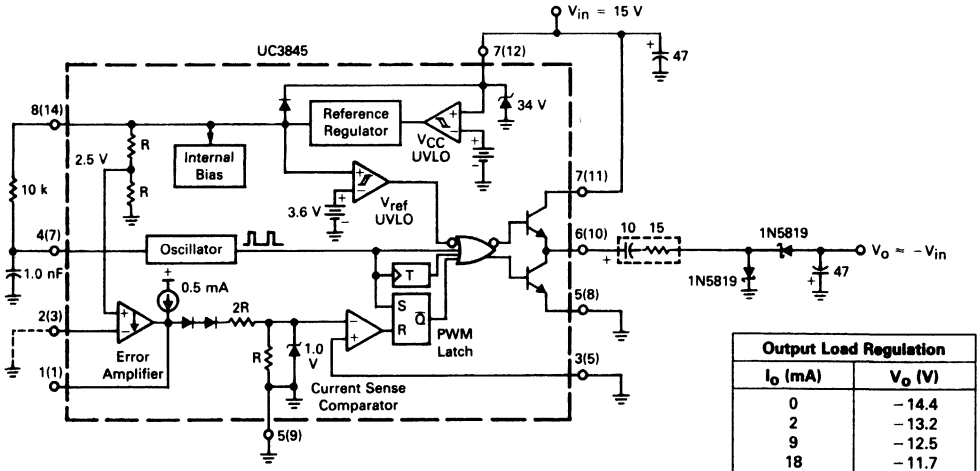
FIGURE 30 — STEP-UP CHARGE PUMP CONVERTER



Output Load Regulation (open loop configuration)	
I_o (mA)	V_o (V)
0	29.9
2	28.8
9	28.3
18	27.4
36	24.4

The capacitor's equivalent series resistance must limit the Drive Output current to 1.0 A.
An additional series resistor may be required when using tantalum or other low ESR capacitors.
The converter's output can provide excellent line and load regulation by connecting the R2/R1 resistor divider as shown.

FIGURE 31 — VOLTAGE-INVERTING CHARGE PUMP CONVERTER



Output Load Regulation	
I_o (mA)	V_o (V)
0	−14.4
2	−13.2
9	−12.5
18	−11.7
32	−10.6

The capacitor's equivalent series resistance must limit the Drive Output current to 1.0 A.
An additional series resistor may be required when using tantalum or other low ESR capacitors.

MOTOROLA

μA78S40

Specifications and Applications Information

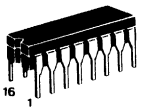
UNIVERSAL SWITCHING REGULATOR SUBSYSTEM

SILICON MONOLITHIC INTEGRATED CIRCUIT

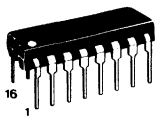
The μA78S40 is a monolithic-switching regulator subsystem, providing all active functions necessary for a switching regulator system. The device consists of a temperature compensated voltage reference, controlled-duty cycle oscillator with an active current limit circuit, comparator, high-current and high-voltage output switch, capable of 1.5 A and 40 V, pinned-out power diode and an uncommitted operational amplifier, which can be powered up or down independent of the IC supply. The switching output can drive external NPN or PNP transistors when voltages greater than 40 V, or currents in excess of 1.5 A, are required. Some of the features are wide-supply voltage range, low standby current, high efficiency and low drift. The μA78S40 is available in commercial (0°C to +70°C), automotive (−40°C to +85°C), and military (−55°C to +125°C) temperature ranges.

Some of the applications include use in step-up, step-down, and inverting regulators, with extremely good results obtained in battery-operated systems.

- Output Adjustable from 1.25 V to 40 V
- Peak Output Current of 1.5 A Without External Transistor
- 80 dB Line and Load Regulation
- Operation from 2.5 V to 40 V Supply
- Low Standby Current Drain
- High Gain, High Output Current, Uncommitted Op Amp

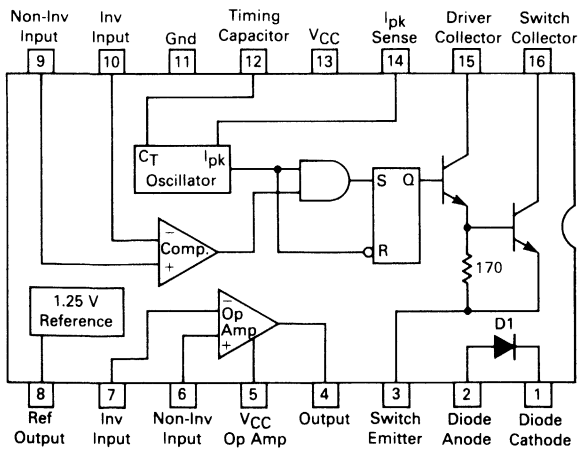


D SUFFIX
CERAMIC PACKAGE
CASE 620-10



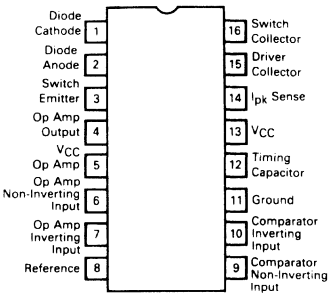
P SUFFIX
PLASTIC PACKAGE
CASE 648-08

BLOCK DIAGRAM



(Bottom View)

PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

Device	Temperature Range	Package
μA78S40PC	0°C to +70°C	Plastic DIP
μA78S40PV	−40°C to +85°C	Plastic DIP
μA78S40DC	0°C to +70°C	Ceramic DIP
μA78S40DM	−55°C to +125°C	Ceramic DIP

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	40	V
Op Amp Power Supply Voltage	V_{CC} (Op Amp)	40	V
Common Mode Input Range (Comparator and Op Amp)	V_{ICR}	−0.3 to V_{CC}	V
Differential Input Voltage (Note 2)	V_{ID}	±30	V
Output Short-Circuit Duration (Op Amp)	—	Continuous	—
Reference Output Current	I_{ref}	10	mA
Voltage from Switch Collectors to Gnd	—	40	V
Voltage from Switch Emitters to Gnd	—	40	V
Voltage from Switch Collectors to Emitter	—	40	V
Voltage from Power Diode to Gnd	—	40	V
Reverse-Power Diode Voltage	V_{DR}	40	V
Current through Power Switch	I_{SW}	1.5	A
Current through Power Diode	I_D	1.5	A
Power Dissipation and Thermal Characteristics Plastic Package — T_A = +25°C Derate above +25°C (Note 1) Ceramic Package — T_A = 25°C Derate above +25°C (Note 1)	 P_D $1/R_{\theta JA}$ P_D $1/R_{\theta JA}$	 1500 14 1000 8.0	 mW mW/°C mW mW/°C
Storage Temperature Range	T_{stg}	−65 to +150	°C
Operating Temperature Range μA78S40M μA78S40V μA78S40C	T_A	 −55 to +125 −40 to +85 0 to +70	°C

Notes:

1. T_{low} = −55°C for μA78S40DM; T_{high} = +125°C for μA78S40DM
   = −40°C for μA78S40PV; = +85°C for μA78S40PV
   = 0°C for μA78S40DC and μA78S40PC; = +70°C for μA78S40DC and μA78S40PC
2. For supply voltages less than 30 V the maximum differential input voltage (Error Amp and Op Amp) is equal to the supply voltage.

ELECTRICAL CHARACTERISTICS (V_{CC} = V_{CC} (Op Amp) = 5.0 V, T_A = T_{low} to T_{high} unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
GENERAL					
Supply Voltage	V_{CC}	2.5	—	40	V
Supply Current (Op Amp V_{CC} Disconnected) (V_{CC} = 5.0 V) (V_{CC} = 40 V)	I_{CC}	 — —	 1.8 2.3	 3.5 5.0	mA
Supply Current (Op Amp V_{CC} Connected) (V_{CC} = 5.0 V) (V_{CC} = 40 V)	I_{CC}	 — —	 — —	 4.0 5.5	mA
REFERENCE					
Reference Voltage (I_{ref} = 1.0 mA)	V_{ref}	1.180	1.245	1.310	V
Reference Voltage Line Regulation (3.0 V ≤ V_{CC} ≤ 40 V, I_{ref} = 1.0 mA, T_A = 25°C)	Reg_{line}	—	0.04	0.2	mV/V
Reference Voltage Load Regulation (1.0 mA ≤ I_{ref} ≤ 10 mA, T_A = 25°C)	Reg_{load}	—	0.2	0.5	mV/mA

ELECTRICAL CHARACTERISTICS (Continued)

Characteristic	Symbol	Min	Typ	Max	Unit
OSCILLATOR					
Charging Current (T_A = 25°C) (V_{CC} = 5.0 V) (V_{CC} = 40 V)	I_{chg}	 20 20	 — —	 50 70	μA
Discharge Current (T_A = 25°C) (V_{CC} = 5.0 V) (V_{CC} = 40 V)	I_{dis}	 150 150	 — —	 250 350	μA
Oscillator Voltage Swing (T_A = 25°C) (V_{CC} = 5.0 V)	V_{osc}	—	0.5	—	V
Ratio of Charge/Discharge Time	t_{chg}/t_{dis}	—	6.0	—	—
CURRENT LIMIT					
Current-Limit Sense Voltage (T_A = 25°C) (V_{CC} – V_{Ipk} Sense)	V_{CLS}	250	—	350	mV
OUTPUT SWITCH					
Output Saturation Voltage 1 (I_{SW} = 1.0 A, Pin 15 tied to Pin 16)	V_{sat1}	—	0.93	1.3	V
Output Saturation Voltage 2 (I_{SW} = 1.0 A, I_{15} = 50 mA)	V_{sat2}	—	0.5	0.7	V
Output Transistor Current Gain (T_A = 25°C) (I_C = 1.0 A, V_{CE} = 5.0 V)	h_{FE}	—	70	—	—
Output Leakage Current (T_A = 25°C) (V_{CE} = 40 V)	$I_{C(off)}$	—	10	—	nA
POWER DIODE					
Forward Voltage Drop (I_D = 1.0 A)	V_D	—	1.25	1.5	V
Diode Leakage Current (T_A = 25°C) (V_{DR} = 40 V)	I_{DR}	—	10	—	nA
COMPARATOR					
Input Offset Voltage (V_{CM} = V_{Ref})	V_{IO}	—	1.5	15	mV
Input Bias Current (V_{CM} = V_{Ref})	I_{IB}	—	35	200	nA
Input Offset Current (V_{CM} = V_{Ref})	I_{IO}	—	5.0	75	nA
Common-Mode Voltage Range (T_A = 25°C)	V_{ICR}	0	—	V_{CC} – 2.0	V
Power-Supply Rejection Ratio (T_A = 25°C) (3.0 ≤ V_{CC} ≤ 40 V)	PSRR	70	96	—	dB
OUTPUT OPERATIONAL AMPLIFIER					
Input Offset Voltage (V_{CM} = 2.5 V)	V_{IO}	—	4.0	15	mV
Input Bias Current (V_{CM} = 2.5 V)	I_{IB}	—	30	200	nA
Input Offset Current (V_{CM} = 2.5 V)	I_{IO}	—	5.0	75	nA
Voltage Gain + (T_A = 25°C) (R_L = 2.0 kΩ to Gnd, 1.0 V ≤ V_O ≤ 2.5 V)	A_{VOL+}	25	250	—	V/mV
Voltage Gain – (T_A = 25°C) (R_L = 2.0 kΩ to V_{CC} (Op Amp), 1.0 V ≤ V_O ≤ 2.5 V)	A_{VOL-}	25	250	—	V/mV
Common-Mode Voltage Range (T_A = 25°C)	V_{ICR}	0	—	V_{CC} – 2.0	V
Common-Mode Rejection Ratio (T_A = 25°C) (V_{CM} = 0 to 3.0 V)	CMRR	76	100	—	dB
Power-Supply Rejection Ratio (T_A = 25°C) (3.0 V ≤ V_{CC} (Op Amp) ≤ 40 V)	PSRR	76	100	—	dB
Output Source Current (T_A = 25°C)	I_{Source}	75	150	—	mA
Output Sink Current (T_A = 25°C)	I_{Sink}	10	35	—	mA
Slew Rate (T_A = 25°C)	SR	—	0.6	—	V/μs
Output Low Voltage (T_A = 25°C, I_L = –5.0 mA)	V_{OL}	—	—	1.0	V
Output High Voltage (T_A = 25°C, I_L = 50 mA)	V_{OH}	V_{CC} (Op Amp) – 3.0	—	—	V

FIGURE 1 — OUTPUT SWITCH ON/OFF TIME versus OSCILLATOR TIMING CAPACITOR

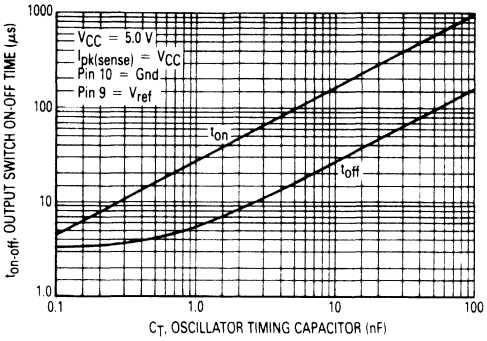


FIGURE 2 — STANDBY SUPPLY CURRENT versus SUPPLY VOLTAGE

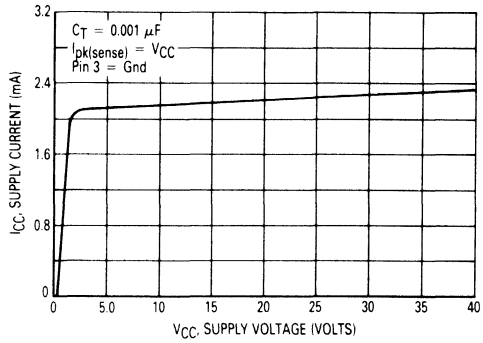


FIGURE 3 — EMITTER-FOLLOWER CONFIGURATION OUTPUT SWITCH SATURATION VOLTAGE versus EMITTER CURRENT

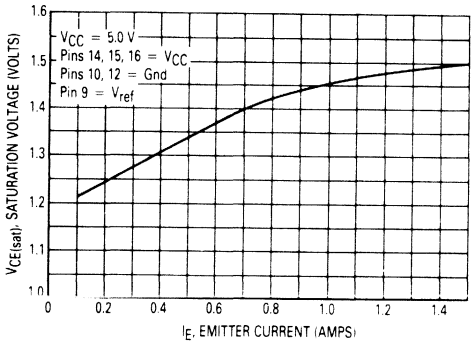


FIGURE 4 — COMMON-EMITTER CONFIGURATION OUTPUT SWITCH SATURATION VOLTAGE versus COLLECTOR CURRENT

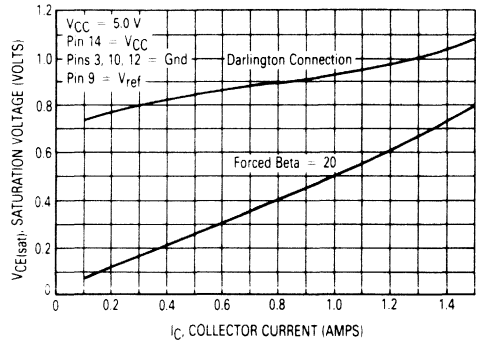


FIGURE 5 — STEP-DOWN CONVERTER

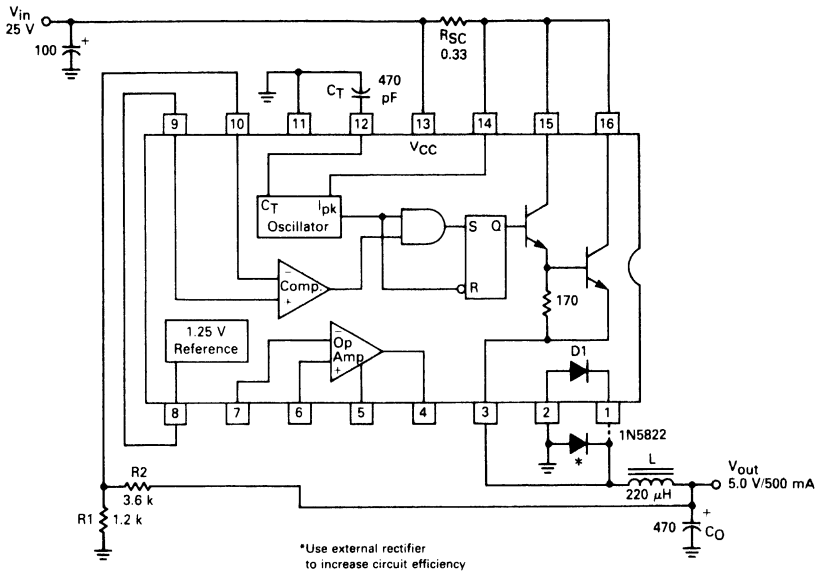


FIGURE 6 — STEP-UP CONVERTER

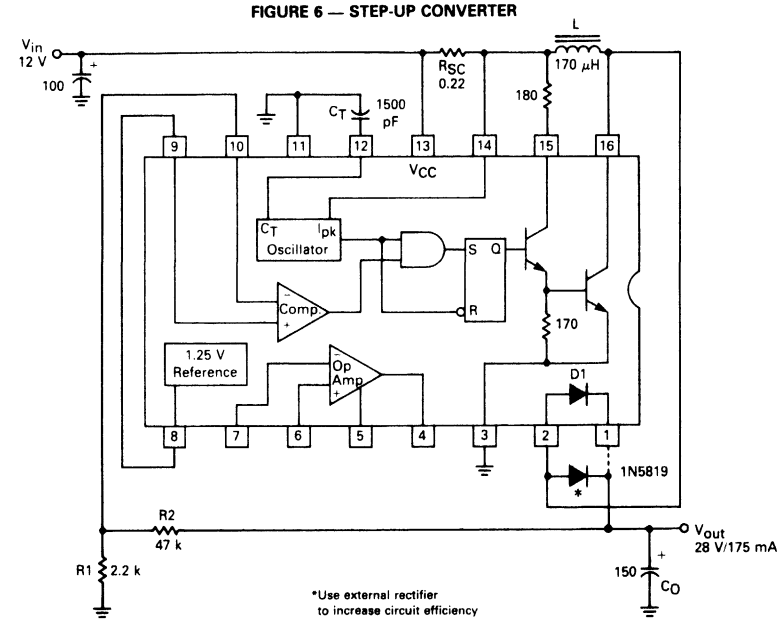


FIGURE 7 — INVERTING CONVERTER

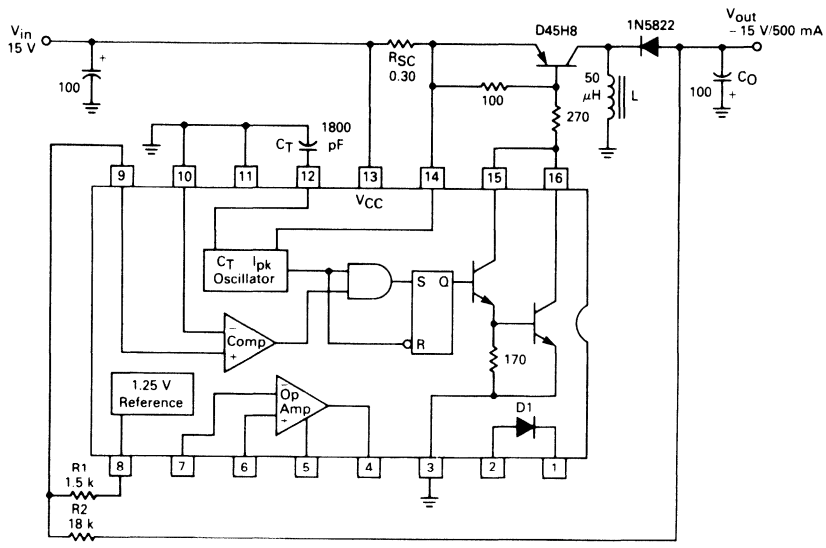


FIGURE 8 — DESIGN FORMULA TABLE

Calculation	Step-Down	Step-Up	Inverting
$\frac{t_{on}}{t_{off}}$	$\frac{V_{out} + V_F}{V_{in(min)} - V_{sat} - V_{out}}$	$\frac{V_{out} + V_F - V_{in(min)}}{V_{in(min)} - V_{sat}}$	$\frac{V_{out} + V_F}{V_{in(min)} - V_{sat}}$
$(t_{on} + t_{off})$ max	$\frac{1}{f_{min}}$	$\frac{1}{f_{min}}$	$\frac{1}{f_{min}}$
C_T	$4 \times 10^{-5} t_{on}$	$4 \times 10^{-5} t_{on}$	$4 \times 10^{-5} t_{on}$
$I_{pk(switch)}$	$2 I_{out(max)}$	$2 I_{out(max)} \left(\frac{t_{on} + t_{off}}{t_{off}}\right)$	$2 I_{out(max)} \left(\frac{t_{on} + t_{off}}{t_{off}}\right)$
R_{SC}	$\frac{0.33}{I_{pk(switch)}}$	$\frac{0.33}{I_{pk(switch)}}$	$\frac{0.33}{I_{pk(switch)}}$
$L_{(min)}$	$\left(\frac{V_{in(min)} - V_{sat} - V_{out}}{I_{pk(switch)}}\right) t_{on(max)}$	$\left(\frac{V_{in(min)} - V_{sat}}{I_{pk(switch)}}\right) t_{on(max)}$	$\left(\frac{V_{in(min)} - V_{sat}}{I_{pk(switch)}}\right) t_{on(max)}$
C_O	$\frac{I_{pk(switch)}(t_{on} + t_{off})}{8 V_{ripple(p-p)}}$	$\approx \frac{I_{out} t_{on}}{V_{ripple}}$	$\approx \frac{I_{out} t_{on}}{V_{ripple}}$

V_{sat} = Saturation voltage of the output switch. V_F = Forward voltage drop of the ringback rectifier.

The following power supply characteristics must be chosen:

V_{in} — Nominal input voltage. If this voltage is not constant, then use $V_{in(max)}$ for step-down and $V_{in(min)}$ for step-up and inverting convertor.

V_{out} — Desired output voltage, $V_{out} = 1.25 \left(1 + \frac{R_2}{R_1}\right)$ for step-down and step-up; $V_{out} = \frac{1.25\ R2}{R1}$ for Inverting.

I_{out} — Desired output current.

f_{min} — Minimum desired output switching frequency at the selected values for V_{in} and I_O.

$V_{ripple(p-p)}$ — Desired peak-to-peak output ripple voltage. In practice, the calculated value will need to be increased due to the capacitor's equivalent series resistance and board layout. The ripple voltage should be kept to a low value since it will directly effect the line and load regulation.

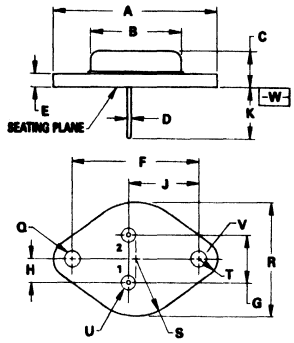
See Application Note AN920A for further information.

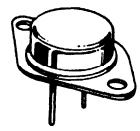
SECTION 19
PACKAGE OUTLINE DIMENSIONS

K SUFFIX
METAL PACKAGE
CASE 1-03
$R_{\theta JA}$ = 45°C/W (TYP)
(TO-3)

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
B	—	22.23	—	0.875
C	6.35	11.43	0.250	0.450
D	0.97	1.09	0.038	0.043
E	—	3.43	—	0.135
F	30.15 BSC		1.187 BSC	
G	10.92 BSC		0.430 BSC	
H	5.46 BSC		0.215 BSC	
J	16.89 BSC		0.665 BSC	
K	7.92	—	0.312	—
Q	3.84	4.09	0.151	0.161
S	—	13.34	—	0.525
T	—	4.78	—	0.188
V	3.84	4.09	0.151	0.161

NOTES:
1. DIAMETER V AND SURFACE W ARE DATUMS.
2. POSITIONAL TOLERANCE FOR HOLE Q:
   ⌖ | ϕ 0.25 (0.010) Ⓜ | W | V Ⓜ |
3. POSITIONAL TOLERANCE FOR LEADS:
   ⌖ | ϕ 0.30 (0.012) Ⓜ | W | V Ⓜ | Q Ⓜ |

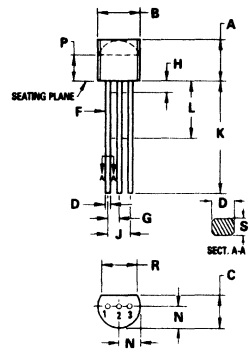




LP, P, Z SUFFIX
PLASTIC PACKAGE
CASE 29-04
$R_{\theta JA}$ = 200°C/W (TYP)
(TO-226AA/TO-92)

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	4.32	5.33	0.170	0.210
B	4.45	5.20	0.175	0.205
C	3.18	4.19	0.125	0.165
D	0.41	0.55	0.016	0.022
F	0.41	0.48	0.016	0.019
G	1.15	1.39	0.045	0.055
H	—	2.54	—	0.100
J	2.42	2.66	0.095	0.105
K	12.70	—	0.500	—
L	6.35	—	0.250	—
N	2.04	2.66	0.080	0.105
P	2.93	—	0.115	—
R	3.43	—	0.135	—
S	0.39	0.50	0.015	0.020

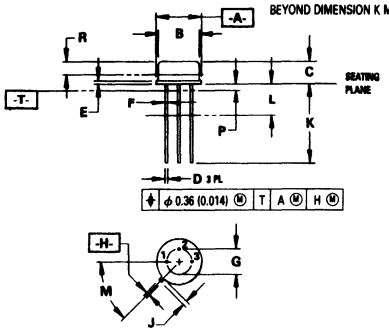
NOTES:
1. CONTOUR OF PACKAGE BEYOND ZONE "P" IS UNCONTROLLED.
2. DIM "F" APPLIES BETWEEN "H" AND "L". DIM "D" & "S" APPLIES BETWEEN "L" & 12.70mm (0.5") FROM SEATING PLANE. LEAD DIM IS UNCONTROLLED IN "H" & BEYOND 12.70mm (0.5") FROM SEATING PLANE.
3. CONTROLLING DIM: INCH.



G, H SUFFIX
METAL PACKAGE
CASE 79-05
$R_{\theta JA}$ = 185°C/W (TYP)
(TO-39)

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	9.02	9.29	0.355	0.366
B	8.01	8.50	0.315	0.335
C	4.20	4.57	0.165	0.180
D	0.44	0.53	0.017	0.021
E	0.44	0.88	0.017	0.035
F	0.41	0.48	0.016	0.019
G	5.08 BSC		0.200 BSC	
H	0.72	0.86	0.028	0.034
J	0.74	1.01	0.029	0.040
K	12.70	19.05	0.500	0.750
L	6.35	—	0.250	—
M	45° BSC		45° BSC	
P	—	1.27	—	0.050
R	2.54	—	0.100	—

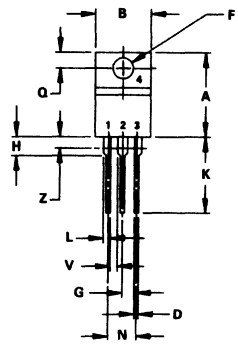
NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION J MEASURED FROM DIMENSION A MAXIMUM.
4. DIMENSION B SHALL NOT VARY MORE THAN 0.25 (0.010) IN ZONE R. THIS ZONE CONTROLLED FOR AUTOMATIC HANDLING.
5. DIMENSION F APPLIES BETWEEN DIMENSION P AND L. DIMENSION D APPLIES BETWEEN DIMENSION L AND K MINIMUM. LEAD DIAMETER IS UNCONTROLLED IN DIMENSION P AND BEYOND DIMENSION K MINIMUM.

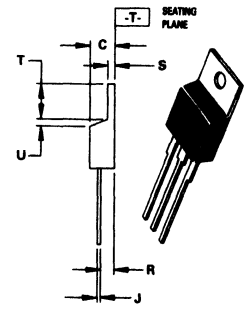


KC, T SUFFIX
PLASTIC PACKAGE
CASE 221A-04
$R_{\theta JA}$ = 65°C/W (TYP)
(TO-220AB)

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	14.48	15.75	0.570	0.620
B	9.66	10.28	0.380	0.405
C	4.07	4.82	0.160	0.190
D	0.64	0.88	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.42	2.66	0.095	0.105
H	2.80	3.93	0.110	0.155
J	0.36	0.55	0.014	0.022
K	12.70	14.27	0.500	0.562
L	1.15	1.39	0.045	0.055
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.15	1.39	0.045	0.055
T	5.97	6.47	0.235	0.255
U	0.00	1.27	0.000	0.050
V	1.15	—	0.045	—
Z	—	2.04	—	0.080

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIM Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.



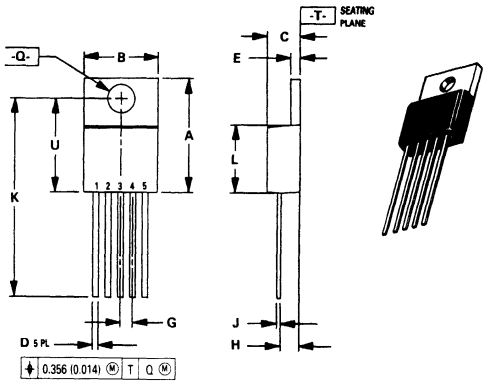


PACKAGE OUTLINE DIMENSIONS (continued)

T SUFFIX
PLASTIC PACKAGE
CASE 314D-02

DIM	MILLIMETERS MIN	MAX	INCHES MIN	MAX
A	14.529	15.570	0.572	0.613
B	9.906	10.541	0.390	0.415
C	4.318	4.572	0.170	0.180
D	0.635	0.965	0.025	0.038
E	1.169	1.397	0.046	0.055
G	1.702 BSC		0.067 BSC	
H	2.109	2.717	0.083	0.107
J	0.381	0.635	0.015	0.025
K	25.807	26.670	1.016	1.050
L	8.052	9.398	0.317	0.370
Q	3.556	3.937	0.140	0.155
U	11.889	12.827	0.468	0.505

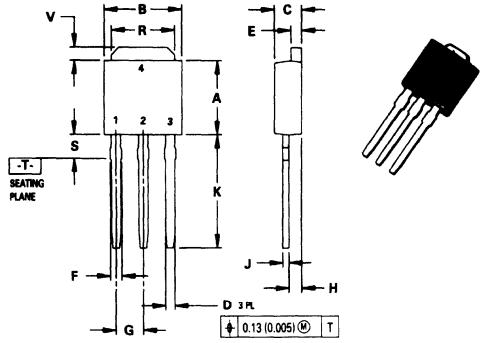
NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.



DT-1 SUFFIX
PLASTIC PACKAGE
CASE 369-03

DIM	MILLIMETERS MIN	MAX	INCHES MIN	MAX
A	5.97	6.22	0.235	0.245
B	6.35	6.73	0.250	0.265
C	2.19	2.38	0.086	0.094
D	0.69	0.88	0.027	0.035
E	0.84	0.94	0.033	0.037
F	0.77	1.14	0.030	0.045
G	2.29 BSC		0.090 BSC	
H	0.97	1.06	0.038	0.042
J	0.46	0.58	0.018	0.023
K	8.89	9.65	0.350	0.380
R	5.21	5.46	0.205	0.215
S	1.91	2.28	0.075	0.090
V	0.89	1.27	0.035	0.050

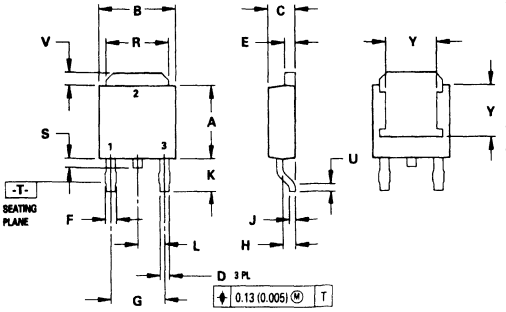
NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.



DT SUFFIX
PLASTIC PACKAGE
CASE 369A-03
DPAK

DIM	MILLIMETERS MIN	MAX	INCHES MIN	MAX
A	5.97	6.22	0.235	0.245
B	6.35	6.73	0.250	0.265
C	2.19	2.38	0.086	0.094
D	0.69	0.88	0.027	0.035
E	0.84	0.94	0.033	0.037
F	0.77	1.14	0.030	0.045
G	4.58 BSC		0.180 BSC	
H	0.97	1.06	0.038	0.042
J	0.46	0.58	0.018	0.023
K	2.60	2.89	0.102	0.114
L	2.29 BSC		0.090 BSC	
R	5.21	5.46	0.205	0.215
S	0.64	0.88	0.025	0.035
U	0.51	—	0.020	—
V	0.89	1.27	0.035	0.050
Y	4.32	—	0.170	—

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

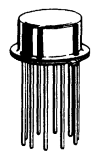


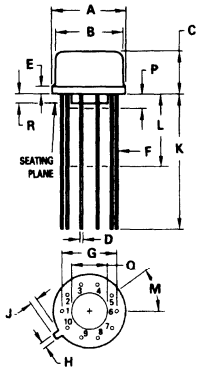
H, G SUFFIX
METAL PACKAGE
CASE 603-04
$R_{\theta JA}$ = 160°C/W
(TO-100)

DIM	MILLIMETERS MIN	MAX	INCHES MIN	MAX
A	8.51	9.39	0.335	0.370
B	7.75	8.51	0.305	0.335
C	4.19	4.70	0.165	0.185
D	0.407	0.533	0.016	0.021
E	—	1.02	—	0.040
F	0.406	0.483	0.016	0.019
G	5.84 BSC		0.230 BSC	
H	0.712	0.864	0.028	0.034
J	0.737	1.14	0.029	0.045
K	12.70	—	0.500	—
L	6.35	12.70	0.250	0.500
M	36° BSC		36° BSC	
P	—	1.27	—	0.050
Q	3.56	4.06	0.140	0.160
R	0.254	1.02	0.010	0.040

NOTE:
LEADS WITHIN 0.18 mm (0.007) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.

All JEDEC Dimensions and Notes Apply.



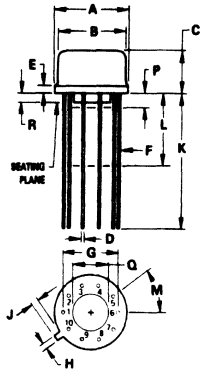


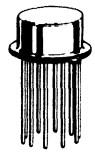
PACKAGE OUTLINE DIMENSIONS (continued)

G SUFFIX
METAL PACKAGE
CASE 603C-01
$R_{\theta JA}$ = 150°C/W (TYP)
(TO-100)

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	8.51	9.39	0.335	0.370
B	7.75	8.51	0.305	0.335
C	4.19	6.73	0.165	0.265
D	0.407	0.533	0.016	0.021
E	—	1.02	—	0.040
F	0.406	0.483	0.016	0.019
G	5.84 BSC		0.230 BSC	
H	0.712	0.864	0.028	0.034
J	0.737	1.14	0.029	0.045
K	12.70	—	0.500	—
L	6.35	12.70	0.250	0.500
M	36° BSC		36° BSC	
P	—	1.27	—	0.050
Q	3.56	4.06	0.140	0.160
R	0.254	1.02	0.010	0.040

NOTES:
1. LEADS WITHIN 0.18 mm (0.007) RADIUS OF TRUE POSITION TO DIM. "A" & "H" AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.
2. LEAD DIA UNCONTROLLED BEYOND DIM "K" MIN.

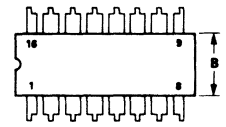


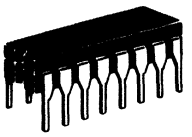


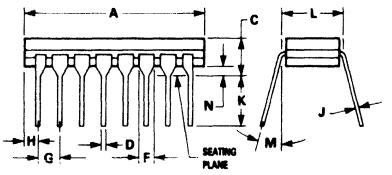
DP2, D, J, L, N SUFFIX
CERAMIC PACKAGE
CASE 620-10
$R_{\theta JA}$ = 100°C/W (TYP)

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	19.05	19.94	0.750	0.785
B	6.10	7.49	0.240	0.295
C	—	5.08	—	0.200
D	0.38	0.53	0.015	0.021
F	1.40	1.78	0.055	0.070
G	2.54 BSC		0.100 BSC	
H	0.51	1.14	0.020	0.045
J	0.20	0.30	0.008	0.012
K	3.18	4.32	0.125	0.170
L	7.62 BSC		0.300 BSC	
M	—	15°	—	15°
N	0.51	1.02	0.020	0.040

NOTES:
1. LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.
2. PACKAGE INDEX: NOTCH IN LEAD NOTCH IN CERAMIC OR INK DOT.
3. DIM "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.
4. DIM "A" AND "B" DO NOT INCLUDE GLASS RUN-OUT.
5. DIM "F" MAY NARROW TO 0.76 mm (0.030) WHERE THE LEAD ENTERS THE CERAMIC BODY.



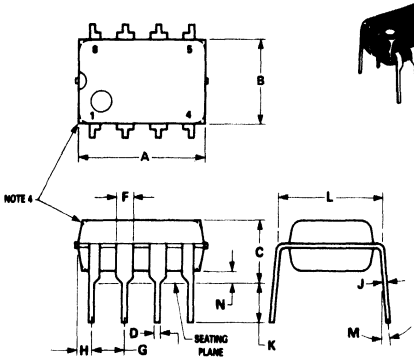




N, P1 SUFFIX
PLASTIC PACKAGE
CASE 626-05
$R_{\theta JA}$ = 100°C/W (TYP)

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	9.40	10.16	0.370	0.400
B	6.10	6.60	0.240	0.260
C	3.94	4.45	0.155	0.175
D	0.38	0.51	0.015	0.020
F	1.02	1.52	0.040	0.060
G	2.54 BSC		0.100 BSC	
H	0.76	1.27	0.030	0.050
J	0.20	0.30	0.008	0.012
K	2.92	3.43	0.115	0.135
L	7.62 BSC		0.300 BSC	
M	—	10°	—	10°
N	0.76	1.01	0.030	0.040

NOTES:
1. LEAD POSITIONAL TOLERANCE:
   ⌖ | ϕ 0.13 (0.005) Ⓜ | T | A Ⓜ | B Ⓜ
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. PACKAGE CONTOUR OPTIONAL (ROUND OR SQUARE CORNERS).
4. DIMENSIONS A AND B ARE DATUMS.
5. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.



L SUFFIX
CERAMIC PACKAGE
CASE 632-08
$R_{\theta JA}$ = 100°C/W (TYP)
(TO-116)

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	19.05	19.94	0.750	0.785
B	6.23	7.11	0.245	0.280
C	3.94	5.08	0.155	0.200
D	0.39	0.50	0.015	0.020
F	1.40	1.65	0.055	0.065
G	2.54 BSC		0.100 BSC	
J	0.21	0.38	0.008	0.015
K	3.18	4.31	0.125	0.170
L	7.62 BSC		0.300 BSC	
M	0°	15°	0°	15°
N	0.51	1.01	0.020	0.040

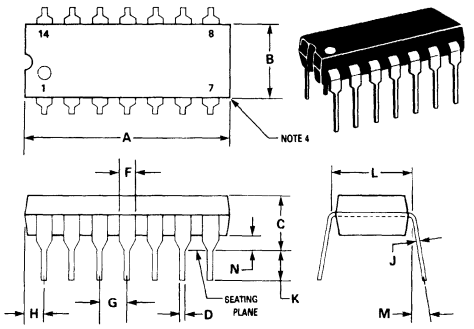
NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
4. DIM F MAY NARROW TO 0.76 (0.030) WHERE THE LEAD ENTERS THE CERAMIC BODY.

PACKAGE OUTLINE DIMENSIONS (continued)

N, P, N-14, P2 SUFFIX
PLASTIC PACKAGE
CASE 646-06
$R_{\theta JA}$ = 100°C/W (TYP)

DIM	MILLIMETERS MIN	MAX	INCHES MIN	MAX
A	18.16	19.56	0.715	0.770
B	6.10	6.60	0.240	0.260
C	3.69	4.69	0.145	0.185
D	0.38	0.53	0.015	0.021
F	1.02	1.78	0.040	0.070
G	2.54 BSC		0.100 BSC	
H	1.32	2.41	0.052	0.095
J	0.20	0.38	0.008	0.015
K	2.92	3.43	0.115	0.135
L	7.62 BSC		0.300 BSC	
M	0°	10°	0°	10°
N	0.39	1.01	0.015	0.039

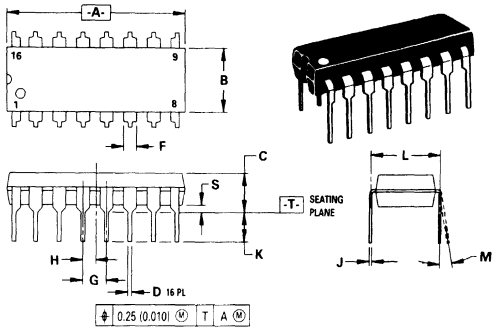
NOTES:
1. LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.
2. DIMENSION "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION "B" DOES NOT INCLUDE MOLD FLASH.
4. ROUNDED CORNERS OPTIONAL.



N, P SUFFIX
PLASTIC PACKAGE
CASE 648-08
$R_{\theta JA}$ = 100°C/W (TYP)

DIM	MILLIMETERS MIN	MAX	INCHES MIN	MAX
A	18.80	19.55	0.740	0.770
B	6.35	6.85	0.250	0.270
C	3.69	4.44	0.145	0.175
D	0.39	0.53	0.015	0.021
F	1.02	1.77	0.040	0.070
G	2.54 BSC		0.100 BSC	
H	1.27 BSC		0.050 BSC	
J	0.21	0.38	0.008	0.015
K	2.80	3.30	0.110	0.130
L	7.50	7.74	0.295	0.305
M	0°	10°	0°	10°
S	0.51	1.01	0.020	0.040

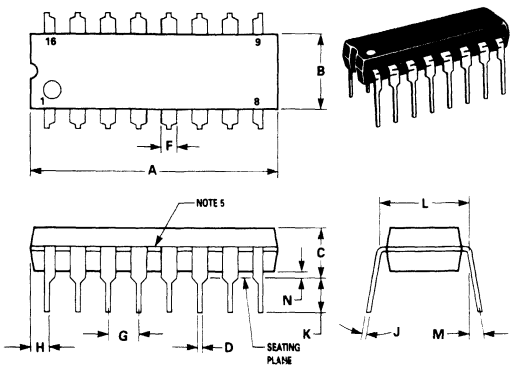
NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.
4. DIMENSION "B" DOES NOT INCLUDE MOLD FLASH.
5. ROUNDED CORNERS OPTIONAL.



P SUFFIX
PLASTIC PACKAGE
CASE 648C-02

DIM	MILLIMETERS MIN	MAX	INCHES MIN	MAX
A	18.80	21.34	0.740	0.840
B	6.10	6.60	0.240	0.260
C	3.69	4.69	0.145	0.185
D	0.38	0.53	0.015	0.021
F	1.02	1.78	0.040	0.070
G	2.54 BSC		0.100 BSC	
H	0.38	2.41	0.015	0.095
J	0.20	0.38	0.008	0.015
K	2.92	3.43	0.115	0.135
L	7.62 BSC		0.300 BSC	
M	0°	10°	0°	10°
N	0.39	1.01	0.015	0.040

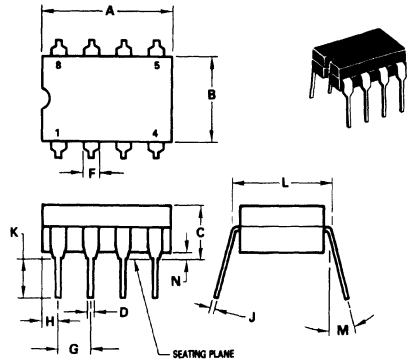
NOTES:
1. LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITON AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.
2. DIMENSION "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION "B" DOES NOT INCLUDE MOLD FLASH.
4. ROUNDED CORNERS OPTIONAL.
5. EXTERNAL LEAD CONNECTION, BETWEEN 4 AND 5, 12 AND 13 AS SHOWN.



J-8, J, JG, U, Z SUFFIX
CERAMIC PACKAGE
CASE 693-02
$R_{\theta JA}$ = 100°C/W (TYP)

DIM	MILLIMETERS MIN	MAX	INCHES MIN	MAX
A	9.91	10.92	0.390	0.430
B	6.22	6.99	0.245	0.275
C	4.32	5.08	0.170	0.200
D	0.41	0.51	0.016	0.020
F	1.40	1.65	0.055	0.065
G	2.54 BSC		0.100 BSC	
H	1.14	1.65	0.045	0.065
J	0.20	0.30	0.008	0.012
K	3.18	4.06	0.125	0.160
L	7.37	7.87	0.290	0.310
M	—	15°	—	15°
N	0.51	1.02	0.020	0.040

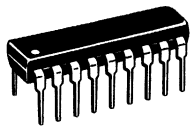
NOTES:
1. LEADS WITHIN 0.13 mm (0.005) RAD OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.
2. DIMENSION "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.



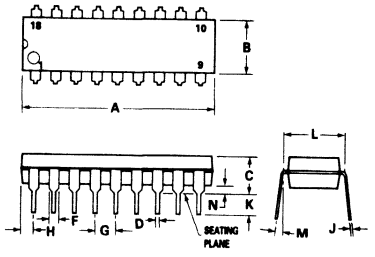
PACKAGE OUTLINE DIMENSIONS (continued)

A, B, N, P SUFFIX
PLASTIC PACKAGE
CASE 707-02
$R_{\theta JA}$ = 100°C/W (TYP)

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	22.22	23.24	0.875	0.915
B	6.10	6.60	0.240	0.260
C	3.56	4.57	0.140	0.180
D	0.36	0.56	0.014	0.022
F	1.27	1.78	0.050	0.070
G	2.54 BSC		0.100 BSC	
H	1.02	1.52	0.040	0.060
J	0.20	0.30	0.008	0.012
K	2.92	3.43	0.115	0.135
L	7.62 BSC		0.300 BSC	
M	0°	15°	0°	15°
N	0.51	1.02	0.020	0.040



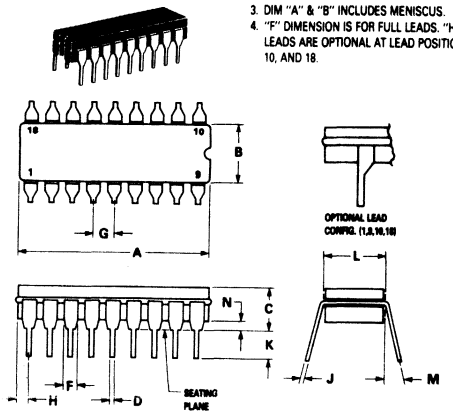
NOTES:
1. POSITIONAL TOLERANCE OF LEADS (D), SHALL BE WITHIN 0.25mm(0.010) AT MAXIMUM MATERIAL CONDITION, IN RELATION TO SEATING PLANE AND EACH OTHER.
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION B DOES NOT INCLUDE MOLD FLASH.



J, L SUFFIX
CERAMIC PACKAGE
CASE 726-04
$R_{\theta JA}$ = 100°C/W (TYP)

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	22.35	23.11	0.880	0.910
B	6.10	7.49	0.240	0.295
C	—	5.08	—	0.200
D	0.38	0.53	0.015	0.021
F	1.40	1.78	0.055	0.070
G	2.54 BSC		0.100 BSC	
H	0.51	1.14	0.020	0.045
J	0.20	0.30	0.008	0.012
K	3.18	4.32	0.125	0.170
L	7.62 BSC		0.300 BSC	
M	0°	15°	0°	15°
N	0.51	1.02	0.020	0.040

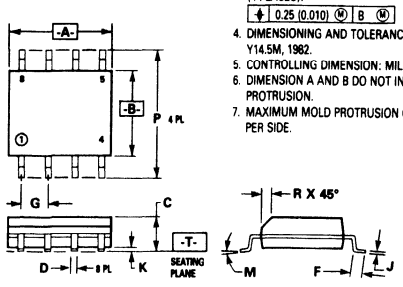
NOTES:
1. LEADS, TRUE POSITIONED WITHIN 0.25 mm (0.010) DIA. AT SEATING PLANE, AT MAXIMUM MATERIAL CONDITION.
2. DIM "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIM "A" & "B" INCLUDES MENISCUS.
4. "F" DIMENSION IS FOR FULL LEADS. "HALF" LEADS ARE OPTIONAL AT LEAD POSITIONS 1, 9, 10, AND 18.



D SUFFIX
CASE 751-03
PLASTIC PACKAGE
SO-8, SOP-8
$R_{\theta JA}$ = 190°C/W (SO-8)
$R_{\theta JA}$ = 160°C/W (SOP-8)

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	4.80	5.00	0.189	0.196
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

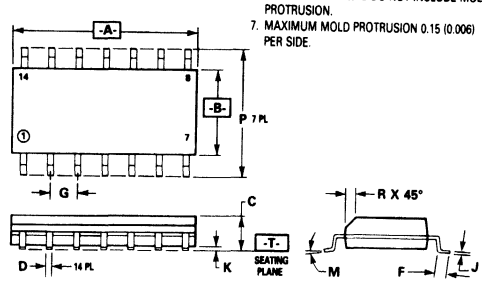
NOTES:
1. DIMENSIONS A AND B ARE DATUMS AND T IS A DATUM SURFACE.
2. POSITIONAL TOLERANCE FOR D DIMENSION (8 PLACES):
   ⌖ 0.25 (0.010) Ⓜ T B Ⓢ A Ⓢ
3. POSITIONAL TOLERANCE FOR P DIMENSION (4 PLACES):
   ⌖ 0.25 (0.010) Ⓜ B Ⓜ
4. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
5. CONTROLLING DIMENSION: MILLIMETER.
6. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
7. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.



D SUFFIX
PLASTIC PACKAGE
CASE 751A-02
SO-14
$R_{\theta JA}$ = 145°C/W (TYP)

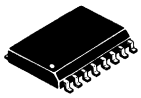
DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	8.55	8.75	0.337	0.344
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

NOTES:
1. DIMENSIONS A AND B ARE DATUMS AND T IS A DATUM SURFACE.
2. POSITIONAL TOLERANCE FOR D DIMENSION (14 PLACES):
   ⌖ 0.25 (0.010) Ⓜ T B Ⓢ A Ⓢ
3. POSITIONAL TOLERANCE FOR P DIMENSION (7 PLACES):
   ⌖ 0.25 (0.010) Ⓜ B Ⓜ
4. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
5. CONTROLLING DIMENSION: MILLIMETER.
6. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
7. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.

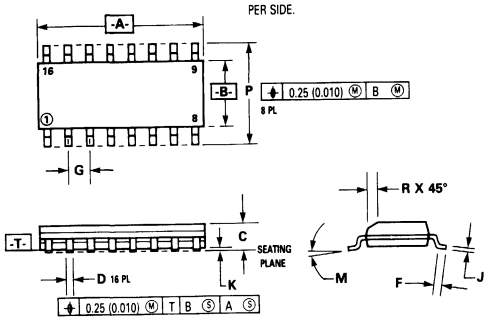


DW SUFFIX
PLASTIC PACKAGE
CASE 751G-01
SO-16L

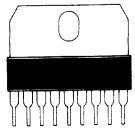
DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	10.15	10.45	0.400	0.411
B	7.40	7.60	0.292	0.299
C	2.35	2.65	0.093	0.104
D	0.35	0.49	0.014	0.019
F	0.50	0.90	0.020	0.035
G	1.27 BSC		0.050 BSC	
J	0.25	0.32	0.010	0.012
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	10.05	10.55	0.395	0.415
	0.25	0.75	0.010	0.029



NOTES:
1. DIMENSIONS A AND B ARE DATUMS AND T IS A DATUM SURFACE.
2. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
3. CONTROLLING DIMENSION: MILLIMETER.
4. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
5. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.

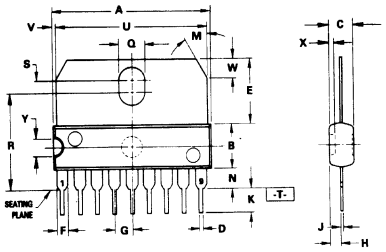


CASE 762-01
PLASTIC MEDIUM
POWER PACKAGE
SIP-9



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	22.40	23.00	0.873	0.897
B	6.40	6.60	0.252	0.260
C	3.45	3.65	0.135	1.143
D	0.40	0.55	0.015	0.021
E	9.35	9.60	0.368	0.377
F	1.40	1.60	0.055	0.062
G	2.54 BSC		0.100BSC	
H	1.51	1.71	0.059	0.067
J	0.360	0.400	0.014	0.015
K	3.95	4.20	0.155	0.165
M	30° BSC		30° BSC	
N	2.50	2.70	0.099	0.106
Q	3.15	3.45	0.124	0.135
R	13.60	13.90	0.535	0.547
S	1.65	1.95	0.064	0.076
U	22.00	22.20	0.866	0.874
V	0.55	0.75	0.021	0.029
W	2.89 BSC		0.113 BSC	
X	0.65	0.75	0.025	0.029
Y	2.70	2.80	0.106	0.110

NOTES:
1. DIMENSIONS A, AND C ARE DATUMS. AND -T- IS A DATUM PLANE.
2. POSITIONAL TOLERANCE FOR LEAD DIMENSION D:
   0.25 (0.010) M -T- A M
3. POSITIONAL TOLERANCE FOR LEAD DIMENSION J:
   0.25 (0.010) M -T- C M
4. POSITIONAL TOLERANCE FOR LEAD DIMENSION Q:
   0.25 (0.010) M -T- A M
5. DIMENSIONING AND TOLERANCING PER ANSI Y14.5, 1982.
6. CONTROLLING DIMENSION: MILLIMETER.



SECTION 20
VOLTAGE REGULATOR
CROSS REFERENCE GUIDE

This cross reference provides a complete interchangeability list linking the most common voltage regulators offered by major Linear Integrated Circuits manufacturers to the nearest equivalent Motorola device. The Motorola "Direct Replacement" column lists devices with identical pin connections and package and the same or better electrical characteristics and temperature range. The Motorola "Functional Equivalent" column provides a device which performs the same function but with possible differences in package configurations, pin connections, temperature range or electrical characteristics.

Reference numbers are listed in alphanumeric sequence, with Greek "μ" preface numbers appearing last.

INDEX CROSS-REFERENCE

Industry Part Number	Motorola Direct Replacement	Motorola Similar Replacement	Page #
AD589J		LM385Z-1.2	—
AD589K		LM385Z-1.2	—
AD589L		LM385Z-1.2	—
AD589M		LM385BZ-1.2	—
AM723DC	MC1723CL		358
AM723DM	MC1723L		358
AM723HC	MC1723CG		358
AM723HM	MC1723G		358
AM723PC	MC1723CP		358
AM7936PC		MC34129P	495
CA723CE	MC1723CP		358
CA723CT	MC1723CG		358
CA723E	MC1723L		358
CA723T	MC1723G		358
CA3085		MC1723G	358
CA3085A		MC1723G	358
CA3085AF		MC1723L	358
CA3085AS		MC1723G	358
CA3085B		MC1723G	358
CA3085BF		MC1723L	358
CA3085BS		MC1723G	358
CA3085F		MC1723L	358
CA3085S		MC1723G	358
ICL8069CCZR		LM385BZ-1.2	—
ICL8069DCZR		LM385BZ-1.2	—
IP494ACJ		TL594CN	570
IP494ACN		TL594CN	570
IP494AJ		TL594MJ	570
IP1525AJ	SG1526AJ		526
IP1526J	SG1526J		526
IP1527AJ	SG1527AJ		519
IP2525AJ	SG2525AJ		519
IP2526J	SG2526J		526
IP2527AJ	SG2527AJ		519
IP3525AJ	SG3525AJ		519
IP3525AN	SG3525AN		519
IP3526J	SG3526J		526
IP3526N	SG3526N		526
IP3527AJ	SG3527AJ		519
IP3527AN	SG3527AN		519
IP33063N	MC33063P1		461
IP34060AN	MC34060AP		442
IP34063N	MC34063P1		461
IP35060AN	MC35060AL		442
IP35063J	MC35063U		461
LM78L05ACH	MC78L05ACG		391
LM78L05ACZ	MC78L05ACP		391
LM78L05CH	MC78L05CG		391
LM78L05CZ	MC78L05CP		391
LM78L08ACH	MC78L08ACG		391
LM78L08ACZ	MC78L08ACP		391
LM78L08CH	MC78L08CG		391
LM78L08CZ	MC78L08CP		391
LM78L12ACH	MC78L12ACG		391
LM78L12ACZ	MC78L12ACP		391
LM78L12CH	MC78L12CG		391
LM78L12CZ	MC78L12CP		391
LM78L15ACH	MC78L15ACG		391
LM78L15ACZ	MC78L15ACP		391
LM78L15CH	MC78L15CG		391
LM78L15CZ	MC78L15CP		391
LM78L18ACZ	MC78L18ACP		391
LM78L18CZ	MC78L18CP		391
LM78L24ACZ	MC78L24ACP		391
LM78L24CZ	MC78L24CP		391
LM78M05CP		MC78M05CT	397
LM78M12CP		MC78M12CT	397
LM78M15CP		MC78M15CT	397
LM79L05ACZ	MC79L05ACP		423
LM79L12ACZ	MC79L12ACP		423
LM79L15ACZ	MC79L15ACP		423
LM79M05CP		MC79M05CT	428
LM79M12CP		MC79M12CT	428
LM79M15CP		MC79M15CT	428
LM109H	LM109H		260
LM109K	LM109K		260
LM109LA	LM109K		260
LM117H	LM117H		265
LM117K	LM117K		265
LM117LA	LM117H		265
LM117LH	LM117LH		273
LM120H-5.0		MC7905CK	414
LM120H-12		MC7912CK	414
LM120H-15		MC7915CK	414
LM120K-5.0		MC7905CK	414
LM120K-12		MC7912CK	414
LM120K-15		MC7915CK	414
LM123AK	LM123AK		281
LM123K	LM123K		281
LM125H		MC1568G	352
LM126H		MC1568G	352
LM128H		MC1568G	352
LM137H	LM137H		287
LM137K	LM137K		287
LM140AK-5.0	LM140AK-5.0		294
LM140AK-12	LM140AK-12		294
LM140AK-15	LM140AK-15		294
LM140K-5.0	LM140K-5.0		294
LM140K-8.0	LM140K-8.0		294
LM140K-12	LM140K-12		294
LM140K-15	LM140K-15		294
LM140LAH-5.0		MC78L05ACG	391
LM140LAH-6.0		MC78L05ACG	391
LM140LAH-8.0		MC78L08ACG	391
LM140LAH-12		MC78L12ACG	391
LM140LAH-15		MC78L15ACG	391
LM140LAH-50		MC78L05ACG	391
LM140LAH-80		MC78L05ACG	391
LM145K		MC7905CK	414
LM150K	LM150K		310
LM209H	LM209H		260
LM209K	LM209K		260
LM209LA	LM209H		260
LM217H	LM217H		265
LM217K	LM217K		265
LM217KC		LM217K	265
LM217KD		LM217H	265
LM217LA	LM217H		265
LM217LH	LM217LH		273
LM220H-5.0		MC7905CK	414
LM220H-12		MC7912CK	414
LM220H-15		MC7915CK	414
LM220K-5.0		MC7905CK	414
LM220K-12		MC7912CK	414
LM220K-15		MC7915CK	414
LM223AK	LM223AK		281
LM223K	LM223K		281
LM225H		MC1568G	352
LM226H		MC1568G	352
LM228H		MC1568G	352
LM237H	LM237H		287
LM237K	LM237K		287
LM240LAH-5.0		MC78L05ACG	391
LM240LAH-8.0		MC78L08ACG	391
LM240LAH-12		MC78L12ACG	391
LM240LAH-15		MC78L15ACG	391
LM240LAZ-5.0		MC78L05ACP	391
LM240LAZ-8.0		MC78L08ACP	391
LM240LAZ-12		MC78L12ACP	391
LM240LAZ-15		MC78L15ACP	391
LM240LAZ-18		MC78L18ACP	391
LM240LAZ-24		MC78L24ACP	391
LM245K		MC7905CK	414
LM250K	LM2540K		310

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LM285Z-1.2	LM285Z-1.2		—
LM285Z-2.5	LM285Z-2.5		—
LM309H	LM309H		260
LM309K	LM309K		260
LM309KC	LM309K		260
LM309LA	LM309K		260
LM317H	LM317H		265
LM317K	LM317K		265
LM317KC	LM317T		265
LM317KD		LM317T	265
LM317LA	LM317H		265
LM317LH	LM317LH		273
LM317LZ	LM317LZ		273
LM317MP	LM317MT		318
LM317MT	LM317MT		318
LM317P	LM317T		265
LM317T	LM317T		265
LM320H-5.0		MC7905CK	414
LM320H-12		MC7912CK	414
LM320H-15		MC7915CK	414
LM320K-5.0	MC7905CK		414
LM320K-12	MC7912CK		414
LM320K-15	MC7915CK		414
LM320LZ-5.0	MC79L05ACP		423
LM320LZ-12	MC79L12ACP		423
LM320LZ-15	MC79L15ACP		423
LM320MP-5.0		MC7905CT	414
LM320MP-5.2		MC7905.2CT	414
LM320MP-6.0		MC7906CT	414
LM320MP-8.0		MC7908CT	414
LM320MP-12		MC7912CT	414
LM320MP-15		MC7915CT	414
LM320MP-18		MC7918CT	414
LM320MP-24		MC7924CT	414
LM320T-5.0	MC7905CT		414
LM320T-5.2		MC7905.2CT	414
LM320T-12	MC7912CT		414
LM320T-15	MC7915CT		414
LM323AK	LM323AK		281
LM323AT	LM323AT		281
LM323K	LM323K		281
LM323T	LM323T		281
LM325AN		MC1468L	352
LM325AS		MC1468L	352
LM325G		MC1468L	352
LM325H		MC1468G	352
LM325N		MC1468L	352
LM326H		MC1468G	352
LM326N		MC1468L	352
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LM328AN		MC1468L	352
LM328H		MC1468G	352
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LM337MP		LM337MT	326
LM337MT	LM337MT		326
LM337T	LM337T		287
LM340AK-5.0	LM340AK-5.0		294
LM340AK-12	LM340AK-12		294
LM340AK-15	LM340AK-15		294
LM340AT-5.0	LM340AT-5.0		294
LM340AT-12	LM340AT-12		294
LM340AT-15	LM340AT-15		294
LM340K-5.0	LM340K-5.0		294
LM340K-5.0	MC7805CK		378
LM340K-6.0	MC7806CK		378
LM340K-8.0	LM340K-8.0		294
LM340K-8.0	MC7808CK		378
LM340K-12	LM340K-12		294
LM340K-15	LM340K-15		294
LM340KC-5.0	LM340T-5.0		294

Industry Part Number	Motorola Direct Replacement	Motorola Similar Replacement	Page #
LM340KC-6.0		MC7806CK	294
LM340KC-8.0		MC7808CK	294
LM340KC-12	LM340T-12		378
LM340KC-15	LM340T-15		378
LM340KC-18	MC7818CK		378
LM340KC-24	MC7824CK		378
LM340LAH-5.0		MC78L05ACG	391
LM340LAH-8.0		MC78L08ACG	391
LM340LAH-12		MC78L12ACG	391
LM340LAH-15		MC78L15ACG	391
LM340LAZ-5.0		MC78L05ACP	391
LM340LAZ-8.0		MC78L08ACP	391
LM340LAZ-12		MC78L12ACP	391
LM340LAZ-15		MC78L15ACP	391
LM340LAZ-18		MC78L18ACP	391
LM340LAZ-24		MC78L24ACP	391
LM340T-5.0	LM340T-5.0		294
LM340T-5.0	MC7805CT		378
LM340T-6.0	LM340T-6.0		294
LM340T-6.0	MC7806CT		378
LM340T-8.0	LM340T-8.0		294
LM340T-8.0	MC7808CT		378
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LM340T-15	MC7815CT		378
LM340T-18	LM340T-18		294
LM340T-18	MC7818CT		378
LM340T-24	LM340T-24		294
LM340T-24	MC7824CT		378
LM341P-5.0	MC78M05CT		397
LM341P-6.0	MC78M06CT		397
LM341P-8.0	MC78M08CT		397
LM341P-12	MC78M12CT		397
LM341P-15	MC78M15CT		397
LM341P-18	MC78M18CT		397
LM341P-24	MC78M24CT		397
LM342P-5.0	MC78M05CT		397
LM342P-6.0	MC78M06CT		397
LM342P-8.0	MC78M08CT		397
LM342P-12	MC78M12CT		397
LM342P-15	MC78M15CT		397
LM342P-18	MC78M18CT		397
LM342P-24	MC78M24CT		397
LM345K		MC7905CK	414
LM350K	LM350K		310
LM350T	LM350T		310
LM385BZ-1.2		LM385BZ-1.2	—
LM385Z-1.2		LM385Z-1.2	—
LM385BZ-2.5		LM385BZ-2.5	—
LM385Z-2.5		LM385Z-2.5	—
LM723CD	LM723CJ		—
LM723CH	MC1723CG		358
LM723CJ	MC1723CL		358
LM723CN	MC1723CP		358
LM723D	LM723J		—
LM723H	MC1723G		358
LM723J	MC1723L		358
LM2931AT-5.0	LM2931AT-5.0		333
LM2931AZ-5.0	LM2931AZ-5.0		333
LM2931CM	LM2931CD		333
LM2931CT	LM2931CT		333
LM2931T-5.0	LM2931T-5.0		333
LM2931Z-5.0	LM2931Z-5.0		333
LM7805CK	MC7805CK		378
LM7805CT	MC7805CT		378
LM7805KC	MC7805CK		378
LM7806KC	MC7806CK		378
LM7808KC	MC7808CK		378
LM7812CK	MC7812CK		378
LM7812CT	MC7812CT		378
LM7812KC	MC7812CK		378

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Industry Part Number	Motorola Direct Replacement	Motorola Similar Replacement	Page #
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